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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f745zgt6

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2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and a low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4 Kbytes of I-cache and 4 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up the software development by using metalanguage development tools, while avoiding saturation.

[Figure 2](#) shows the general block diagram of the STM32F745xx and STM32F746xx devices.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

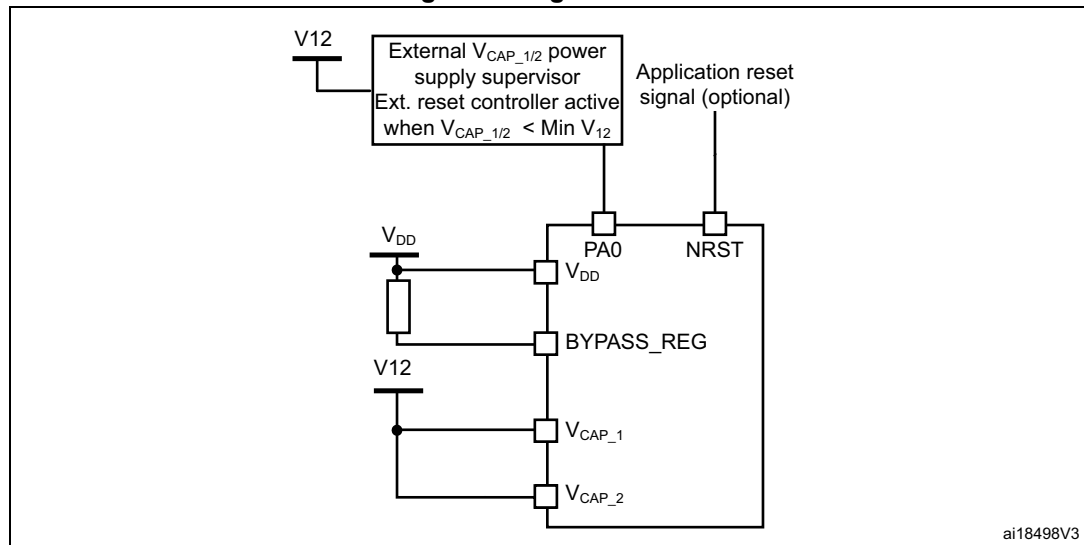
The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 9](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 10](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in Stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in Stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

2.22.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.22.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F74xxx devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F74xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

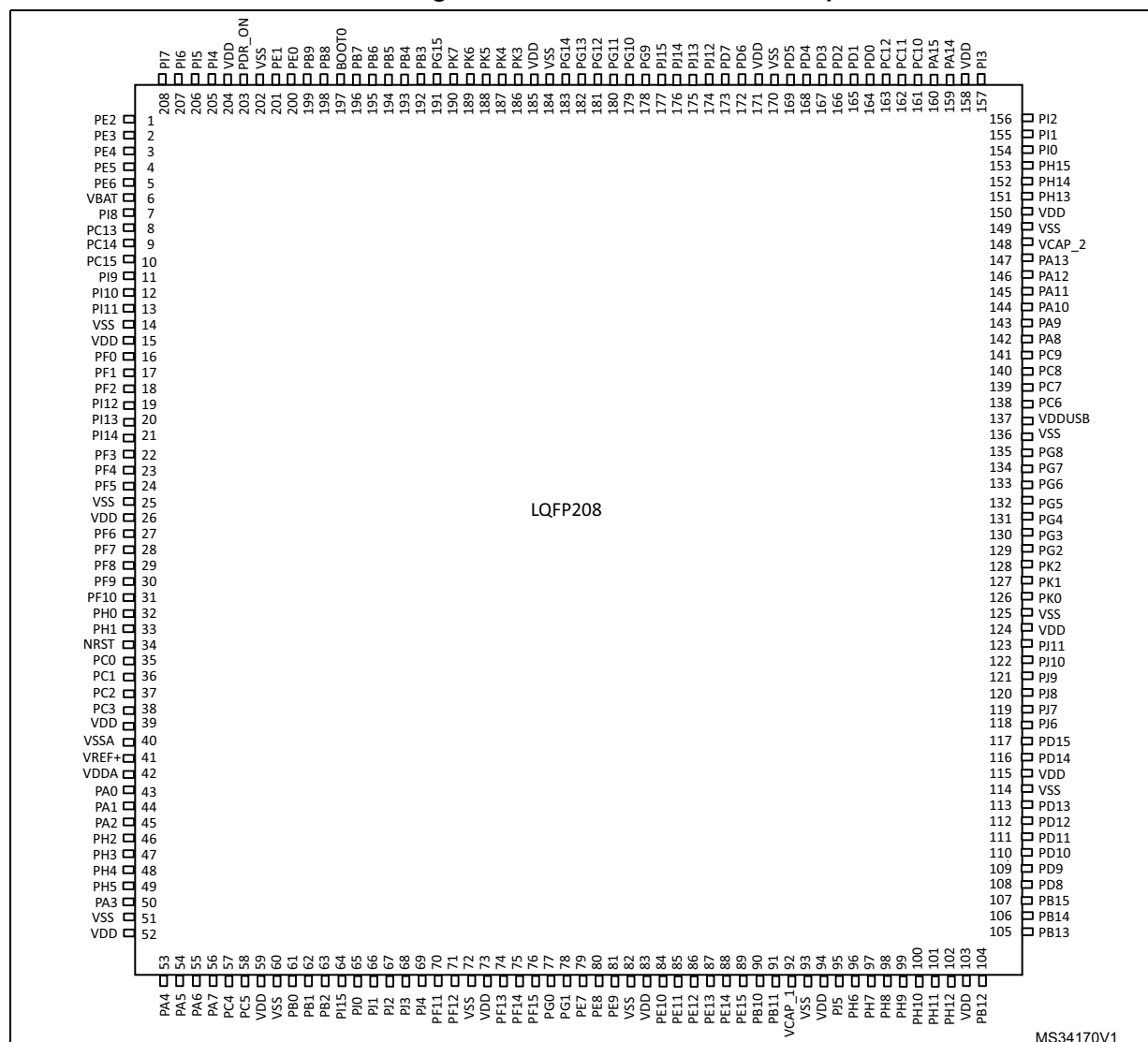
Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Figure 16. STM32F74xBx LQFP208 pinout



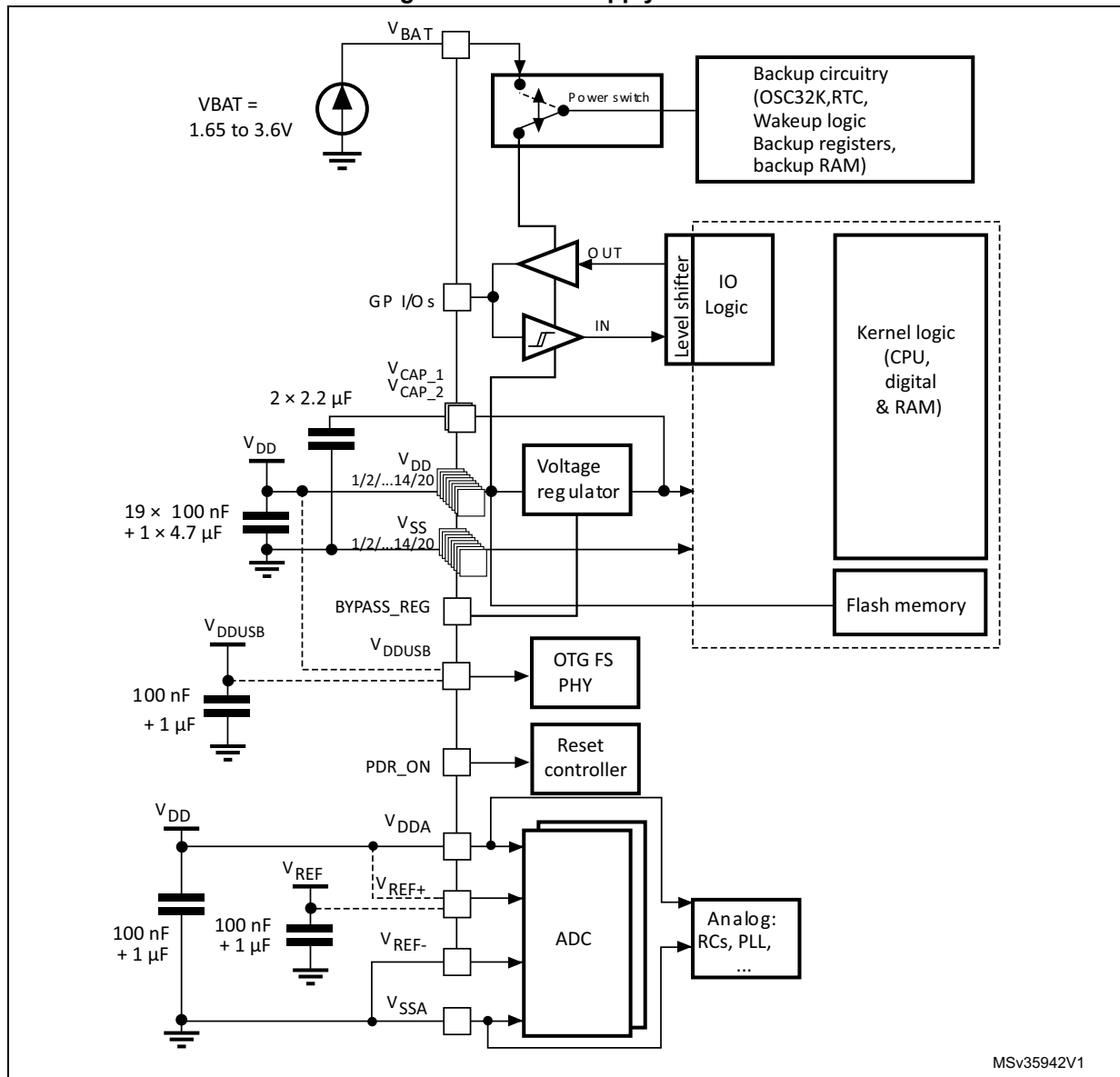
1. The above figure shows the package top view.

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
4	D3	D9	4	B2	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	E3	E8	5	B3	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	-	G6	VSS	S	-	-	-	-
-	-	-	-	-	-	-	F5	VDD	S	-	-	-	-
6	B2	C11	6	C1	6	6	C1	VBAT	S	-	-	-	-
-	-	-	-	D2	7	7	C2	PI8	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP2/ RTC_TS,WK UP5
7	A2	D10	7	D1	8	8	D1	PC13	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP1/ RTC_TS/RTC _OUT,WKUP 4
8	A1	D11	8	E1	9	9	E1	PC14- OSC32_I N(PC14)	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
9	B1	E11	9	F1	10	10	F1	PC15- OSC32_ OUT(PC 15)	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	G5	VDD	S	-	-	-	-
-	-	-	-	D3	11	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	-	-	E3	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-

5.1.6 Power supply scheme

Figure 22. Power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to [Section 2.17: Power supply supervisor](#) and [Section 2.18: Voltage regulator](#)
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 19. VCAP1/VCAP2 operating conditions⁽¹⁾

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 μ F
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 μ F V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t _{VDD}	V _{DD} rise time rate	20	∞	μ s/V
	V _{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up / power-down (regulator OFF)⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t _{VDD}	V _{DD} rise time rate	Power-up	20	∞	μ s/V
	V _{DD} fall time rate	Power-down	20	∞	
t _{VCAP}	V _{CAP_1} and V _{CAP_2} rise time rate	Power-up	20	∞	
	V _{CAP_1} and V _{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

5.3.5 Reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 34. Switching output I/O current consumption⁽¹⁾ (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V _{DD} = 3.3 V	Typ V _{DD} = 1.8 V	Unit
I _{DDIO}	I/O switching Current	C _{EXT} = 22 pF C = C _{INT} + C _S + C _{EXT}	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C _{EXT} = 33 pF C = C _{INT} + C _S + C _{EXT}	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. C_{INT} + C_S, PCB board capacitance including the pad pin is estimated to 15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V_{I2} = 1.32 V.
- HCLK is the system clock. f_{PCLK1} = f_{HCLK}/4, and f_{PCLK2} = f_{HCLK}/2.

The given value is calculated by measuring the difference of current consumption

- with all peripherals clocked off
- with only one peripheral clocked on
- f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

5.3.10 Internal clock source characteristics

The parameters given in [Table 41](#) and [Table 42](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

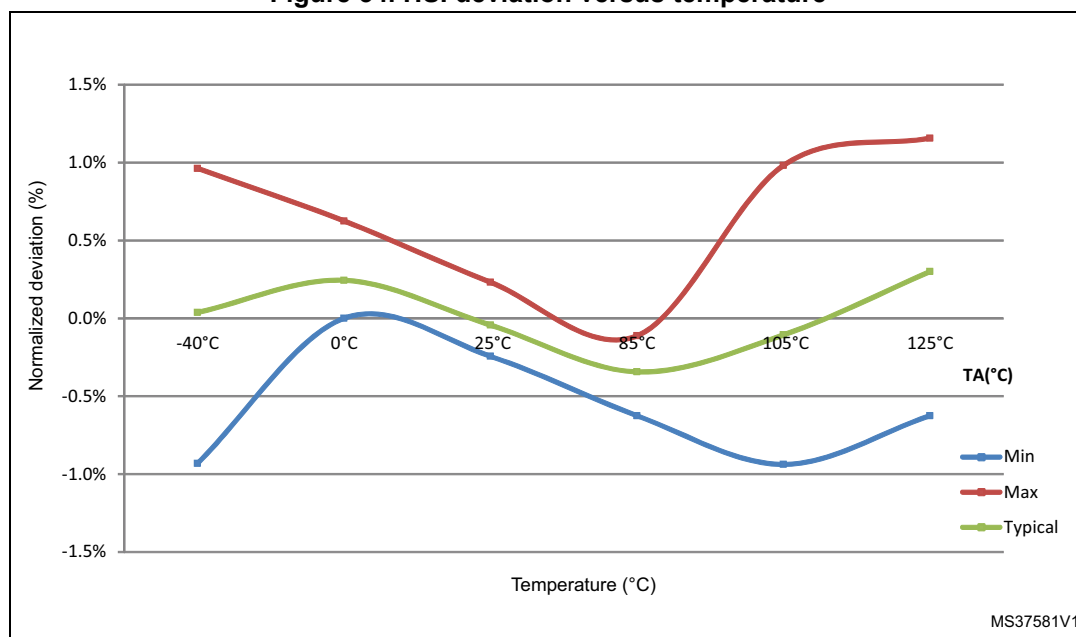
High-speed internal (HSI) RC oscillator

Table 41. HSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step ⁽²⁾	-	-	-	1	%
	Accuracy of the HSI oscillator	$T_A = -40$ to $105\text{ }^{\circ}\text{C}$ ⁽³⁾	- 8	-	4.5	%
		$T_A = -10$ to $85\text{ }^{\circ}\text{C}$ ⁽³⁾	- 4	-	4	%
		$T_A = 25\text{ }^{\circ}\text{C}$ ⁽⁴⁾	- 1	-	1	%
$t_{su(HSI)}$ ⁽²⁾	HSI oscillator startup time	-	-	2.2	4	μs
$I_{DD(HSI)}$ ⁽²⁾	HSI oscillator power consumption	-	-	60	80	μA

1. $V_{DD} = 3.3\text{ V}$, $T_A = -40$ to $105\text{ }^{\circ}\text{C}$ unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 34. HSI deviation versus temperature



1. Guaranteed by characterization results.

Table 48. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{ERASE256KB}	Sector (256 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t _{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	8	16	s
		Program/erase parallelism (PSIZE) = x 16	-	5.6	11.2	
		Program/erase parallelism (PSIZE) = x 32	-	4	8	
V _{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

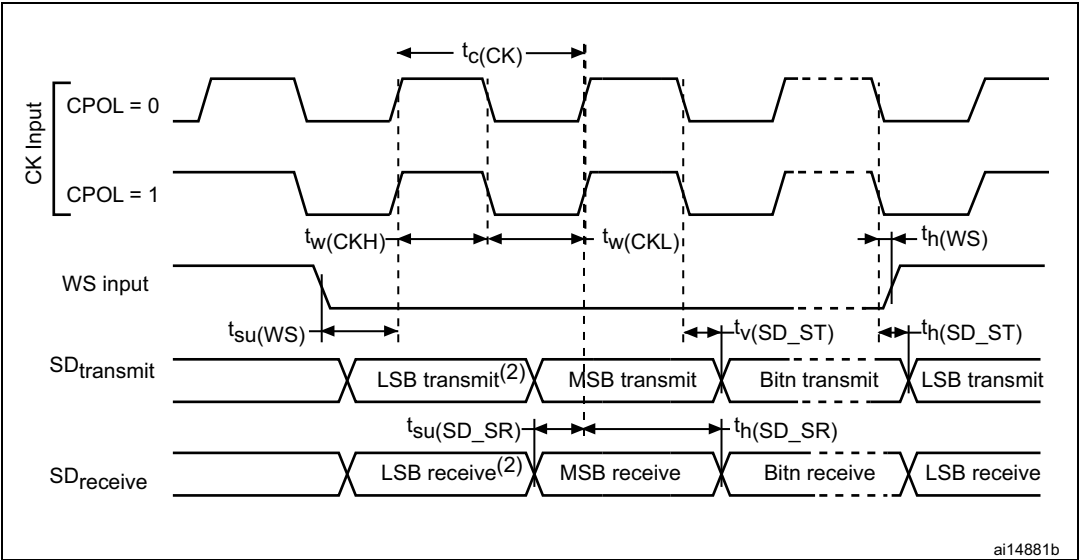
1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t _{prog}	Double word programming	T _A = 0 to +40 °C V _{DD} = 3.3 V V _{PP} = 8.5 V	-	16	100 ⁽²⁾	μs
t _{ERASE32KB}	Sector (32 KB) erase time		-	180	-	ms
t _{ERASE128KB}	Sector (128 KB) erase time		-	450	-	
t _{ERASE256KB}	Sector (256 KB) erase time		-	900	-	
t _{ME}	Mass erase time	-	-	6.9	-	s
V _{prog}	Programming voltage	-	2.7	-	3.6	V
V _{PP}	V _{PP} voltage range	-	7	-	9	V
I _{PP}	Minimum current sunk on the V _{PP} pin	-	10	-	-	mA
t _{VPP} ⁽³⁾	Cumulative time during which V _{PP} is applied	-	-	-	1	hour

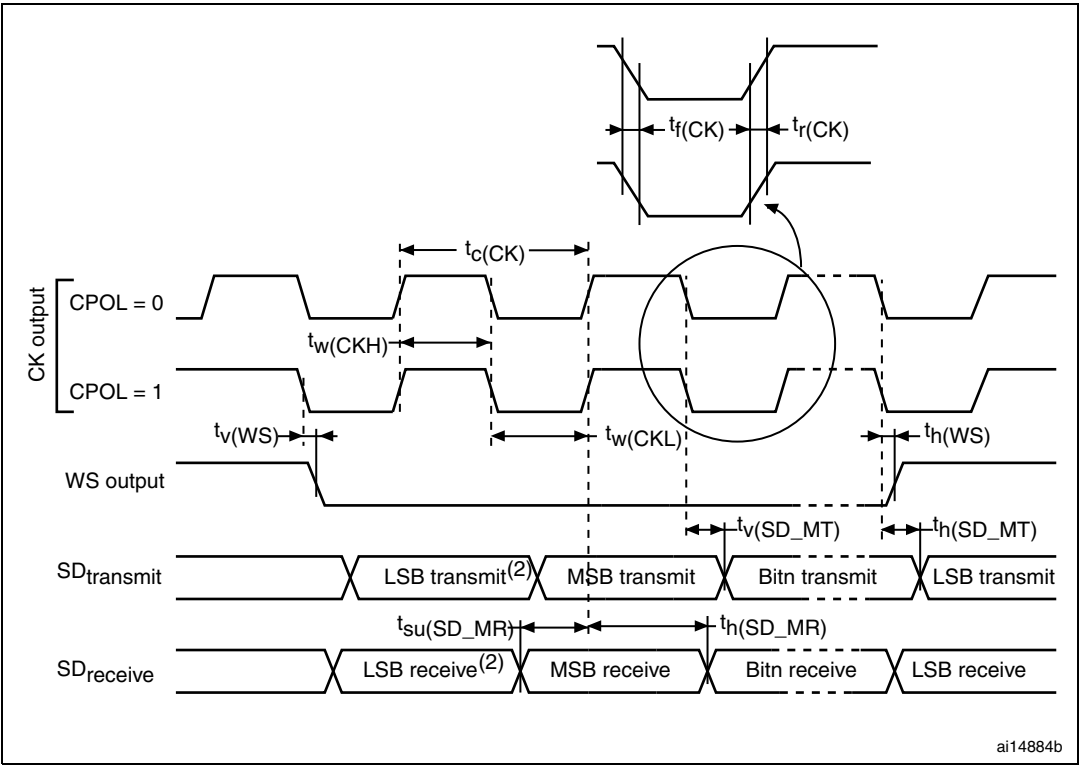
1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Figure 49. I²S slave timing diagram (Philips protocol)⁽¹⁾



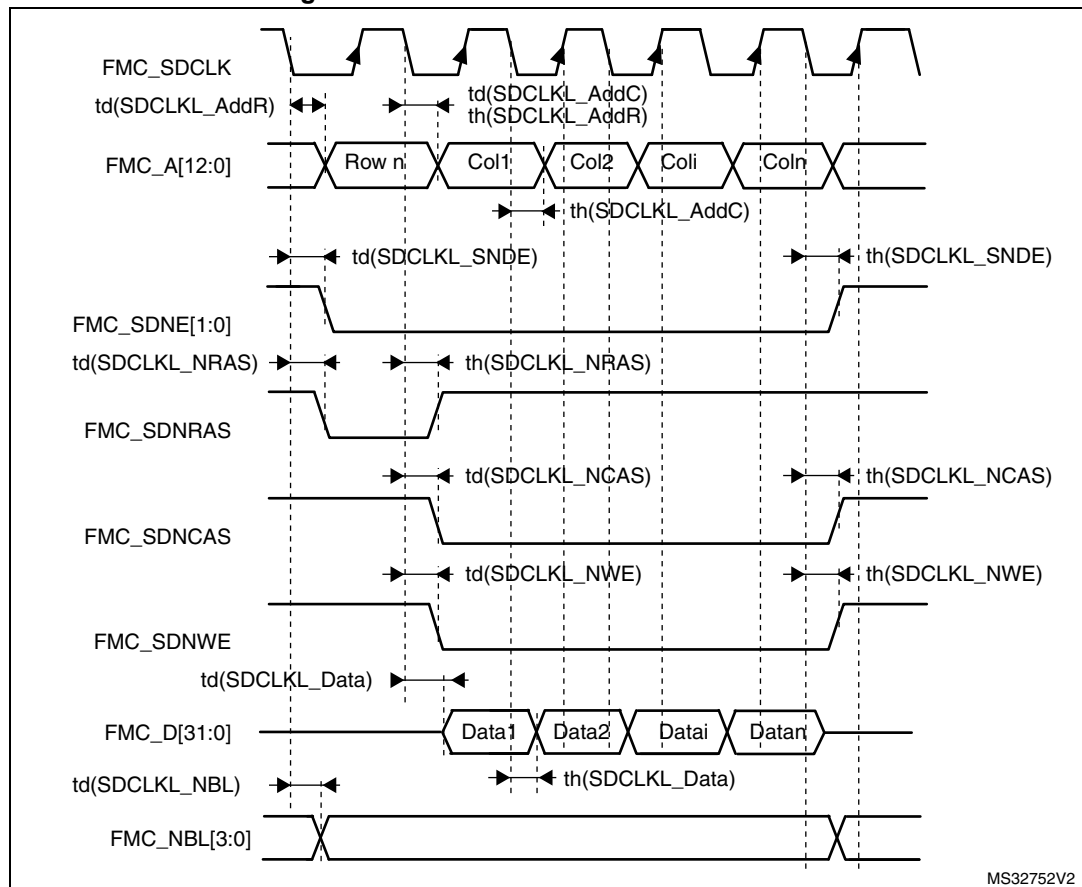
1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)⁽¹⁾



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 71. SDRAM write access waveforms

Table 104. SDRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}} - 0.5$	$2T_{\text{HCLK}} + 0.5$	ns
$t_d(\text{SDCLKL_Data})$	Data output valid time	-	2	
$t_h(\text{SDCLKL_Data})$	Data output hold time	0.5	-	
$t_d(\text{SDCLKL_Add})$	Address valid time	-	4	
$t_d(\text{SDCLKL_SDNWE})$	SDNWE valid time	-	0.5	
$t_h(\text{SDCLKL_SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL_SDNE})$	Chip select valid time	-	0.5	
$t_h(\text{SDCLKL_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL_SDNRAS})$	SDNRAS valid time	-	0.5	
$t_h(\text{SDCLKL_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL_SDNCAS})$	SDNCAS valid time	-	0.5	
$t_h(\text{SDCLKL_SDNCAS})$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 106. Quad-SPI characteristics (continued) in SDR mode⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	$t(CK)/2 - 1$	-	$t(CK)/2$	ns
tw(CKL)			$t(CK)/2$	-	$t(CK)/2 + 1$	
ts(IN)	Data input setup time	-	1	-	-	
th(IN)	Data input hold time		3	-	-	
tv(OUT)	Data output valid time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	1.5	3	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	1.5	4	
th(OUT)	Data output hold time	-	0	-	-	

1. Guaranteed by characterization results.

Table 107. Quad-SPI characteristics in DDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$ CL=20 pF	-	-	80	MHz
		$1.8\text{ V} < V_{DD} < 3.6\text{ V}$ CL=15 pF	-	-	80	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	$t(CK)/2 - 1$	-	$t(CK)/2$	ns
tw(CKL)			$t(CK)/2$	-	$t(CK)/2 + 1$	
ts(IN), tsf(IN)	Data input setup time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	1.5	-	-	
		$1.71\text{ V} < V_{DD} < 2\text{ V}$	0.75	-	-	
thr(IN), thf(IN)	Data input hold time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	3.5	-	-	
		$1.71\text{ V} < V_{DD} < 2\text{ V}$	4.5	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	8	10.5	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$ DHHC=0	-	8	14.5	
		DHHC=1 Pres=1, 2...	-	Thclk/2 +1.75	Thclk/2 +2.25	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	7.5	-	-	
		DHHC=1 Pres=1, 2...	Thclk/2 +1.5	-	-	

1. Guaranteed by characterization results.

Table 110. Dynamic characteristics: SD / MMC characteristics, $V_{DD}=2.7V$ to $3.6V^{(1)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
t _{W(CKL)}	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
t _{W(CKH)}	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	fpp =50 MHz	2.5	-	-	ns
t _{IH}	Input hold time HS	fpp =50 MHz	3	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t _{OV}	Output valid time HS	fpp =50 MHz	-	11.5	12	ns
t _{OH}	Output hold time HS	fpp =50 MHz	10.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t _{ISUD}	Input setup time SD	fpp =25 MHz	2	-	-	ns
t _{IHD}	Input hold time SD	fpp =25 MHz	4	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t _{OVD}	Output valid default time SD	fpp =25 MHz	-	1.5	2	ns
t _{OHD}	Output hold default time SD	fpp =25 MHz	0.5	-	-	

1. Guaranteed by characterization results,.

Table 111. Dynamic characteristics: eMMC characteristics, $V_{DD}=1.71V$ to $1.9V^{(1)(2)}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
t _{W(CKL)}	Clock low time	fpp =50 MHz	9.5	10.5	-	ns
t _{W(CKH)}	Clock high time	fpp =50 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t _{ISU}	Input setup time HS	fpp =50 MHz	0.5	-	-	ns
t _{IH}	Input hold time HS	fpp =50 MHz	3.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t _{OV}	Output valid time HS	fpp =50 MHz	-	12	12.5	ns
t _{OH}	Output hold time HS	fpp =50 MHz	11	-	-	

1. Guaranteed by characterization results.

2. $C_{load} = 20$ pF.

Table 112. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 119. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.