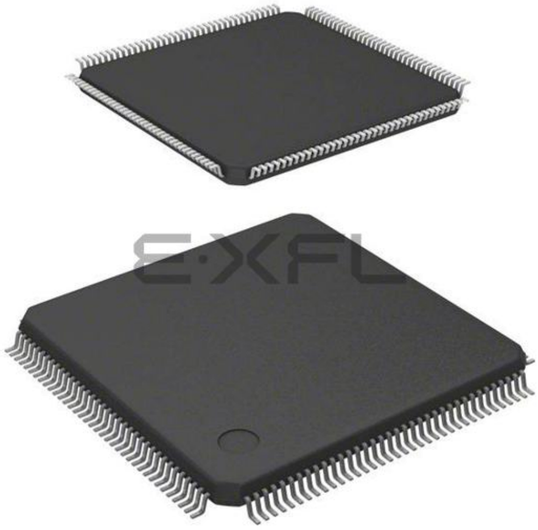
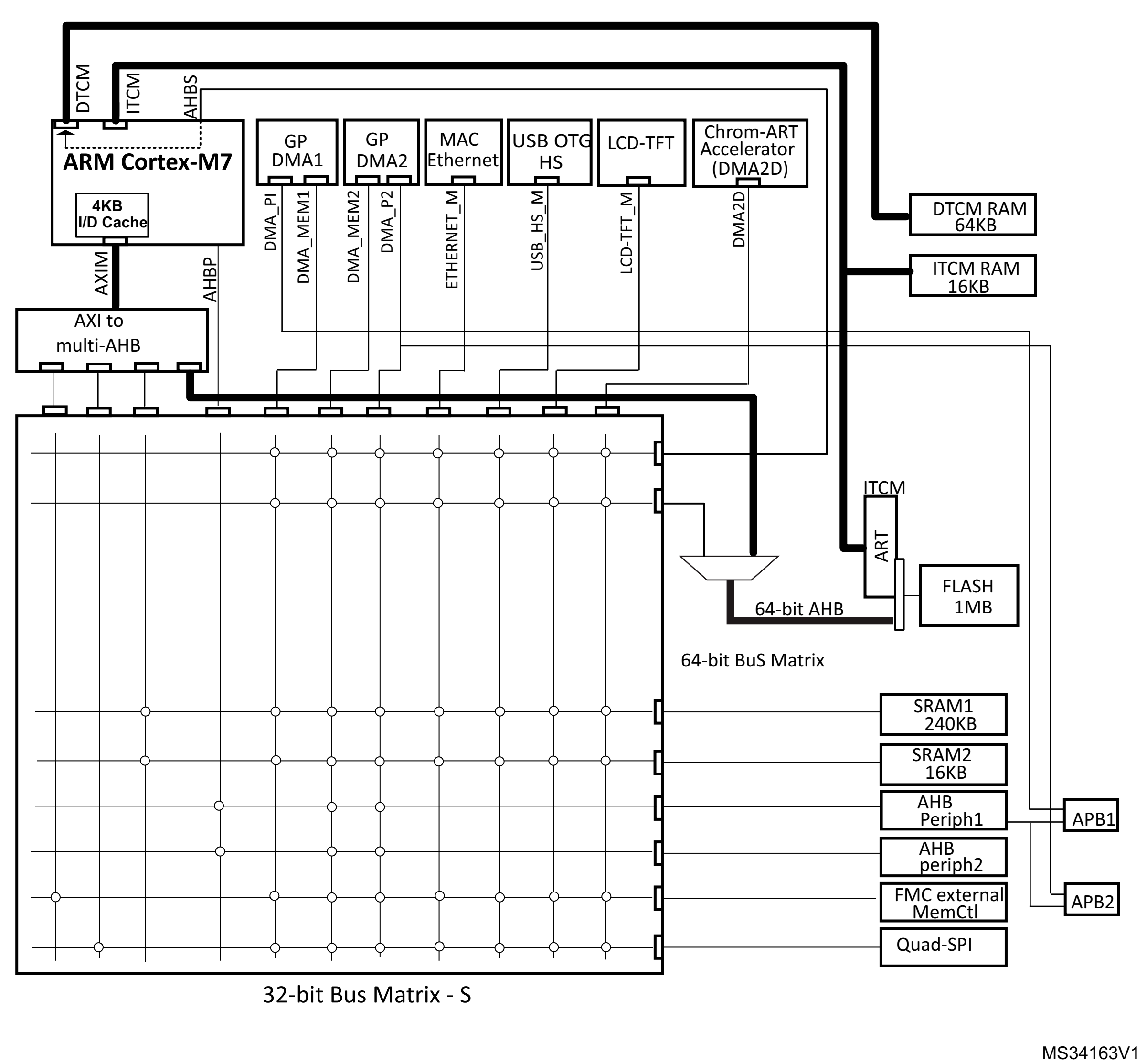


Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f745zgt7

Figure 3. STM32F745xx and STM32F746xx AXI-AHB bus matrix architecture



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

2.15 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface.

2.16 Power supply schemes

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DD} = 1.7 to 3.6 Vexternal power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 2.17.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 4* and *Figure 5*). For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:
  - During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
  - During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
  - V_{DDSUB} rising and falling time rate specifications must be respected (see *Table 20* and *Table 21*)
  - In operating mode phase, V_{DDUSB} could be lower or higher than $V_{DD:}$

    - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.

    - The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.

    - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

2.23 Inter-integrated circuit interface (I^2C)

The device embeds 4 I2C. Refer to *Table 7: I2C implementation* for the features implementation.

The I^2C bus interface handles communication between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus^{TM}) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X

1. X: supported

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)[(1)]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
31	K3	L8	43	R3	53	56	R3	PA7	I/O	FT	(4)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
32	G4	M8	44	N5	54	57	N5	PC4	I/O	FT	(4)	I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
33	H4	N9	45	P5	55	58	P5	PC5	I/O	FT	(4)	SPDIFRX_IN3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	J7	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-
34	J4	N8	46	R5	56	61	R5	PB0	I/O	FT	(4)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
35	K4	K7	47	R4	57	62	R4	PB1	I/O	FT	(4)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
36	G5	L7	48	M6	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

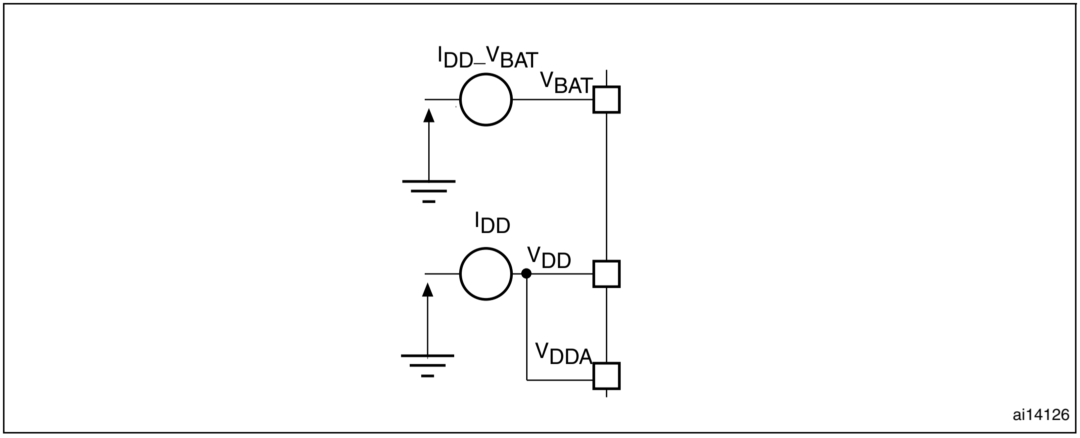
Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
53	H10	K3	75	R14	94	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
54	G10	J3	76	R15	95	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
55	K9	L2	77	P15	96	108	L15	PD8	I/O	FT	-	USART3_TX, SPDIFRX_IN11, FMC_D13, EVENTOUT	-
56	J9	M1	78	P14	97	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
57	H9	H4	79	N15	98	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	G9	K2	80	N14	99	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	K10	H6	81	N13	100	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	J10	H5	82	M15	101	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-

Table 12. STM32F745xx and STM32F746xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	-	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	-	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT

5.1.7 Current consumption measurement

Figure 23. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics*, and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{DD}, V_{BAT} and V_{DDUSB}) (1)	− 0.3	4.0	V
V_{IN}	Input voltage on FT pins[2]	V_{SS} − 0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS} − 0.3	4.0	
	Input voltage on any other pin	V_{SS} − 0.3	4.0	
	Input voltage on BOOT pin	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins[3]	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.15: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}, V_{DDUSB}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 15* for the values of the maximum allowed injected current.
3. Include VREF- pin.

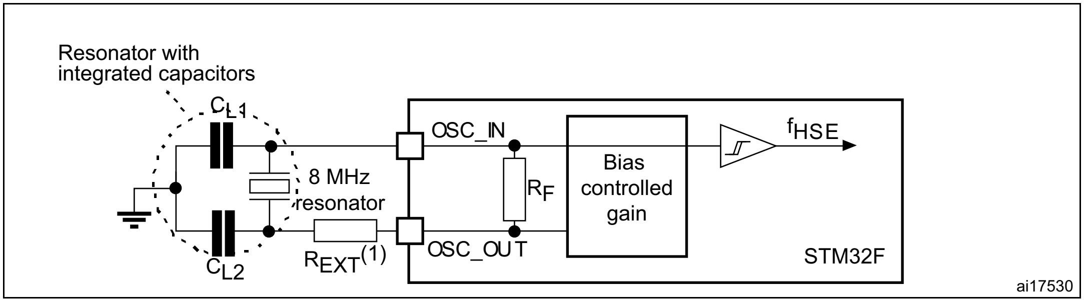
Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)[1]			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 54 MHz)	TIM2	19.8	18.7	16.1	µA/MHz
	TIM3	16.6	15.1	13.6	
	TIM4	16.2	15.1	13.3	
	TIM5	19	17.8	15.8	
	TIM6	3	2.7	2.5	
	TIM7	3	2.7	2.5	
	TIM12	12.4	11.3	10.3	
	TIM13	6	5.3	5	
	TIM14	6	5.3	5	
	LPTIM1	9.4	8.7	8.1	
	WWDG	1.8	1.6	1.4	
	SPI2/I2S2[3]	3	2.9	2.8	
	SPI3/I2S3[3]	3.2	2.9	2.8	
	SPDIFRX	2.2	2	1.7	
	USART2	12.8	12	10.8	
	USART3	15.6	14.2	13.1	
	UART4	11.8	10.7	9.7	
	UART5	11.2	10	9.2	
	I2C1	9.8	8.7	7.8	
	I2C2	8.6	7.8	7.2	
	I2C3	8.6	7.8	7.2	
	I2C4	12	10.9	9.7	
	CAN1	6.8	6	5.6	
	CAN2	6.8	6	5.8	
	CEC	1	0.7	0.8	
	PWR	1.2	0.9	0.8	
	DAC[4]	3	2.7	2.5	
	UART7	12.4	11.6	10	
	UART8	10.4	9.3	8.6	

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 32*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 32. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 58*, respectively.

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 58. I/O AC characteristics(1)(2)

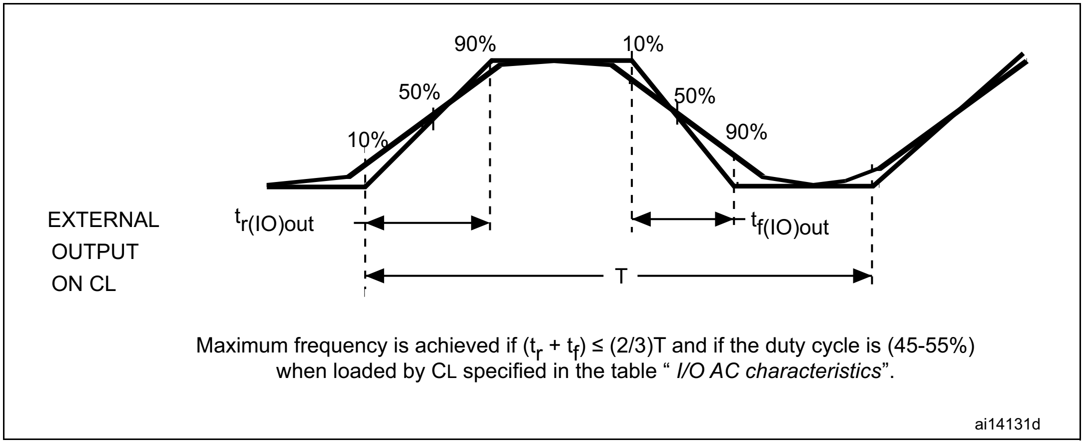
OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	$C_L = 50$ pF, $V_{DD} \geq 2.7$ V	-	-	4	MHz
			$C_L = 50$ pF, $V_{DD} \geq 1.7$ V	-	-	2	
			$C_L = 10$ pF, $V_{DD} \geq 2.7$ V	-	-	8	
			$C_L = 10$ pF, $V_{DD} \geq 1.8$ V	-	-	4	
			$C_L = 10$ pF, $V_{DD} \geq 1.7$ V	-	-	3	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50$ pF, $V_{DD} = 1.7$ V to 3.6 V	-	-	100	ns
01	$f_{max(IO)out}$	Maximum frequency(3)	$C_L = 50$ pF, $V_{DD} \geq 2.7$ V	-	-	25	MHz
			$C_L = 50$ pF, $V_{DD} \geq 1.8$ V	-	-	12.5	
			$C_L = 50$ pF, $V_{DD} \geq 1.7$ V	-	-	10	
			$C_L = 10$ pF, $V_{DD} \geq 2.7$ V	-	-	50	
			$C_L = 10$ pF, $V_{DD} \geq 1.8$ V	-	-	20	
			$C_L = 10$ pF, $V_{DD} \geq 1.7$ V	-	-	12.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50$ pF, $V_{DD} \geq 2.7$ V	-	-	10	ns
			$C_L = 10$ pF, $V_{DD} \geq 2.7$ V	-	-	6	
			$C_L = 50$ pF, $V_{DD} \geq 1.7$ V	-	-	20	
			$C_L = 10$ pF, $V_{DD} \geq 1.7$ V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	$C_L = 40$ pF, $V_{DD} \geq 2.7$ V	-	-	50(4)	MHz
			$C_L = 10$ pF, $V_{DD} \geq 2.7$ V	-	-	100(4)	
			$C_L = 40$ pF, $V_{DD} \geq 1.7$ V	-	-	25	
			$C_L = 10$ pF, $V_{DD} \geq 1.8$ V	-	-	50	
			$C_L = 10$ pF, $V_{DD} \geq 1.7$ V	-	-	42.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 40$ pF, $V_{DD} \geq 2.7$ V	-	-	6	ns
			$C_L = 10$ pF, $V_{DD} \geq 2.7$ V	-	-	4	
			$C_L = 40$ pF, $V_{DD} \geq 1.7$ V	-	-	10	
			$C_L = 10$ pF, $V_{DD} \geq 1.7$ V	-	-	6	

Table 58. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

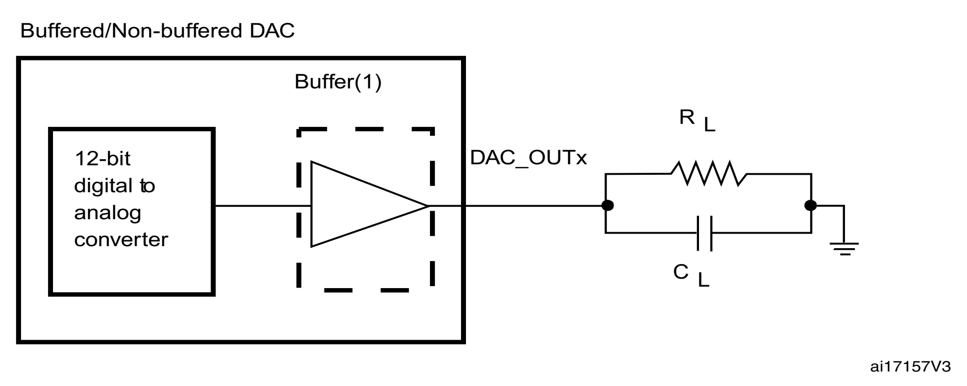
1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F75xxx and STM32F74xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 39*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 39. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

Figure 45. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 Communications interfaces

I^{2}C interface characteristics

The I^{2}C interface meets the timings requirements of the I^{2}C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I^{2}C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0385 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 74. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog Filtre ON DNF=0	10	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	22.5	
			Analog Filtre OFF DNF=1	16	

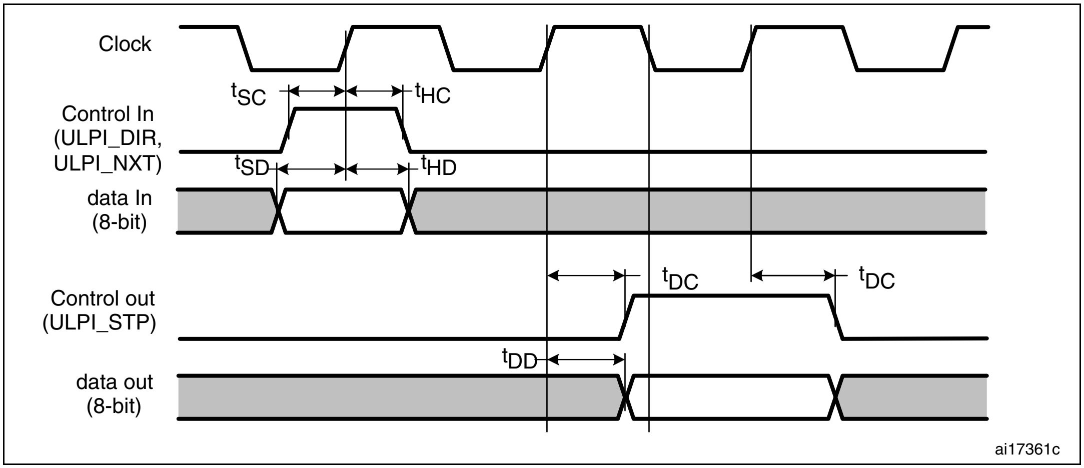
The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

Table 83. USB HS clock timing parameters[1]

Symbol	Parameter		Min	Typ	Max	Unit
-	f_{HCLK} value to guarantee proper operation of USB HS interface		30	-	-	MHz
F_{START_8BIT}	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
D_{START_8BIT}	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
t_{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
t_{START_DEV}	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
t_{START_HOST}		Host	-	-	-	
t_{PREP}	PHY preparation time after the first transition of the input clock		-	-	-	µs

1. Guaranteed by design.

Figure 54. ULPI timing diagram



5.3.27 FMC characteristics

Unless otherwise specified, the parameters given in *Table 88* to *Table 101* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 58 through *Figure 61* represent asynchronous waveforms and *Table 88* through *Table 95* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Figure 71. SDRAM write access waveforms

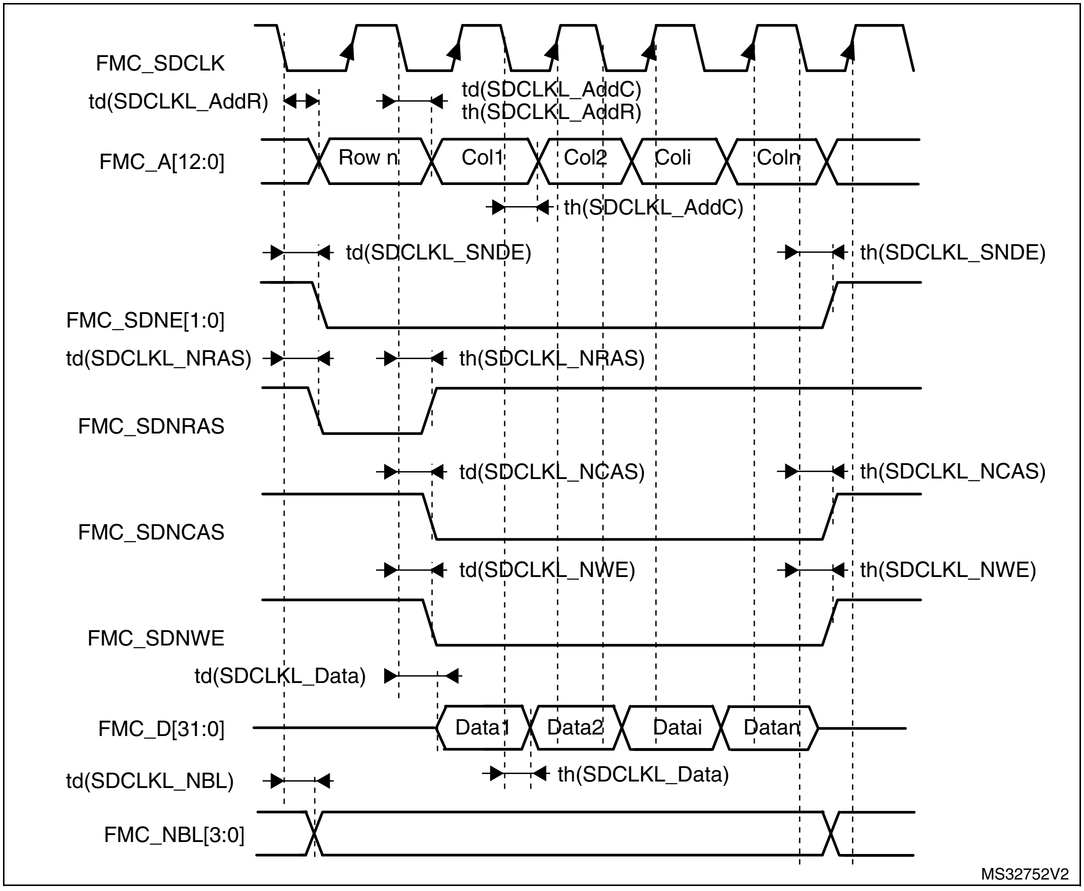


Table 104. SDRAM write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	4	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	0.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 105. LPSDR SDRAM write timings[(1)]

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	4	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	0.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

5.3.28 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 106* and *Table 107* for Quad-SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

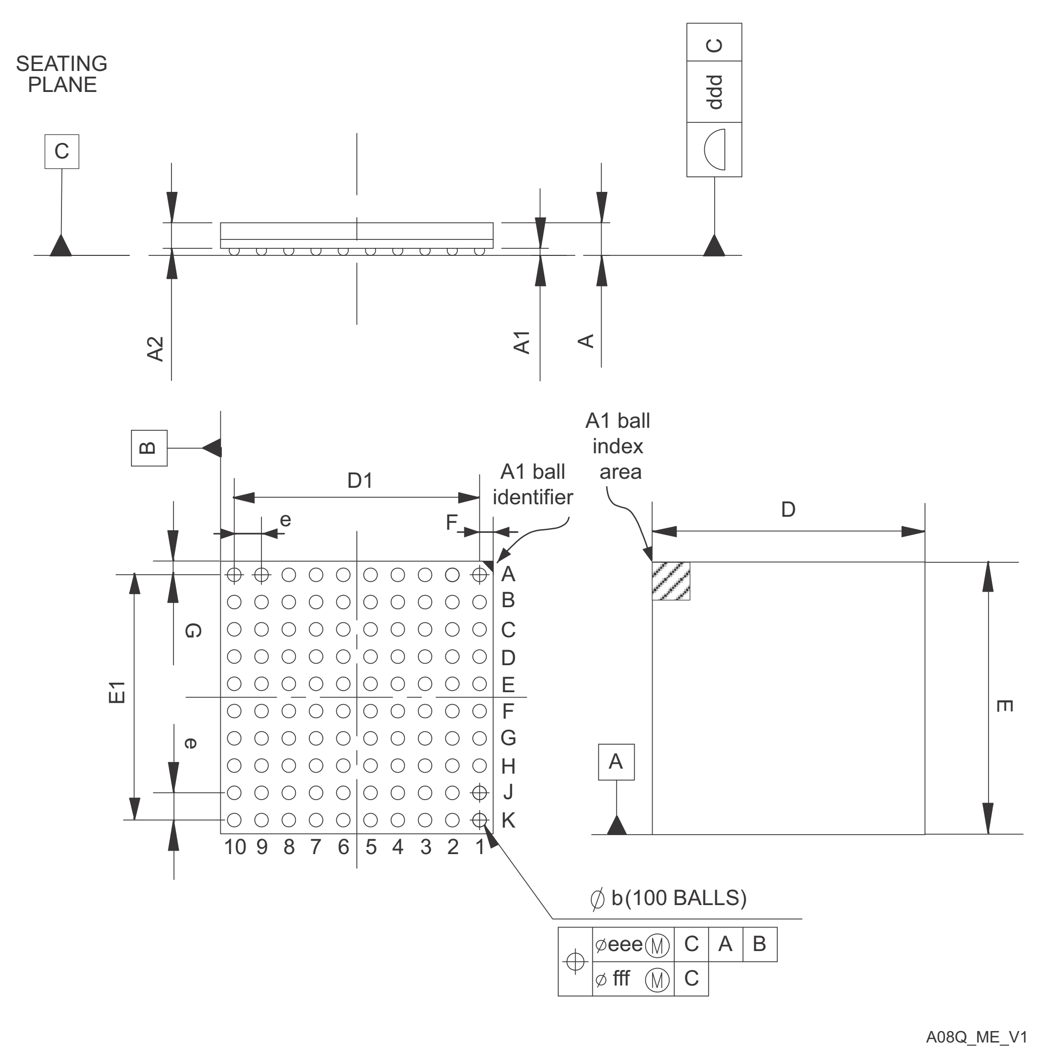
Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 106. Quad-SPI characteristics in SDR mode[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	$2.7\ V \leq V_{DD} < 3.6\ V$ CL=20 pF	-	-	108	MHz
		$1.71\ V < V_{DD} < 3.6\ V$ CL=15 pF	-	-	100	

6.2 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

Figure 82. TFBGA100, 8 × 8 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

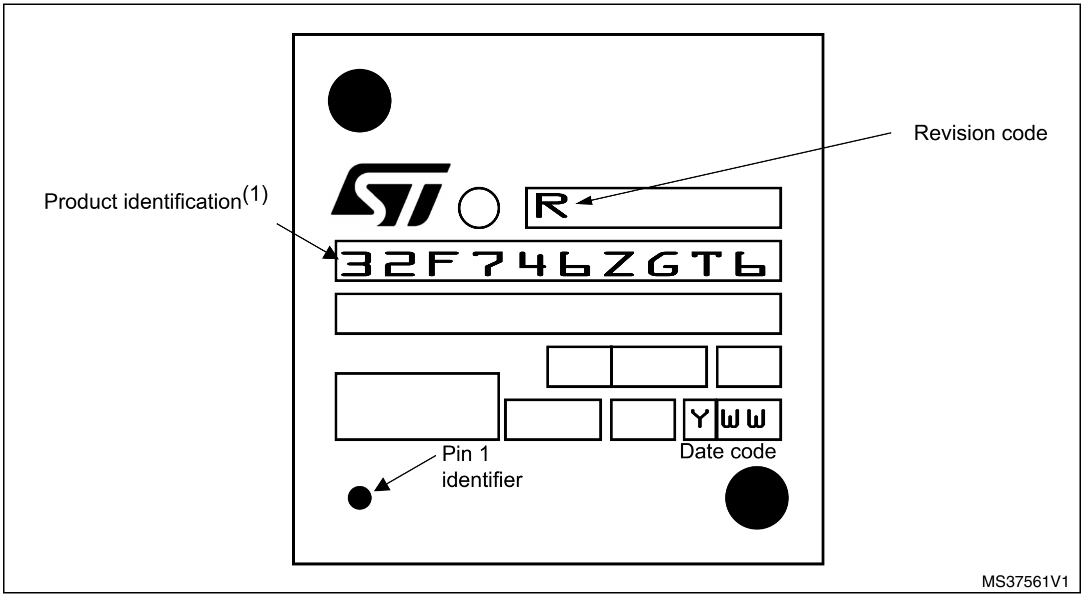
Table 113. TFBGA100, 8 x 8 × 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 90. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 101. TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint

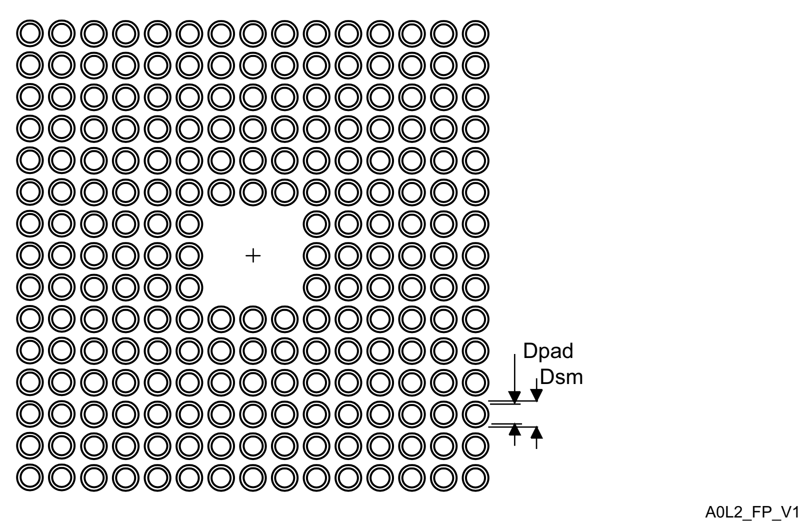


Table 123. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm