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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746igt6

1 Description

The STM32F745xx and STM32F746xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports all ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F745xx and STM32F746xx devices incorporate high-speed embedded memories with a Flash memory up to 1 Mbyte, 320 Kbytes of SRAM (including 64 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control and one low-power timer available in Stop mode, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to four I^2Cs
- Six SPIs, three I^2Ss in duplex mode. To achieve the audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- Two SAI serial audio interfaces
- An SDMMC host interface
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

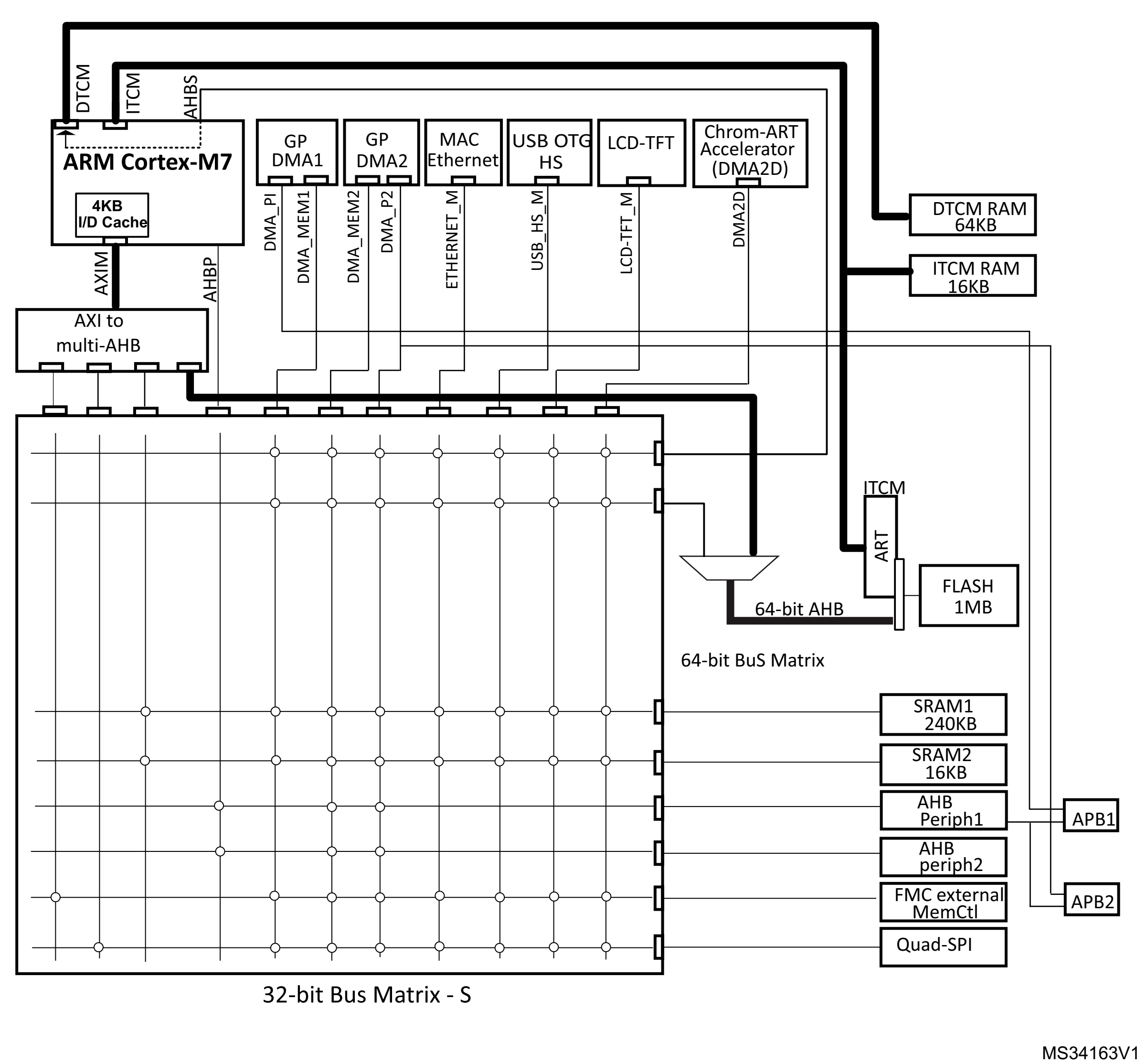
Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F745xx and STM32F746xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F745xx and STM32F746xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) is available on all the packages except LQFP100 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.17.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F745xx and STM32F746xx devices offer devices in 8 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

Figure 3. STM32F745xx and STM32F746xx AXI-AHB bus matrix architecture



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

2.15 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface.

2.16 Power supply schemes

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DD} = 1.7 to 3.6 Vexternal power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

Note: *V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 2.17.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.*

- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6V) for USB transceivers (refer to *Figure 4* and *Figure 5*). For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to V_{DDUSB}. When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear. The following conditions V_{DDUSB} must be respected:
  - During power-on phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
  - During power-down phase ($V_{DD} < V_{DD\_MIN}$), V_{DDUSB} should be always lower than V_{DD}
  - V_{DDSUB} rising and falling time rate specifications must be respected (see *Table 20* and *Table 21*)
  - In operating mode phase, V_{DDUSB} could be lower or higher than $V_{DD:}$

    - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.

    - The V_{DDUSB} supply both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.

    - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

2.24 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds USART. Refer to *Table 8: USART implementation* for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (Max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

features(1)	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.42 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.43 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F74xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
69	D10	D5	102	D15	121	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
70	C10	D4	103	C15	122	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
71	B10	E1	104	B15	123	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	A10	D3	105	A15	124	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	E7	D1	106	F13	125	148	E11	VCAP_2	S	-	-	-	-
74	E5	D2	107	F12	126	149	F10	VSS	S	-	-	-	-
75	F5	C1	108	G13	127	150	F11	VDD	S	-	-	-	-
-	-	-	-	E12	128	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	-	-	E13	129	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	-	-	D13	130	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	-	E14	131	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	-	-	D14	132	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-
PB7	NADV	NADV	-	-

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port B	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	CAN1_TX	-	-	SDMMC1_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI/I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENTOUT
Port C	PC0	-	-	-	-	-	-	-	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENTOUT
	PC1	TRACED0	-	-	-	-	SPI2_MOSI/I2S2_SD	SAI1_SD_A	-	-	-	-	ETH_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENTOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port C	PC4	-	-	-	-	-	I2S1_MCK	-	-	SPDIFRX_IN2	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	SPDIFRX_IN3	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDMMC1_D6	DCMI_D0	LCD_HSYNC	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDMMC1_D7	DCMI_D1	LCD_G6	EVENTOUT
	PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-	-	UART5_RTS	USART6_CK	-	-	-	SDMMC1_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	UART5_CTS	-	QUADSPI_BK1_IO0	-	-	SDMMC1_D1	DCMI_D3	-	EVENTOUT
	PC10	-	-	-	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDMMC1_D2	DCMI_D8	LCD_R2	EVENTOUT
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDMMC1_D3	DCMI_D4	-	EVENTOUT
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	320	mA
$\Sigma\ I_{VSS}$	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	− 320	
$\Sigma\ I_{VDDUSB}$	Total current into V_{DDUSB} power line (source)	25	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	− 100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	− 25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins(2)	− 120	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins (3)	− 5/+0	
	Injected current on TTa pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14: Voltage characteristics* for the values of the maximum allowed input voltage.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

6. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
9. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
10. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 18. Limitations depending on the operating power supply range

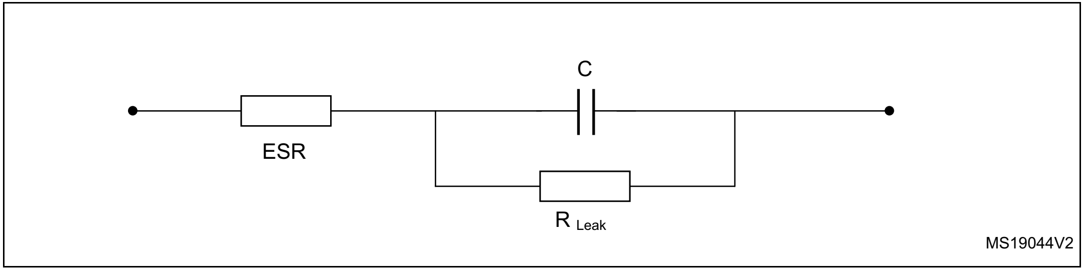
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs Flash memory wait states (1)(2)	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	216 MHz with 9 wait states and over-drive ON	No I/O compensation	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	216 MHz with 8 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V(4)	Conversion time up to 2.4 Msps	30 MHz	216 MHz with 7 wait states and over-drive ON	I/O compensation works	32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.17.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in *Table 19*.

Figure 24. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

1. Guaranteed by design.
2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in *Table 23*. They are sbject to general operating conditions for T_A.

Table 23. Over-drive switching characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tod_swen	Over_drive switch enable time	HSI	-	45	-	µs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
Tod_swdis	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 23: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 34. Switching output I/O current consumption(1) (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 22 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C_{EXT} = 33 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. CINT + $C_{S,}$ PCB board capacitance including the pad pin is estimated to15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

5.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 36* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	13	13	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	µs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
tWUSTDBY (2)	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

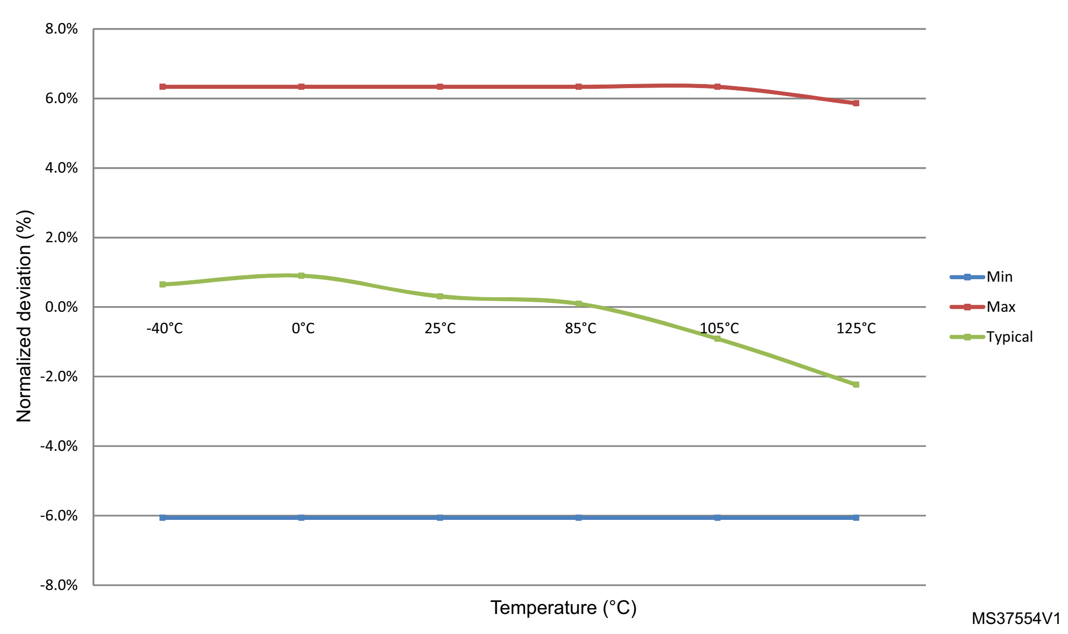
Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics [1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}[2]	Frequency	17	32	47	kHz
$t_{su(LSI)}$[3]	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$[3]	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 35. LSI deviation versus temperature



5.3.11 PLL characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 43. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock[1]	-	0.95[2]	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	216	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	

Table 99. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$2T_{HCLK}-1$	-	ns
$t_{d(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{(CLKH\text{-}NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL\text{-}NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH\text{-}NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL\text{-}Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL\text{-}NBLL)}$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{d(CLKH\text{-}NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+0.5	-	
$t_{su(NWAIT\text{-}CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH\text{-}NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 66 through *Figure 69* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 71. SDRAM write access waveforms

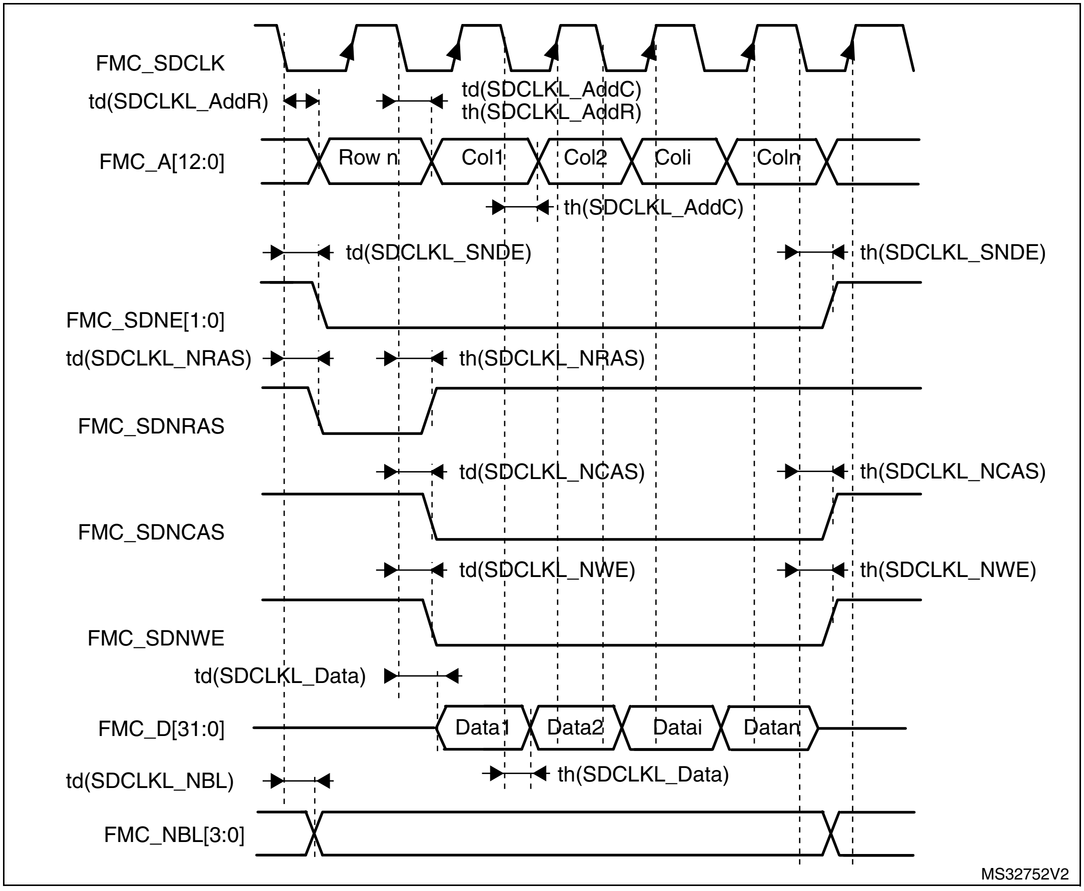
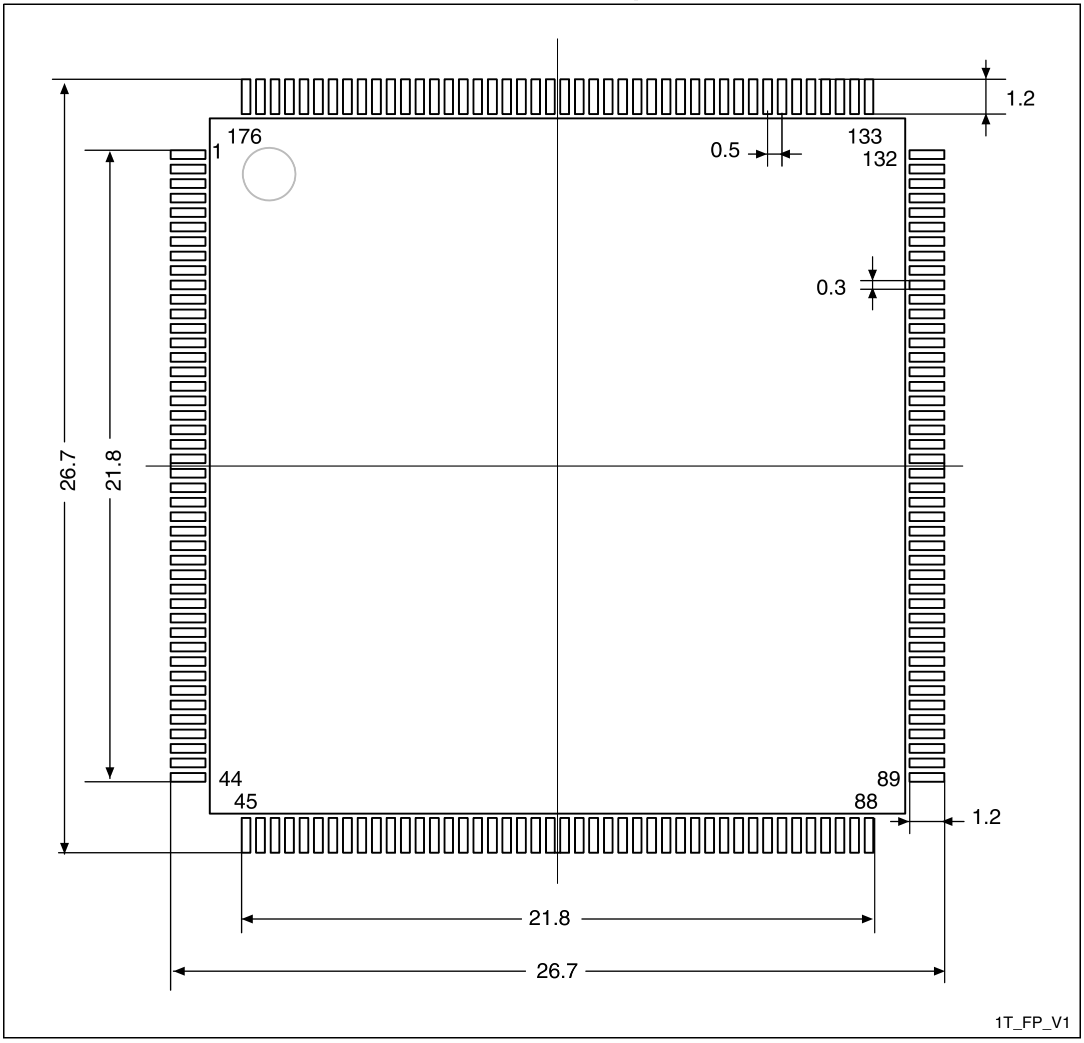


Table 104. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{d(SDCLKL\_Data)}$	Data output valid time	-	2	
$t_{h(SDCLKL\_Data)}$	Data output hold time	0.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	4	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	0.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL-\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

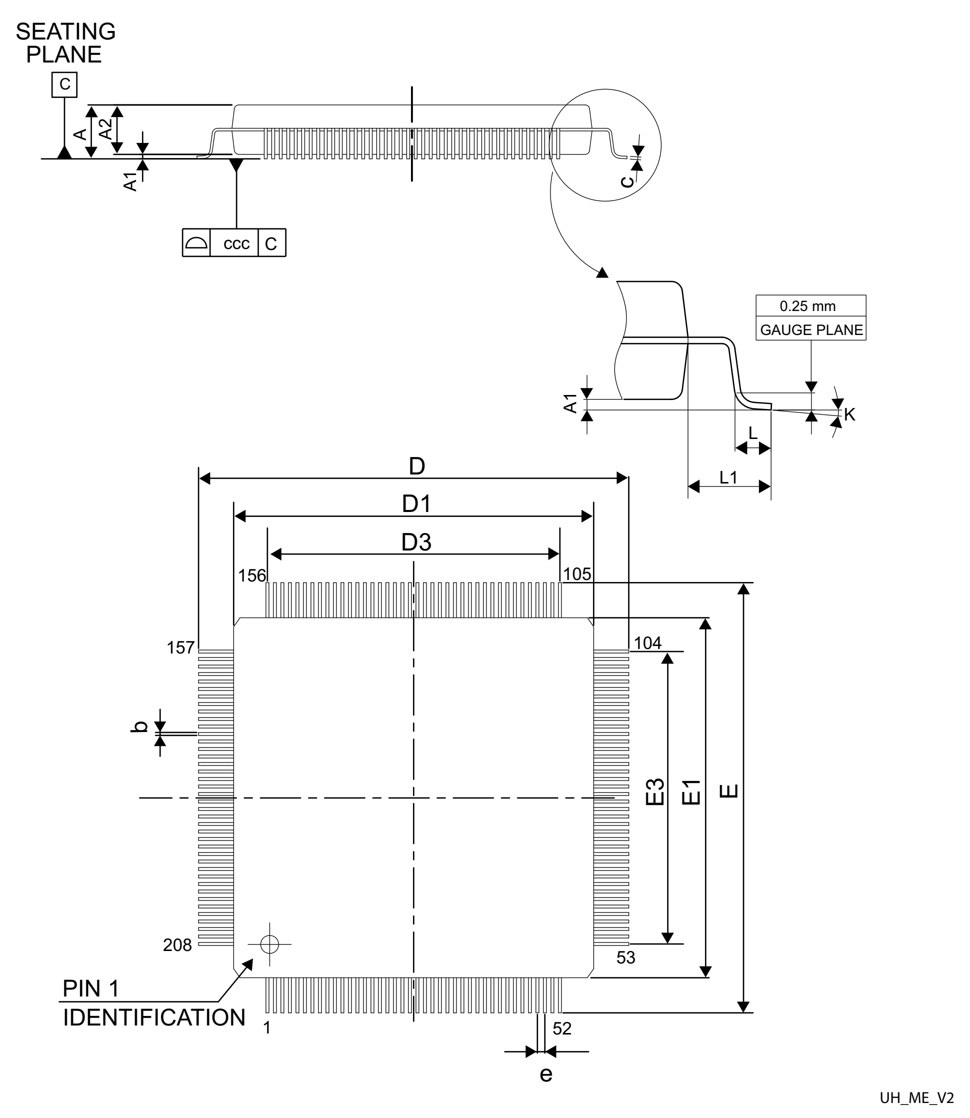
Figure 92. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.6 LQFP208, 28 x 28 mm low-profile quad flat package information

Figure 94. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 119. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571