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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746igt6e

List of figures

These features make the STM32F745xx and STM32F746xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

Figure 2 shows the general block diagram of the device family.

Table 2. STM32F745xx and STM32F746xx features and peripheral counts

Peripherals		STM32F745Vx		STM32F746Vx		STM32F745Zx		STM32F746Zx		STM32F745Ix		STM32F746Ix		STM32F745Bx		STM32F746Bx		STM32F745Nx		STM32F746Nx	
Flash memory in Kbytes		512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024
SRAM in Kbytes	System	320(240+16+64)																			
	Instruction	16																			
	Backup	4																			
FMC memory controller		Yes(1)																			
Ethernet		Yes																			
Timers	General-purpose	10																			
	Advanced-control	2																			
	Basic	2																			
	Low-power	1																			
Random number generator		Yes																			

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	-	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	-	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	K2	M11	37	R2	47	50	R2	PA3	I/O	FT	(4)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
26	J1	-	38	-	-	51	K6	VSS	S	-	-	-	-
-	E6	N11	-	L4	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	K1	J8	39	K4	49	52	K5	VDD	S	-	-	-	-
28	G3	M10	40	N4	50	53	N4	PA4	I/O	TTa	(4)	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
29	H3	M9	41	P4	51	54	P4	PA5	I/O	TTa	(4)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
30	J3	N10	42	P3	52	55	P3	PA6	I/O	FT	(4)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 11. FMC pin definition (continued)

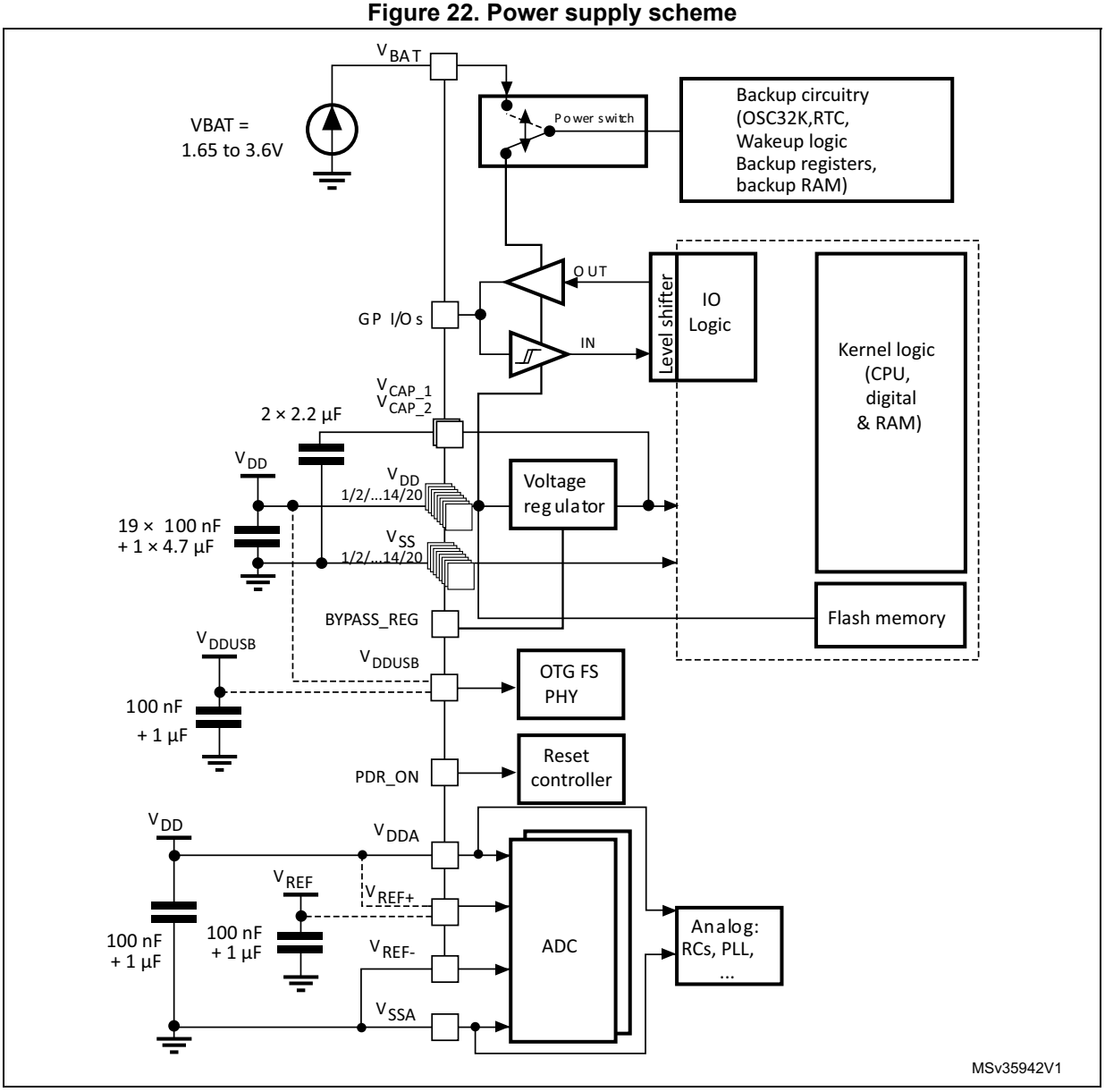
Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF6	-	-	-	-
PF7	-	-	-	-
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port H	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT

5.1.6 Power supply scheme

Figure 22. Power supply scheme



1. To connect BYPASS_REG and PDR_ON pins, refer to *Section 2.17: Power supply supervisor* and *Section 2.18: Voltage regulator*
2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins[7]	Max frequency 144 MHz	1.10	1.14	1.20	
		Max frequency 168MHz	1.20	1.26	1.32	
		Max frequency 180 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST and FT pins[8]	2 V ≤V_{DD} ≤3.6 V	− 0.3	-	5.5	
		V_{DD} ≤2 V	− 0.3	-	5.2	
	Input voltage on TTa pins	-	− 0.3	-	V_{DDA}+ 0.3	
	Input voltage on BOOT pin	-	0	-	9	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7[9]	LQFP100	-	-	465	mW
		TFBGA100	-	-	351	
		WLCSP143	-	-	641	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40	-	85	°C
		Low power dissipation[10]	− 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40	-	105	°C
		Low power dissipation[10]	− 40	-	125	
T_J	Junction temperature range	6 suffix version	− 40	-	105	°C
		7 suffix version	− 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. 216 MHz maximum frequency for 6 suffix version (200 MHz maximum frequency for 7 suffix version).
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.17.2: Internal reset OFF*).
4. When the ADC is used, refer to *Table 62: ADC characteristics*.
5. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V ≤ V_{DD} ≤ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	178	208(4)	230(4)	-	mA
			200	165	193	212	230	
			180	147	171(4)	185(4)	198(4)	
			168	130	152	164	177	
			144	100	116	127	137	
			60	44	52	63	73	
			25	21	25	36	46	
		All peripherals disabled(3)	216	102	120(4)	141(4)	-	
			200	95	111	131	149	
			180	84	98(4)	112(4)	125(4)	
			168	75	87	100	112	
			144	58	67	77	88	
			60	25	30	41	51	
			25	12	15	25	36	

1. Guaranteed by characterization results.

Table 34. Switching output I/O current consumption(1) (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 22 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.1	mA
			8	1.0	0.5	
			25	3.5	1.6	
			50	5.9	4.2	
			60	10.0	4.4	
			84	19.12	5.8	
			90	19.6	-	
		C_{EXT} = 33 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.3	0.2	
			8	1.3	0.7	
			25	3.5	2.3	
			50	10.26	5.19	
			60	16.53	-	

1. CINT + C_S, PCB board capacitance including the pad pin is estimated to15 pF.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART/L1-cache is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 54 MHz)	TIM2	19.8	18.7	16.1	µA/MHz
	TIM3	16.6	15.1	13.6	
	TIM4	16.2	15.1	13.3	
	TIM5	19	17.8	15.8	
	TIM6	3	2.7	2.5	
	TIM7	3	2.7	2.5	
	TIM12	12.4	11.3	10.3	
	TIM13	6	5.3	5	
	TIM14	6	5.3	5	
	LPTIM1	9.4	8.7	8.1	
	WWDG	1.8	1.6	1.4	
	SPI2/I2S2(3)	3	2.9	2.8	
	SPI3/I2S3(3)	3.2	2.9	2.8	
	SPDIFRX	2.2	2	1.7	
	USART2	12.8	12	10.8	
	USART3	15.6	14.2	13.1	
	UART4	11.8	10.7	9.7	
	UART5	11.2	10	9.2	
	I2C1	9.8	8.7	7.8	
	I2C2	8.6	7.8	7.2	
	I2C3	8.6	7.8	7.2	
	I2C4	12	10.9	9.7	
	CAN1	6.8	6	5.6	
	CAN2	6.8	6	5.8	
	CEC	1	0.7	0.8	
	PWR	1.2	0.9	0.8	
	DAC(4)	3	2.7	2.5	
	UART7	12.4	11.6	10	
	UART8	10.4	9.3	8.6	

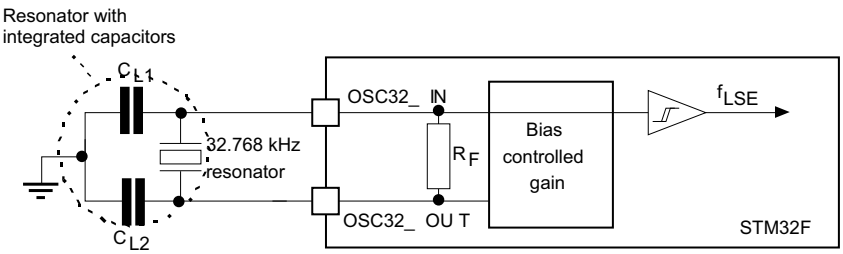
Table 40. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 33. Typical application with a 32.768 kHz crystal



5.3.15 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Table 53. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD S5.3.1-2009, LQFP100, LQFP144, LQFP176, LQFP208, WLCSP143, UFBGA176, TFBGA100 and TFBGA216 packages	C3	250	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 54. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

Table 56. I/O static characteristics (continued)

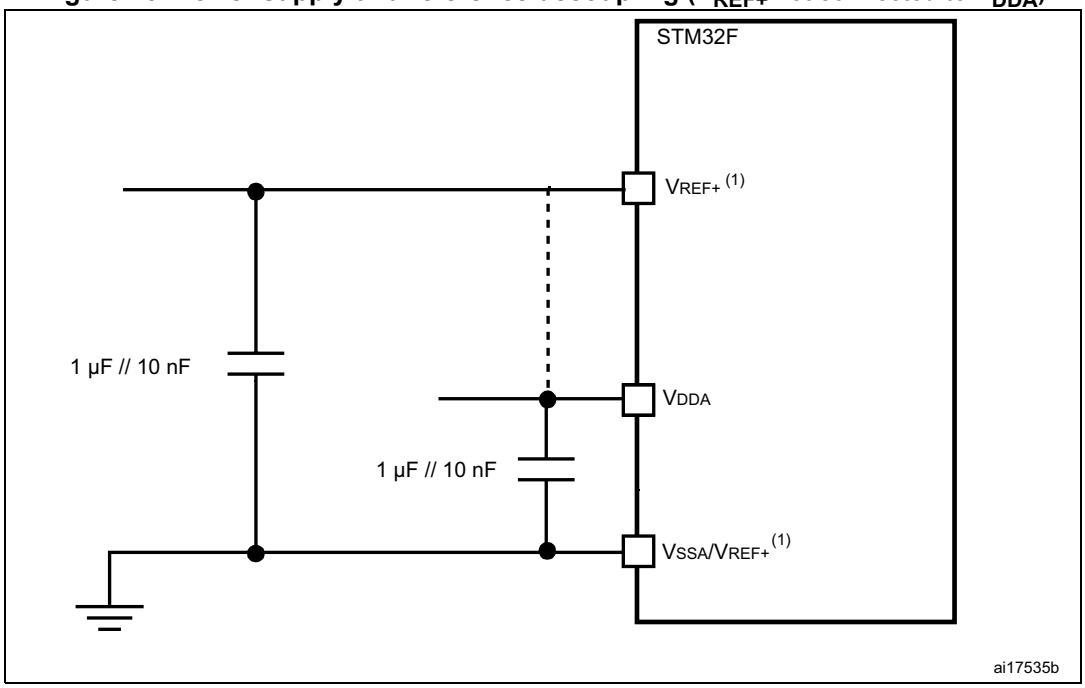
Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)		1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1)	-	-	V
				$0.7V_{DD}$(2)			
	BOOT I/O input high level voltage		1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	$10\%V_{DD}$(3)	-	-	V
	BOOT I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	0.1	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 55: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 55: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).

General PCB design guidelines

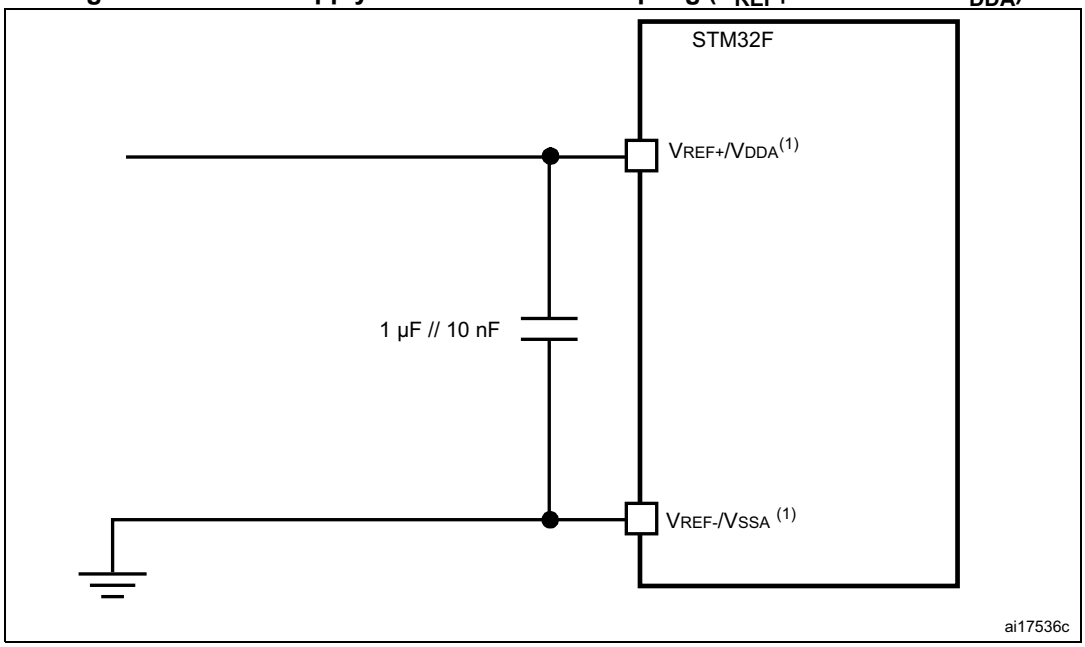
Power supply decoupling should be performed as shown in *Figure 43* or *Figure 44*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 43. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all the packages except TFBGA100 whereas the V_{REF-} is available only on UFBGA176 and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 44. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all the packages except TFBGA100, whereas the V_{REF-} is available only on UFBGA176 and TFBGA216. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 77. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	ns
		Slave mode PCM short pulse mode(3)	3	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
		Slave mode PCM short pulse mode(3)	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD\_SR)}$		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3.5	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. The maximum value of 256xFs is 45 MHz (APB1 maximum frequency).
3. Measurement done with respect to I2S_CK rising edge.

Note: Refer to RM0385 reference manual I2S section for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Table 83. USB HS clock timing parameters(1)

Symbol	Parameter		Min	Typ	Max	Unit
-	f_{HCLK} value to guarantee proper operation of USB HS interface		30	-	-	MHz
F_{START_8BIT}	Frequency (first transition)	8-bit ±10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm		59.97	60	60.03	MHz
D_{START_8BIT}	Duty cycle (first transition)	8-bit ±10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm		49.975	50	50.025	%
t_{STEADY}	Time to reach the steady state frequency and duty cycle after the first transition		-	-	1.4	ms
t_{START_DEV}	Clock startup time after the de-assertion of SuspendM	Peripheral	-	-	5.6	ms
t_{START_HOST}		Host	-	-	-	
t_{PREP}	PHY preparation time after the first transition of the input clock		-	-	-	µs

1. Guaranteed by design.

Figure 54. ULPI timing diagram

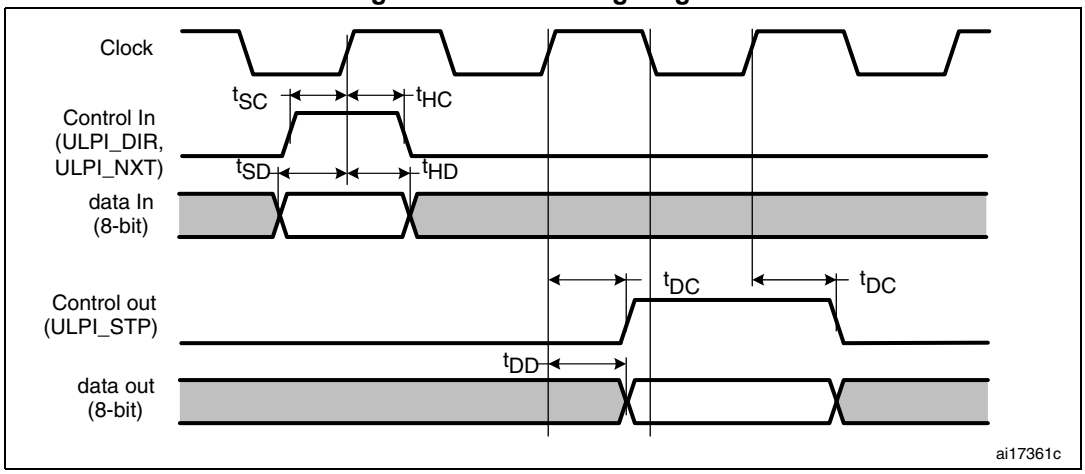


Table 102. SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3.5	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	4	
$t_{d(SDCLKL-SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 103. LPSDR SDRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{W(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH\_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL\_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\_SDNRAS}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0	-	

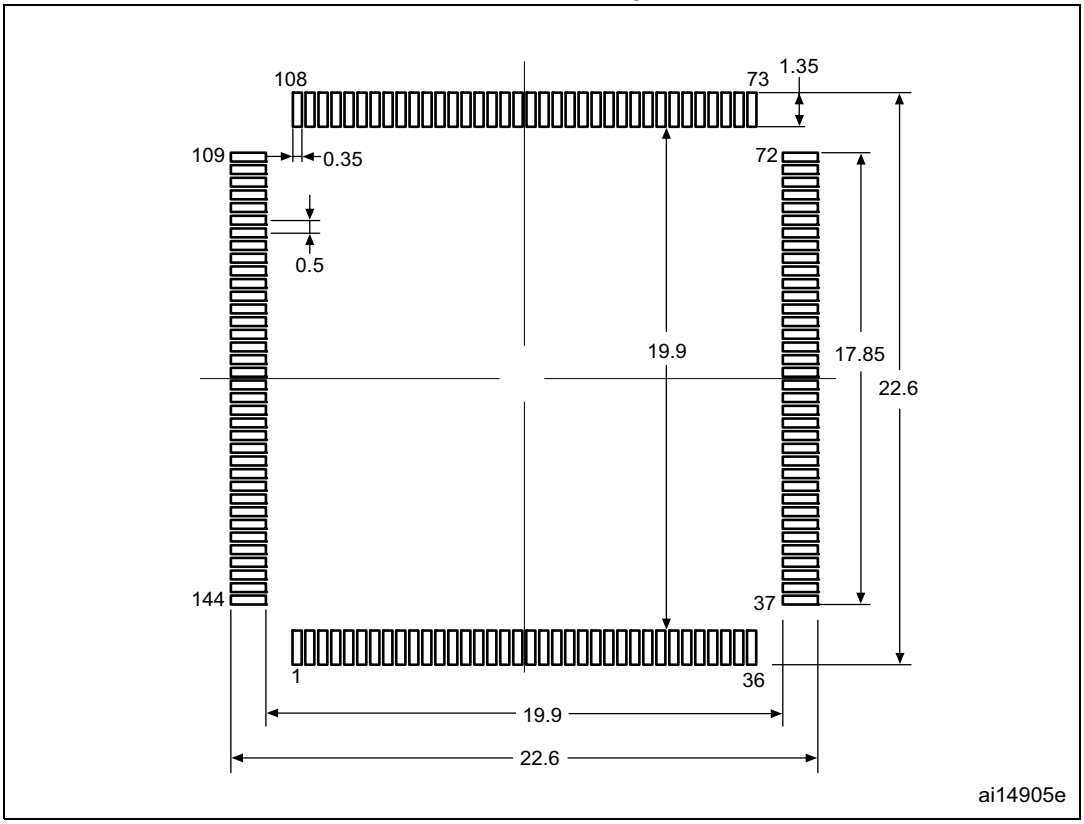
1. Guaranteed by characterization results.

Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 89. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.