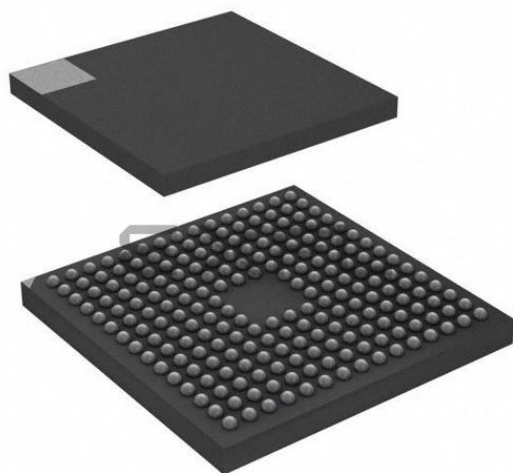




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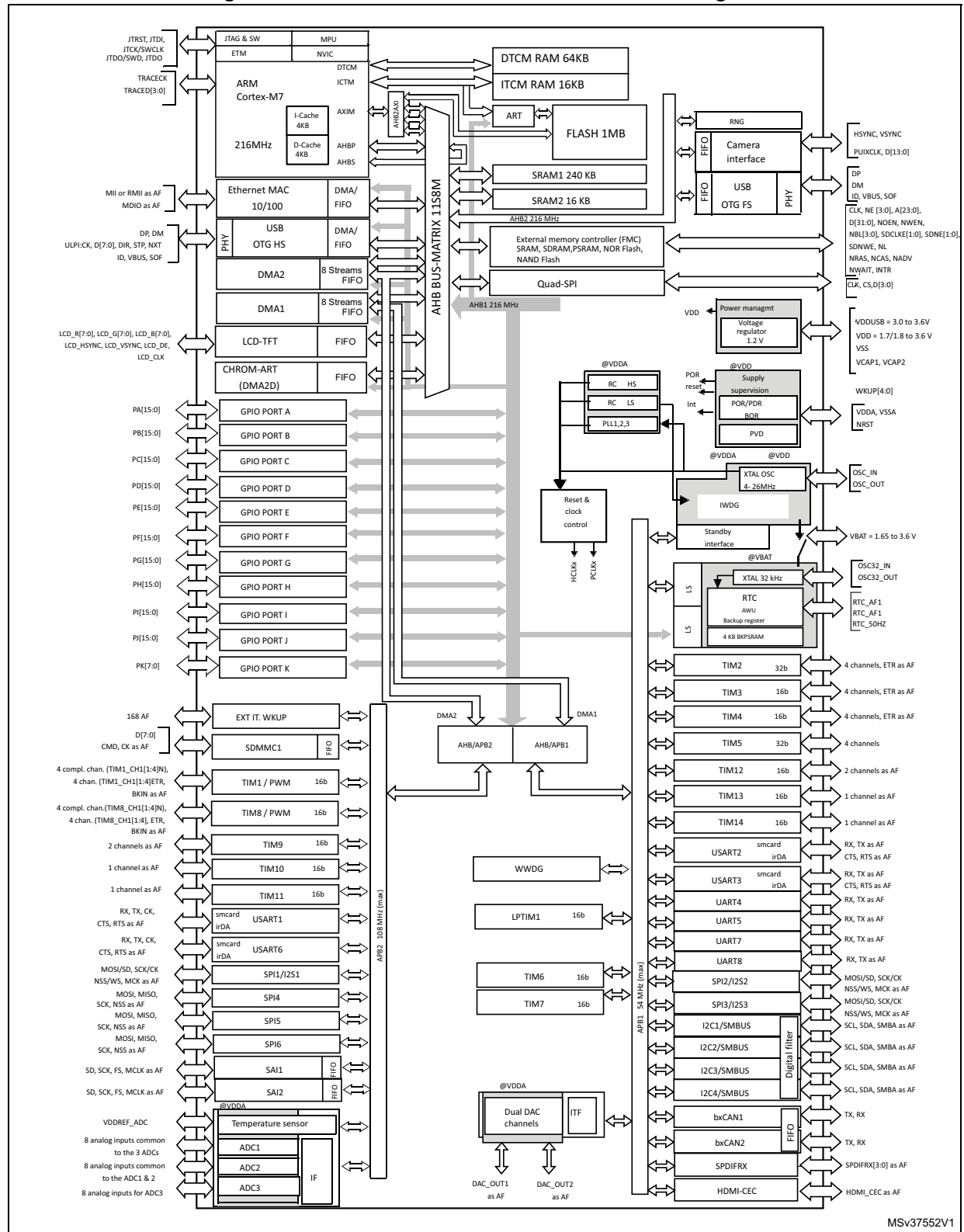
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Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746neh6

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Figure 2. STM32F745xx and STM32F746xx block diagram



MSV37552V1

1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and a low-power consumption, while delivering an outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (4 Kbytes of I-cache and 4 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up the software development by using metalanguage development tools, while avoiding saturation.

[Figure 2](#) shows the general block diagram of the STM32F745xx and STM32F746xx devices.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.18.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP100	Yes	No	Yes	No
LQFP144, LQFP208			Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
TFBGA100, LQFP176, WLCSP143, UFBGA176, TFBGA216	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

2.19 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

2.24 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds USART. Refer to [Table 8: USART implementation](#) for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (Max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

features ⁽¹⁾	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	83	-	102	114	J10	VSS	S	-	-	-	-
-	-	L1	84	J13	103	115	J11	VDD	S	-	-	-	-
61	H8	J2	85	M14	104	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	G8	K1	86	L14	105	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	-	-	118	K12	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	J12	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-
-	-	-	-	-	-	120	H12	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	J13	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	-	-	122	H13	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	G12	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	H11	VDD	S	-	-	-	-
-	-	-	-	-	-	125	H10	VSS	S	-	-	-	-
-	-	-	-	-	-	126	G13	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	F12	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	F13	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	-	J1	87	L15	106	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	-	G3	88	K15	107	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	-	G5	89	K14	108	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	G6	90	K13	109	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	G4	91	J15	110	133	J15	PG6	I/O	FT	-	DCMI_D12, LCD_R7, EVENTOUT	-
-	-	H1	92	J14	111	134	J14	PG7	I/O	FT	-	USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-



Table 12. STM32F745xx and STM32F746xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port A	PA0	-	TIM2_C H1/TIM2 _ETR	TIM5_C H1	TIM8_ET R	-	-	-	USART2 _CTS	UART4_ TX	-	SAI2_SD_ B	ETH_MII_ CRS	-	-	-	EVEN TOUT
	PA1	-	TIM2_C H2	TIM5_C H2	-	-	-	-	USART2 _RTS	UART4_ RX	QUADSP I_BK1_IO 3	SAI2_MC K_B	ETH_MII_ RX_CLK/ ETH_RMI I_REF_C LK	-	-	LCD_R2	EVEN TOUT
	PA2	-	TIM2_C H3	TIM5_C H3	TIM9_CH 1	-	-	-	USART2 _TX	SAI2_SC K_B	-	-	ETH_MDI O	-	-	LCD_R1	EVEN TOUT
	PA3	-	TIM2_C H4	TIM5_C H4	TIM9_CH 2	-	-	-	USART2 _RX	-	-	OTG_HS_ ULPI_D0	ETH_MII_ COL	-	-	LCD_B5	EVEN TOUT
	PA4	-	-	-	-	-	SPI1_NS S/I2S1_ WS	SPI3_NS S/I2S3_ WS	USART2 _CK	-	-	-	-	OTG_HS_ _SOF	DCMI_H SYNC	LCD_VS YNC	EVEN TOUT
	PA5	-	TIM2_C H1/TIM2 _ETR	-	TIM8_CH 1N	-	SPI1_SC K/I2S1_ CK	-	-	-	-	OTG_HS_ ULPI_CK	-	-	-	LCD_R4	EVEN TOUT
	PA6	-	TIM1_B KIN	TIM3_C H1	TIM8_BKI N	-	SPI1_MI SO	-	-	-	TIM13_C H1	-	-	-	DCMI_PI XCLK	LCD_G2	EVEN TOUT
	PA7	-	TIM1_C H1N	TIM3_C H2	TIM8_CH 1N	-	SPI1_M OSI/I2S1 _SD	-	-	-	TIM14_C H1	-	ETH_MII_ RX_DV/E TH_RMII_ CRS_DV	FMC_SD NWE	-	-	EVEN TOUT
	PA8	MCO1	TIM1_C H1	-	TIM8_BKI N2	I2C3_SC L	-	-	USART1 _CK	-	-	OTG_FS_ SOF	-	-	-	LCD_R6	EVEN TOUT
	PA9	-	TIM1_C H2	-	-	I2C3_SM BA	SPI2_SC K/I2S2_ CK	-	USART1 _TX	-	-	-	-	-	DCMI_D 0	-	EVEN TOUT
	PA10	-	TIM1_C H3	-	-	-	-	-	USART1 _RX	-	-	OTG_FS_ ID	-	-	DCMI_D 1	-	EVEN TOUT
	PA11	-	TIM1_C H4	-	-	-	-	-	USART1 _CTS	-	CAN1_R X	OTG_FS_ DM	-	-	-	LCD_R4	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SPI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVEN TOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	-	UART4_RTS	-	-	-	-	-	-	EVEN TOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVEN TOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVEN TOUT
	PB2	-	-	-	-	-	-	SAI1_SDA	SPI3_MOSI/I2S3_SD	-	QUADSPI_CLK	-	-	-	-	-	EVEN TOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	EVEN TOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-	EVEN TOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SD_CKE1	DCMI_D10	-	EVEN TOUT
	PB6	-	-	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	-	FMC_SD_NE1	DCMI_D5	-	EVEN TOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVEN TOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVEN TOUT

Table 13. STM32F745xx and STM32F746xx register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M7	0xE000 0000 - 0xE00F FFFF	Cortex-M7 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	Quad-SPI control register
	0xA000 0000 - 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00 - 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 0400 - 0x5006 07FF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000 - 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

Table 35. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 54 MHz)	TIM2	19.8	18.7	16.1	μA/MHz
	TIM3	16.6	15.1	13.6	
	TIM4	16.2	15.1	13.3	
	TIM5	19	17.8	15.8	
	TIM6	3	2.7	2.5	
	TIM7	3	2.7	2.5	
	TIM12	12.4	11.3	10.3	
	TIM13	6	5.3	5	
	TIM14	6	5.3	5	
	LPTIM1	9.4	8.7	8.1	
	WWDG	1.8	1.6	1.4	
	SPI2/I2S2 ⁽³⁾	3	2.9	2.8	
	SPI3/I2S3 ⁽³⁾	3.2	2.9	2.8	
	SPDIFRX	2.2	2	1.7	
	USART2	12.8	12	10.8	
	USART3	15.6	14.2	13.1	
	UART4	11.8	10.7	9.7	
	UART5	11.2	10	9.2	
	I2C1	9.8	8.7	7.8	
	I2C2	8.6	7.8	7.2	
	I2C3	8.6	7.8	7.2	
	I2C4	12	10.9	9.7	
	CAN1	6.8	6	5.6	
	CAN2	6.8	6	5.8	
	CEC	1	0.7	0.8	
	PWR	1.2	0.9	0.8	
	DAC ⁽⁴⁾	3	2.7	2.5	
	UART7	12.4	11.6	10	
	UART8	10.4	9.3	8.6	

5.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 36](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3$ V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	13	13	CPU clock cycles
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	μs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
$t_{WUSTDBY}^{(2)}$	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.

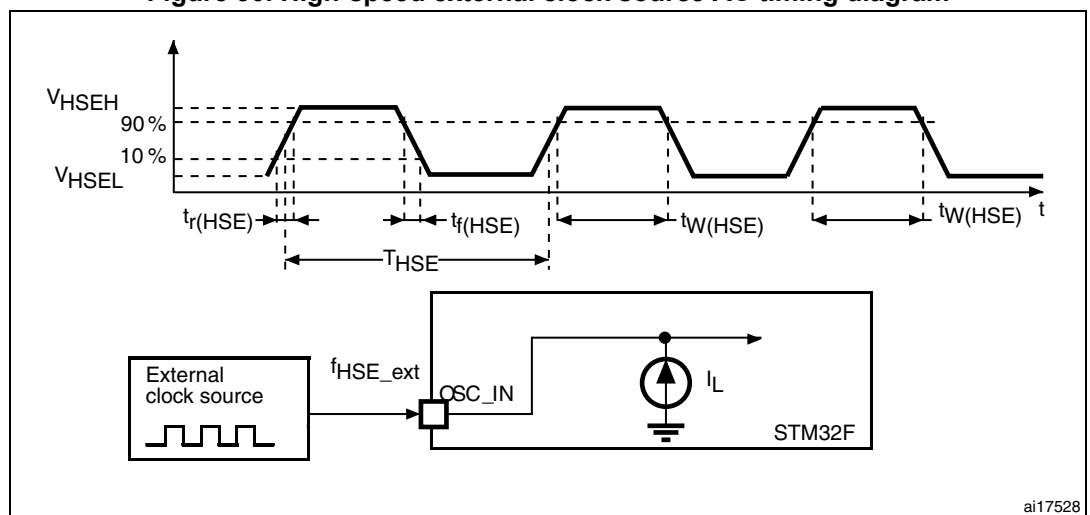
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 38. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency ⁽¹⁾	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time ⁽¹⁾		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance ⁽¹⁾	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 30. High-speed external clock source AC timing diagram



ai17528

Table 62. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VREF+}^{(2)}$	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	μA
$I_{VDDA}^{(2)}$	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

- V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 2.17.2: Internal reset OFF](#)).
- Guaranteed by characterization results.
- V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
- R_{ADC} maximum value is given for $V_{DD}=1.7$ V, and minimum value for $V_{DD}=3.3$ V.
- For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 62](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. $N = 12$ (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 63. ADC static accuracy at $f_{ADC} = 18$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to 3.6 V $V_{REF} = 1.7$ to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	± 3	± 4	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 1	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 2	± 3	

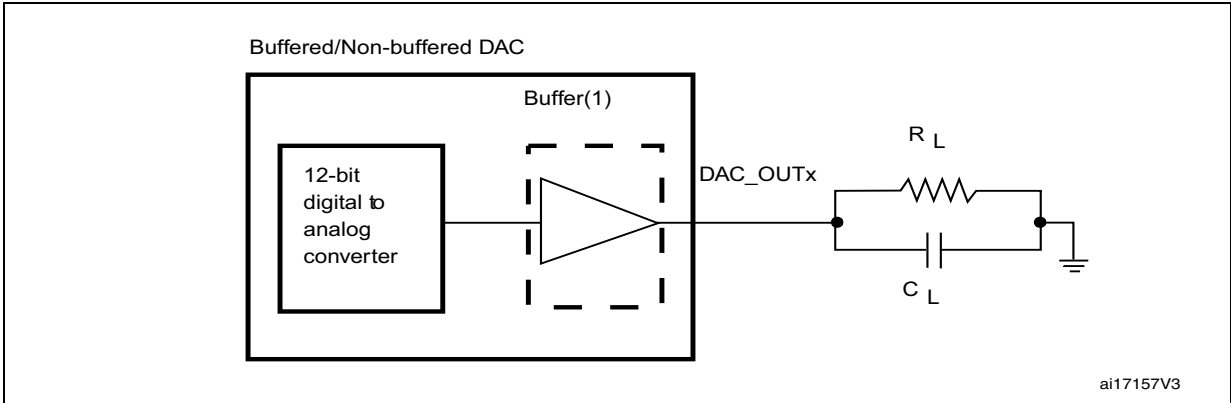
- Guaranteed by characterization results.

Table 64. ADC static accuracy at $f_{ADC} = 30$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 30$ MHz, $R_{AIN} < 10$ k Ω , $V_{DDA} = 2.4$ to 3.6 V, $V_{REF} = 1.7$ to 3.6 V, $V_{DDA} - V_{REF} < 1.2$ V	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 4	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

- Guaranteed by characterization results.

Figure 45. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0385 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 74. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog Filtre ON DNF=0	10	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	22.5	
			Analog Filtre OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

Figure 47. SPI timing diagram - slave mode and CPHA = 1

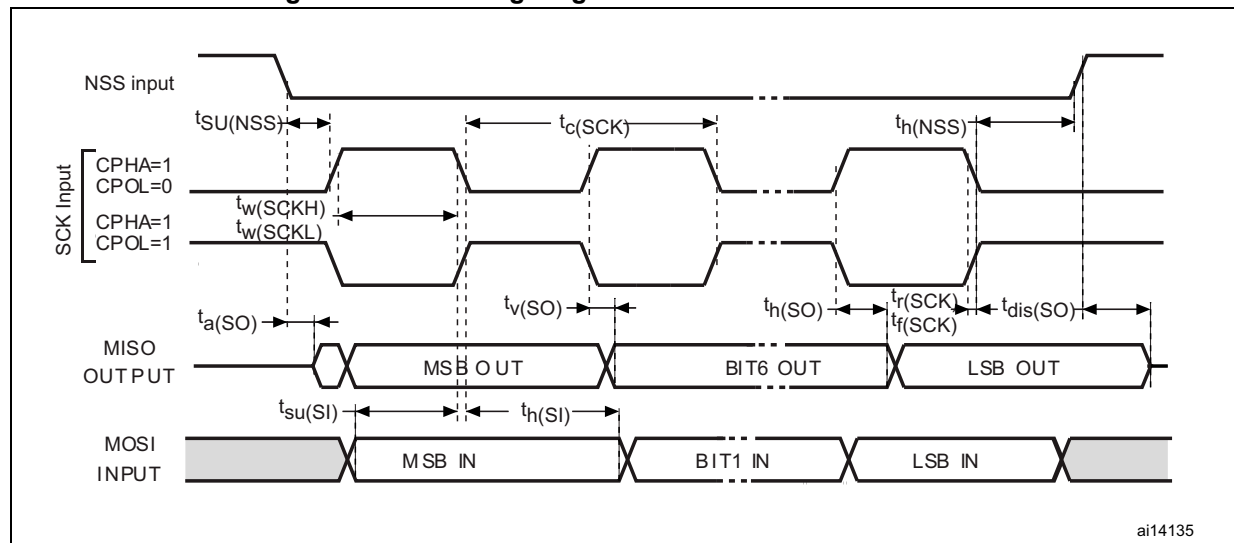
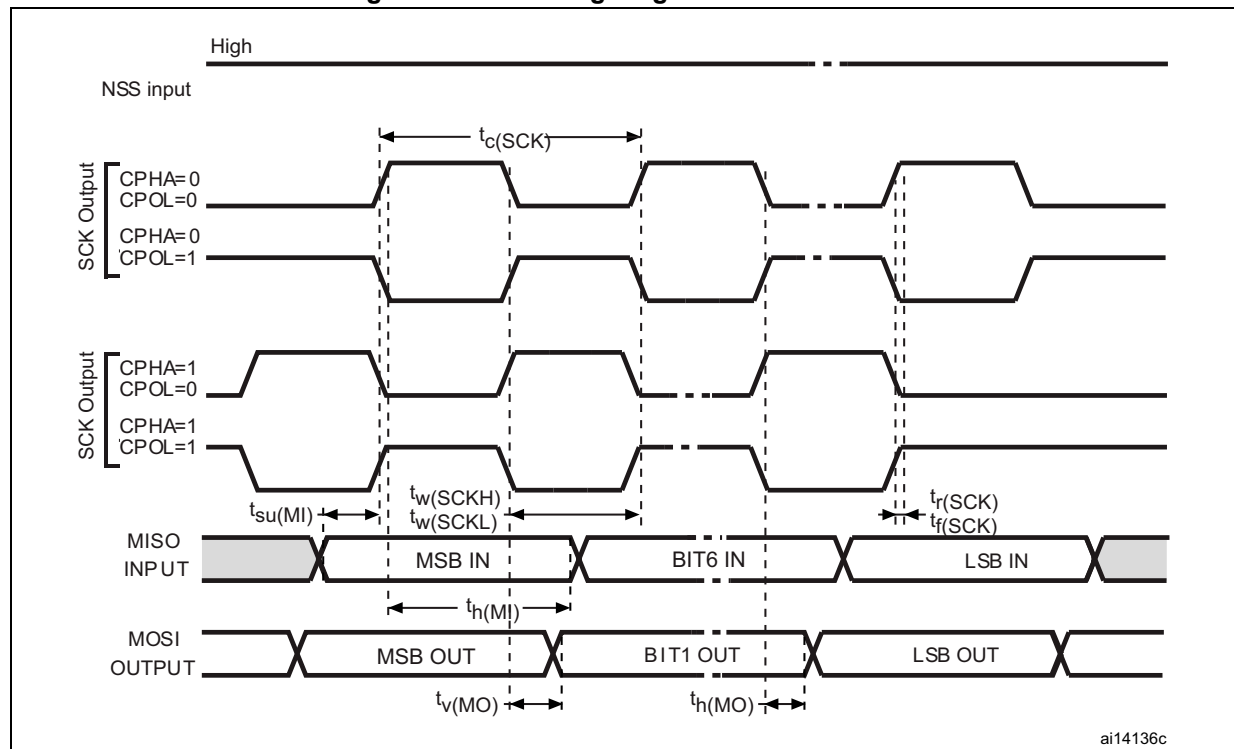


Figure 48. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 77](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

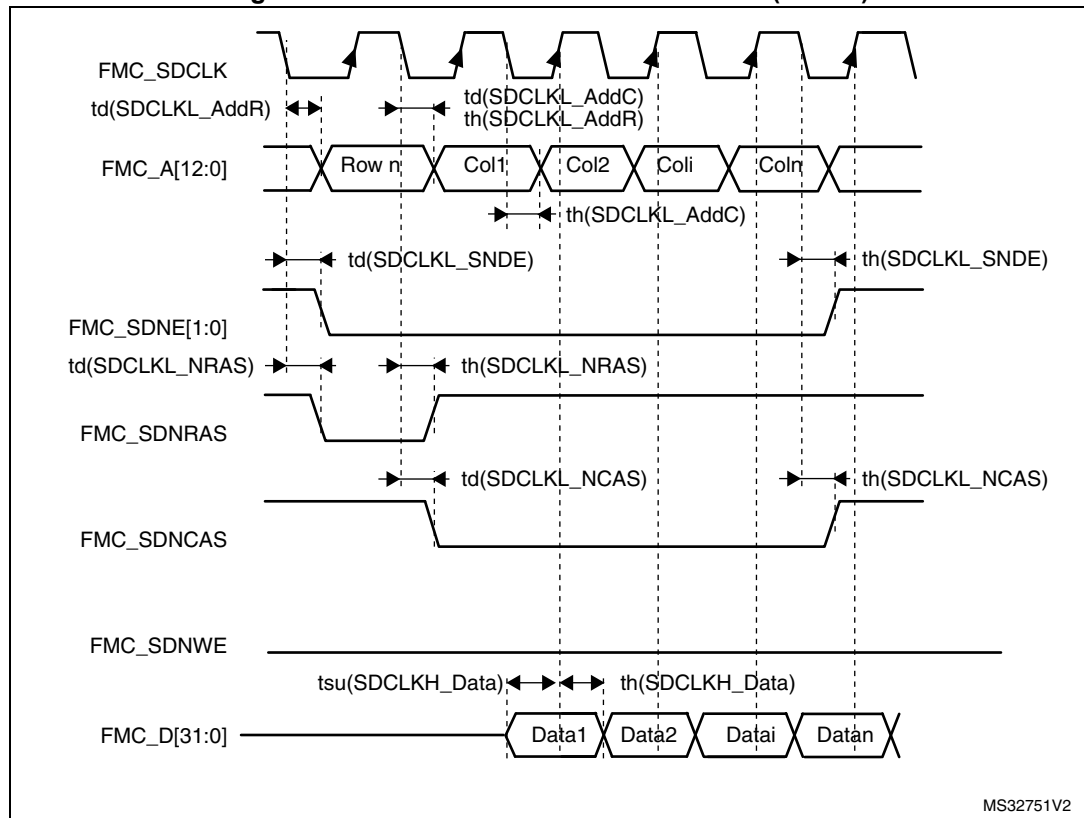
- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

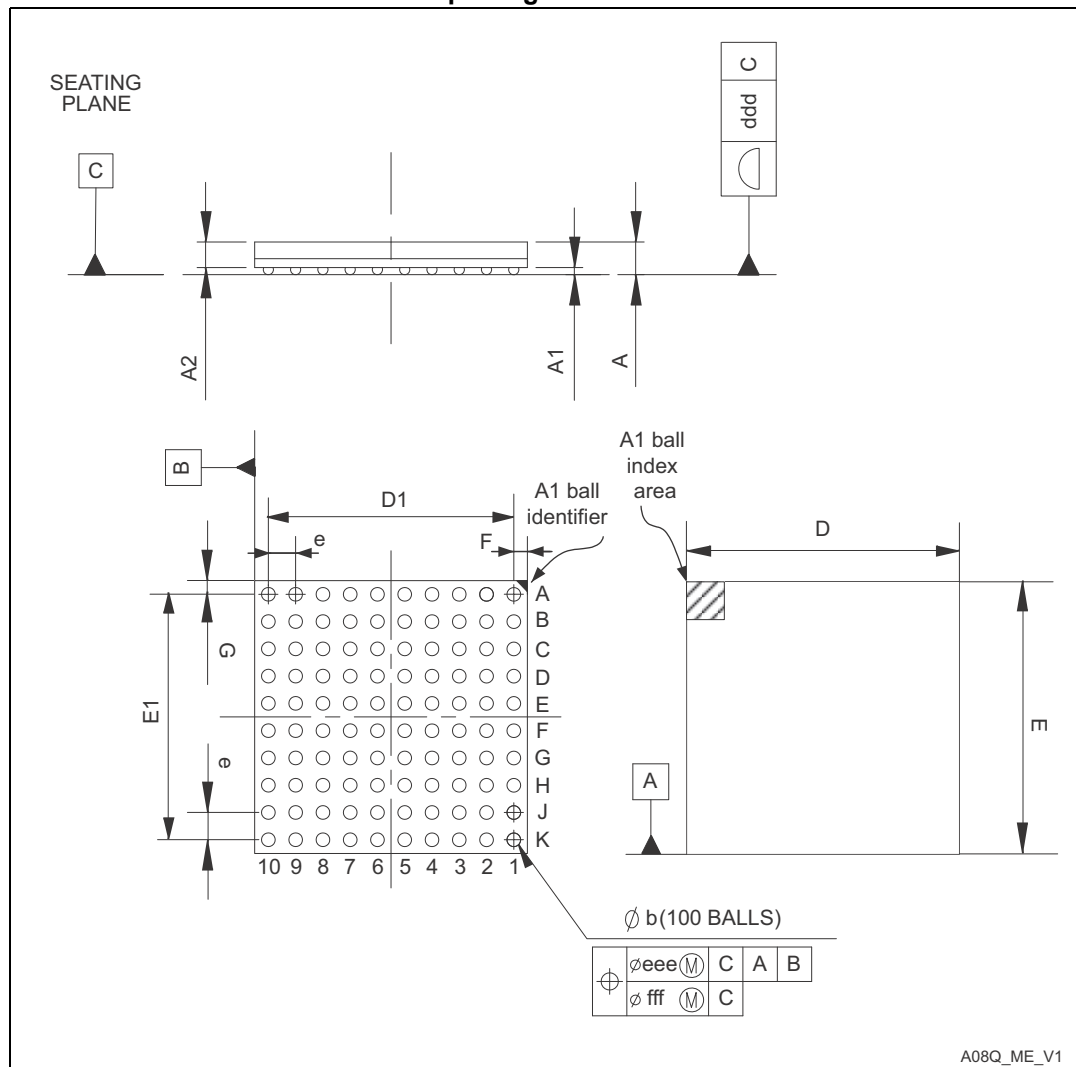
In all timing tables, the T_{HCLK} is the HCLK clock period.

- For $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, maximum FMC_SDCLK = 100 MHz at CL=20 pF (on FMC_SDCLK).
- For $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For $1.71\text{ V} \leq V_{DD} < 1.9\text{ V}$, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 70. SDRAM read access waveforms (CL = 1)

6.2 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

Figure 82. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package outline



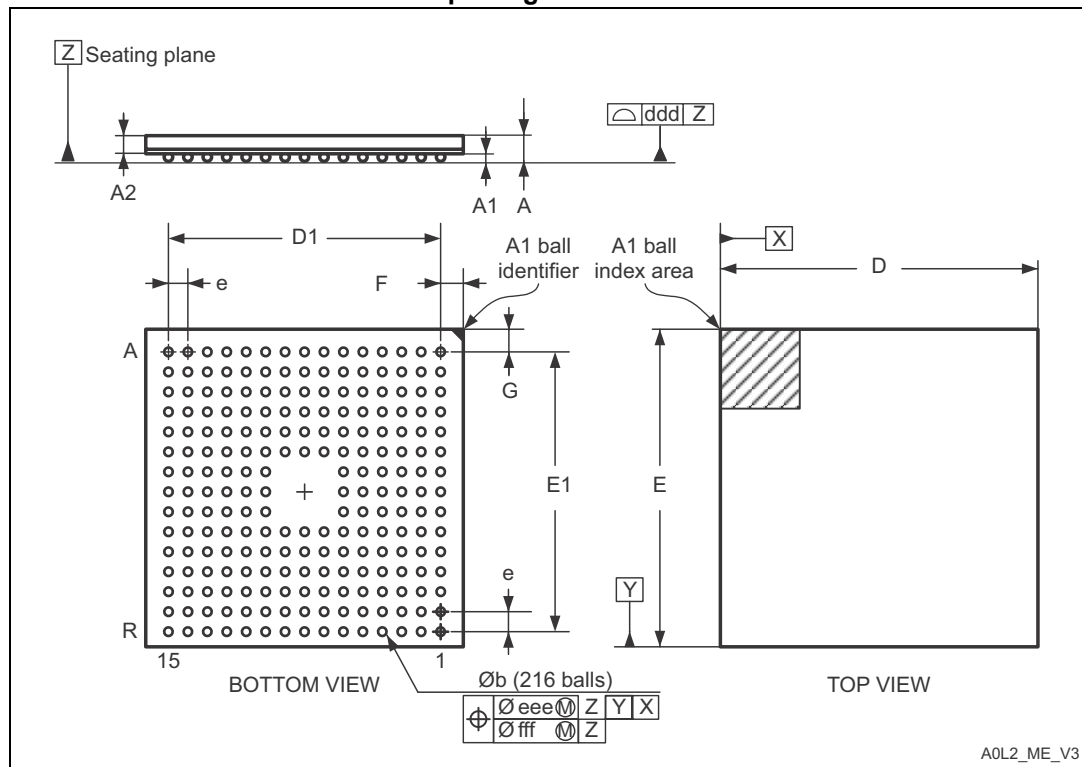
1. Drawing is not to scale.

Table 113. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177

6.8 TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package information

Figure 100. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-

Table 127. Document revision history (continued)

Date	Revision	Changes
10-Dec-2015	3	Updated Table 10: STM32F745xx and STM32F746xx pin and ball definition additional functions column: WKUP1, 2, 3, 4, 5, 6 must be respectively PA0, PA2, PC1, PC13, PI8, PI11. Updated Table 62: ADC characteristics adding V_{REF-} negative voltage reference. Update Table 14: Voltage characteristics adding table note 3. Updated Table 69: Temperature sensor calibration values memory addresses. Updated Table 72: Internal reference voltage calibration values memory addresses.
18-Feb-2016	4	Updated Table 52: EMI characteristics modifying 25/180 MHz by 25/200 MHz. Updated Figure 13: STM32F74xZx WLCSP143 ballout. Added TFBGA100 8 x 8 mm package: – Updated Cover page. – Updated Section 1: Description. – Updated Table 2: STM32F745xx and STM32F746xx features and peripheral counts. – Updated Table 4: Regulator ON/OFF and internal reset ON/OFF availability. – Updated Section 3: Pinouts and pin description adding Figure 12: STM32F74xVx TFBGA100 ballout and adding TFBGA100 ball description in Table 10: STM32F745xx and STM32F746xx pin and ball definition. – Updated Table 17: General operating conditions. – Updated Table 53: ESD absolute maximum ratings. – Updated notes below Figure 43 and Figure 44. – Updated Section 6: Package information adding TFBGA100 package information and adding thermal resistance in Table 124: Package thermal characteristics. – Updated Table 10: STM32F745xx and STM32F746xx pin and ball definition note 5. Updated Table 35: Peripheral current consumption peripheral consumption on APB1 and APB2. Updated Figure 18: STM32F74xNx TFBGA216 ballout.