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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746ngh6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746ngh6</a>

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effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

## 2.9 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers.
- External flash status register polling mode.
- Memory mapped mode.

Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

## 2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

## 2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

The RTC is functional in  $V_{BAT}$  mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in  $V_{BAT}$  mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

## 2.20 Low-power modes

The devices support three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in Stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

**Table 5. Voltage regulator modes in Stop mode**

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

## 2.24 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds USART. Refer to [Table 8: USART implementation](#) for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (Max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Programmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode ( T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard )
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

**Table 8. USART implementation**

features <sup>(1)</sup>	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

## 2.29 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

## 2.30 SD/SDIO/MMC card host interface (SDMMC)

An SDMMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory card specification version 2.0.

The SDMMC card specification version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

## 2.31 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Support of 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

## 2.38 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 108 MHz.

## 2.39 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

## 2.40 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as  $V_{BAT}$ , ADC1\_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and  $V_{BAT}$  conversion are enabled at the same time, only  $V_{BAT}$  conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

## 2.41 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.



Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) <sup>(1)</sup>	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
41	H6	K4	64	P10	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	J6	L4	65	R10	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	K6	N4	66	N11	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	G7	M4	67	P11	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	H7	L3	68	R11	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	J7	M3	69	R12	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	N3	70	R13	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_R MII_TX_EN, LCD_G5, EVENTOUT	-
48	F8	N2	71	M10	81	92	L11	VCAP_1	S	-	-	-	-
49	-	H2	-	-	-	93	K9	VSS	S	-	-	-	-
50	-	J6	72	N10	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	-	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-
PB7	NADV	NADV	-	-

**Table 19. VCAP1/VCAP2 operating conditions<sup>(1)</sup>**

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 $\mu$ F
ESR	ESR of external capacitor	< 2 $\Omega$

1. When bypassing the voltage regulator, the two 2.2  $\mu$ F  $V_{CAP}$  capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

### 5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for  $T_A$ .

**Table 20. Operating conditions at power-up / power-down (regulator ON)**

Symbol	Parameter	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	20	$\infty$	$\mu$ s/V
	$V_{DD}$ fall time rate	20	$\infty$	

### 5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for  $T_A$ .

**Table 21. Operating conditions at power-up / power-down (regulator OFF)<sup>(1)</sup>**

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	Power-up	20	$\infty$	$\mu$ s/V
	$V_{DD}$ fall time rate	Power-down	20	$\infty$	
$t_{VCAP}$	$V_{CAP\_1}$ and $V_{CAP\_2}$ rise time rate	Power-up	20	$\infty$	
	$V_{CAP\_1}$ and $V_{CAP\_2}$ fall time rate	Power-down	20	$\infty$	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when  $V_{DD}$  reach below 1.08 V.

### 5.3.5 Reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 17](#).

**Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator OFF**

Symbol	Parameter	Conditions	f <sub>HCLK</sub> (MHz)	Typ		Max <sup>(1)</sup>						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and VDD supply	All Peripherals Enabled <sup>(2)(3)</sup>	180	151	1	174	2	190	2	204	2	mA
			168	135	1	156	2	170	2	182	2	
			144	108	1	124	2	136	2	146	2	
			60	52	1	60	2	71	2	82	2	
			25	25	1	29	2	40	2	50	2	
		All Peripherals Disabled <sup>(3)</sup>	180	89	1	102	2	117	2	130	2	
			168	80	1	91	2	105	2	118	2	
			144	66	1	75	2	86	2	97	2	
			60	33	1	38	2	49	2	60	2	
			25	16	1	18	2	29	2	40	2	

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

3. When the ADC is ON (ADON bit set in the ADC\_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

**Table 31. Typical and maximum current consumptions in Stop mode**

Symbol	Parameter	Conditions	Typ	Max <sup>(1)</sup>				Unit
			V <sub>DD</sub> = 3.6 V					
			T <sub>A</sub> = 25 °C	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C		
I <sub>DD_STOP_NM</sub> (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.45	2.00	14.00	22.00	mA	
		Flash memory in Deep power down mode, all oscillators OFF	0.40	2.00	14.00	22.00		
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.32	1.50	10.00	18.00		
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.27	1.50	10.00	18.00		
I <sub>DD_STOP_UDM</sub> (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.15	0.80	4.00	7.00		
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.10	0.70	4.00	7.00		

1. Data based on characterization, tested in production.

### 5.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 36](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and  $V_{DD}=3.3$  V.

**Table 36. Low-power mode wakeup timings**

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Max <sup>(1)</sup>	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	13	13	CPU clock cycles
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	$\mu s$
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode )	112.7	120	
$t_{WUSTDBY}^{(2)}$	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

### 5.3.9 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 30](#).

The characteristics given in [Table 37](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

**Table 37. High-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HSE\_ext}$	External user clock source frequency <sup>(1)</sup>	-	1	-	50	MHz
$V_{HSEH}$	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	$V_{DD}$	V
$V_{HSEL}$	OSC_IN input pin low level voltage		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time <sup>(1)</sup>		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time <sup>(1)</sup>		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance <sup>(1)</sup>	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
$I_L$	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design.

#### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 56: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 31](#).

The characteristics given in [Table 38](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

**Table 40. LSE oscillator characteristics ( $f_{LSE} = 32.768 \text{ kHz}$ ) <sup>(1)</sup> (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_{m\_crit\_max}$	Maximum critical crystal $g_m$	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	$\mu A/V$
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
$t_{SU}^{(2)}$	start-up time	$V_{DD}$ is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results.  $t_{SU}$  is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note:* For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

**Figure 33. Typical application with a 32.768 kHz crystal**

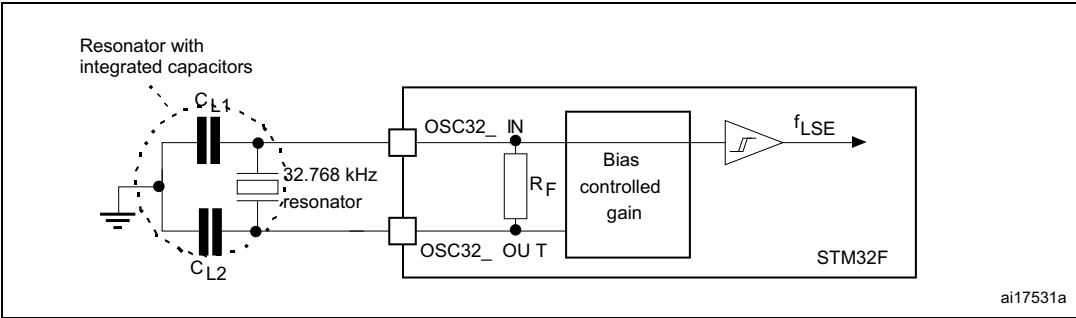




Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	FT, TTa and NRST I/O input high level voltage <sup>(5)</sup>		1.7 V≤V <sub>DD</sub> ≤3.6 V	0.45V <sub>DD</sub> +0.3 <sup>(1)</sup>	-	-	V
				0.7V <sub>DD</sub> <sup>(2)</sup>			
	BOOT I/O input high level voltage		1.75 V≤V <sub>DD</sub> ≤3.6 V, −40 °C≤T <sub>A</sub> ≤105 °C	0.17V <sub>DD</sub> +0.7 <sup>(1)</sup>	-	-	
1.7 V≤V <sub>DD</sub> ≤3.6 V, 0 °C≤T <sub>A</sub> ≤105 °C							
V <sub>HYS</sub>	FT, TTa and NRST I/O input hysteresis		1.7 V≤V <sub>DD</sub> ≤3.6 V	10%V <sub>DD</sub> <sup>(3)</sup>	-	-	V
	BOOT I/O input hysteresis		1.75 V≤V <sub>DD</sub> ≤3.6 V, −40 °C≤T <sub>A</sub> ≤105 °C	0.1	-	-	
			1.7 V≤V <sub>DD</sub> ≤3.6 V, 0 °C≤T <sub>A</sub> ≤105 °C				
I <sub>lkg</sub>	I/O input leakage current <sup>(4)</sup>		V <sub>SS</sub> ≤V <sub>IN</sub> ≤V <sub>DD</sub>	-	-	±1	μA
	I/O FT input leakage current <sup>(5)</sup>		V <sub>IN</sub> = 5 V	-	-	3	
R <sub>PU</sub>	Weak pull-up equivalent resistor <sup>(6)</sup>	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID )	V <sub>IN</sub> = V <sub>SS</sub>	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID )		7	10	14	
R <sub>PD</sub>	Weak pull-down equivalent resistor <sup>(7)</sup>	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID )	V <sub>IN</sub> = V <sub>DD</sub>	30	40	50	
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID )		7	10	14	
C <sub>IO</sub> <sup>(8)</sup>	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.

2. Tested in production.

3. With a minimum of 200 mV.

4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to [Table 55: I/O current injection susceptibility](#)5. To sustain a voltage higher than  $V_{DD} + 0.3\text{ V}$ , the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 55: I/O current injection susceptibility](#)

6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).

**Table 92. Asynchronous multiplexed PSRAM/NOR read timings<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}-0.5$	$3T_{HCLK}+1.5$	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}-1$	$2T_{HCLK}+0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{HCLK}-0.5$	$T_{HCLK}+0.5$	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK}-0.5$	$T_{HCLK}+1.5$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	$T_{HCLK}-0.5$	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{HCLK}-2$	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	$T_{HCLK}-2$	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

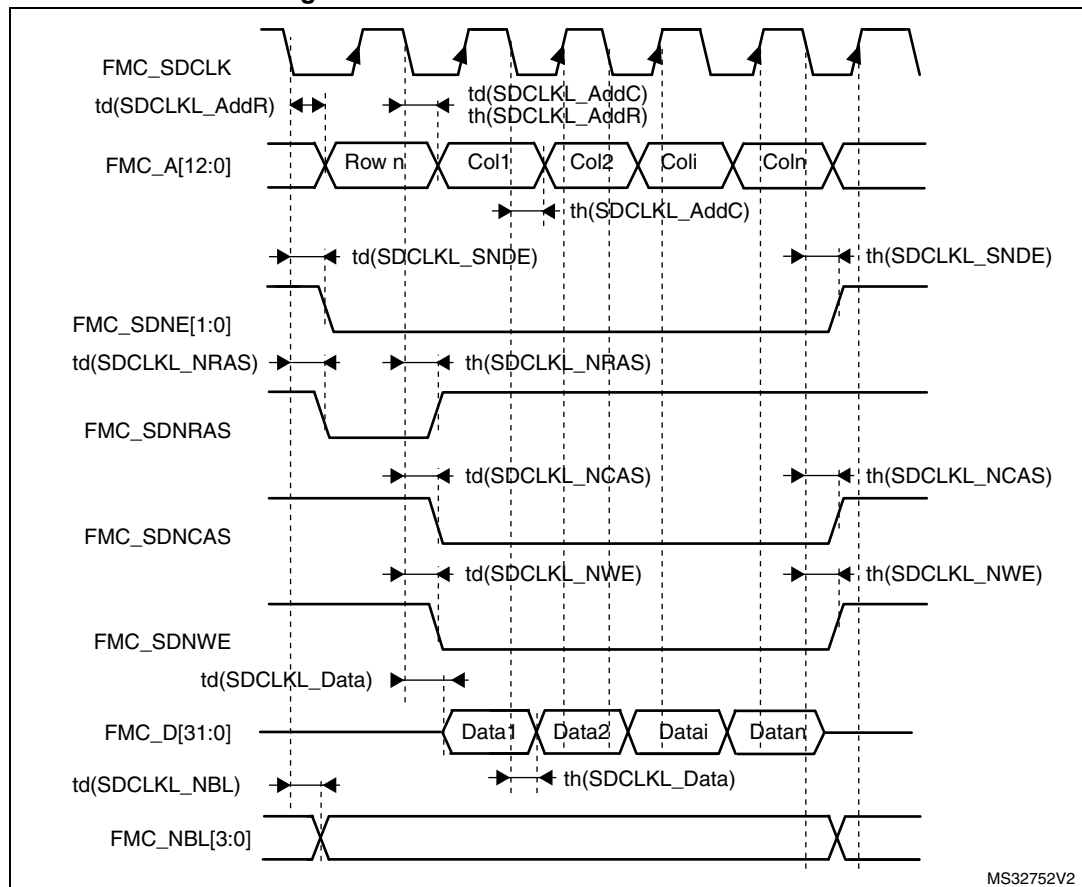
1. Guaranteed by characterization results.

**Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings<sup>(1)</sup>**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}-1$	$8T_{HCLK}+2$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}-1$	$5T_{HCLK}+1$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}+1.5$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}+1$	-	

1. Guaranteed by characterization results.

Figure 71. SDRAM write access waveforms

Table 104. SDRAM write timings<sup>(1)</sup>

Symbol	Parameter	Min	Max	Unit
$t_w(\text{SDCLK})$	FMC_SDCLK period	$2T_{\text{HCLK}}-0.5$	$2T_{\text{HCLK}}+0.5$	ns
$t_d(\text{SDCLKL\_Data})$	Data output valid time	-	2	
$t_h(\text{SDCLKL\_Data})$	Data output hold time	0.5	-	
$t_d(\text{SDCLKL\_Add})$	Address valid time	-	4	
$t_d(\text{SDCLKL\_SDNWE})$	SDNWE valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNWE})$	SDNWE hold time	0	-	
$t_d(\text{SDCLKL\_SDNE})$	Chip select valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNE})$	Chip select hold time	0	-	
$t_d(\text{SDCLKL\_SDNRAS})$	SDNRAS valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNRAS})$	SDNRAS hold time	0	-	
$t_d(\text{SDCLKL\_SDNCAS})$	SDNCAS valid time	-	0.5	
$t_h(\text{SDCLKL\_SDNCAS})$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Figure 75. LCD-TFT horizontal timing diagram

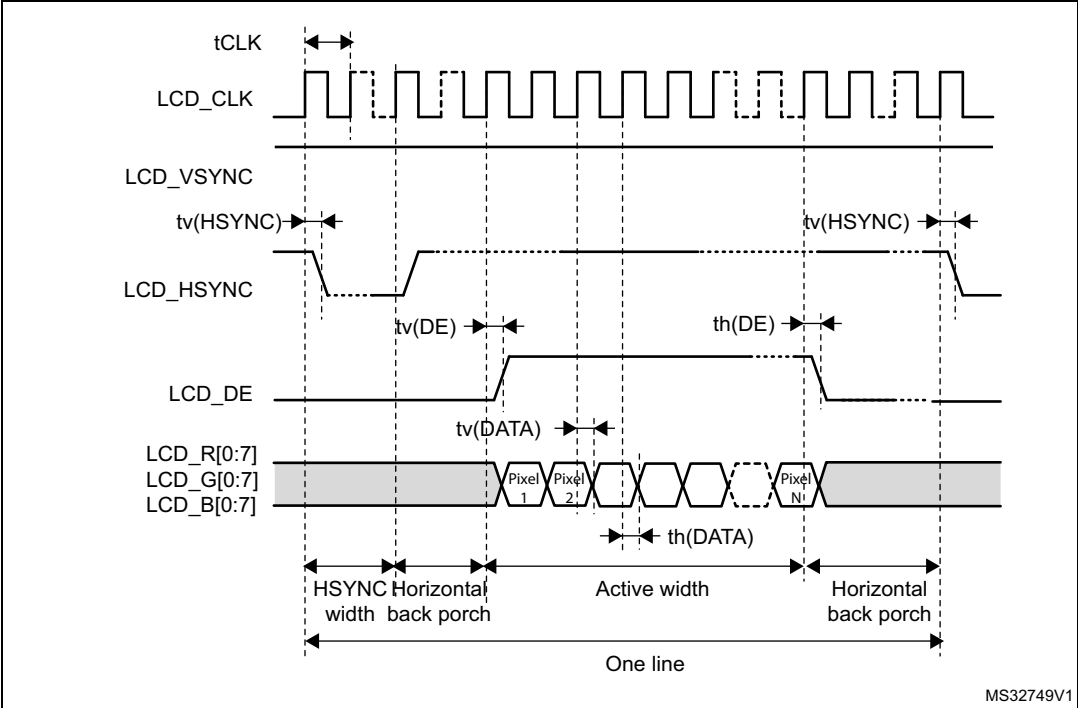
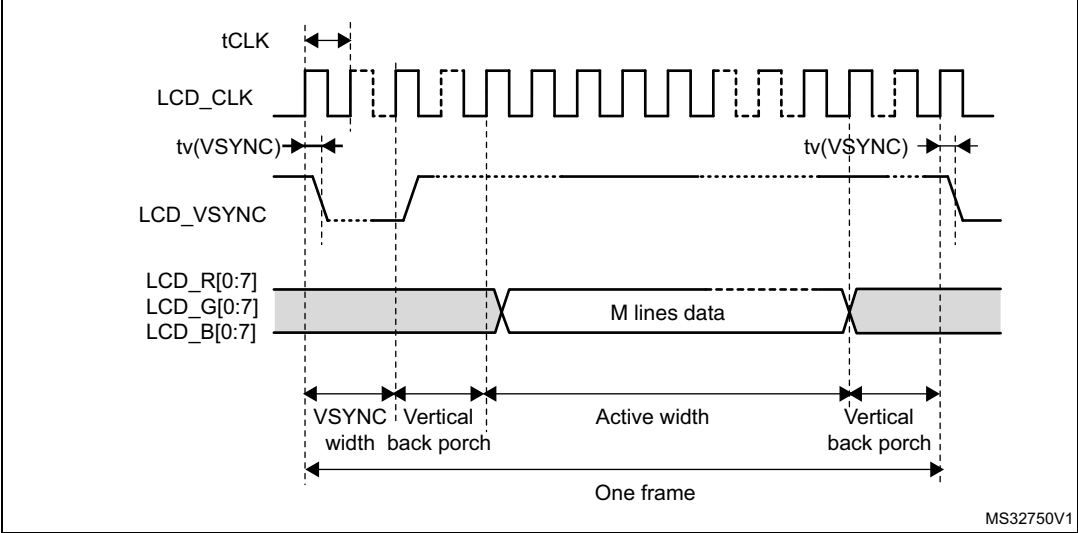
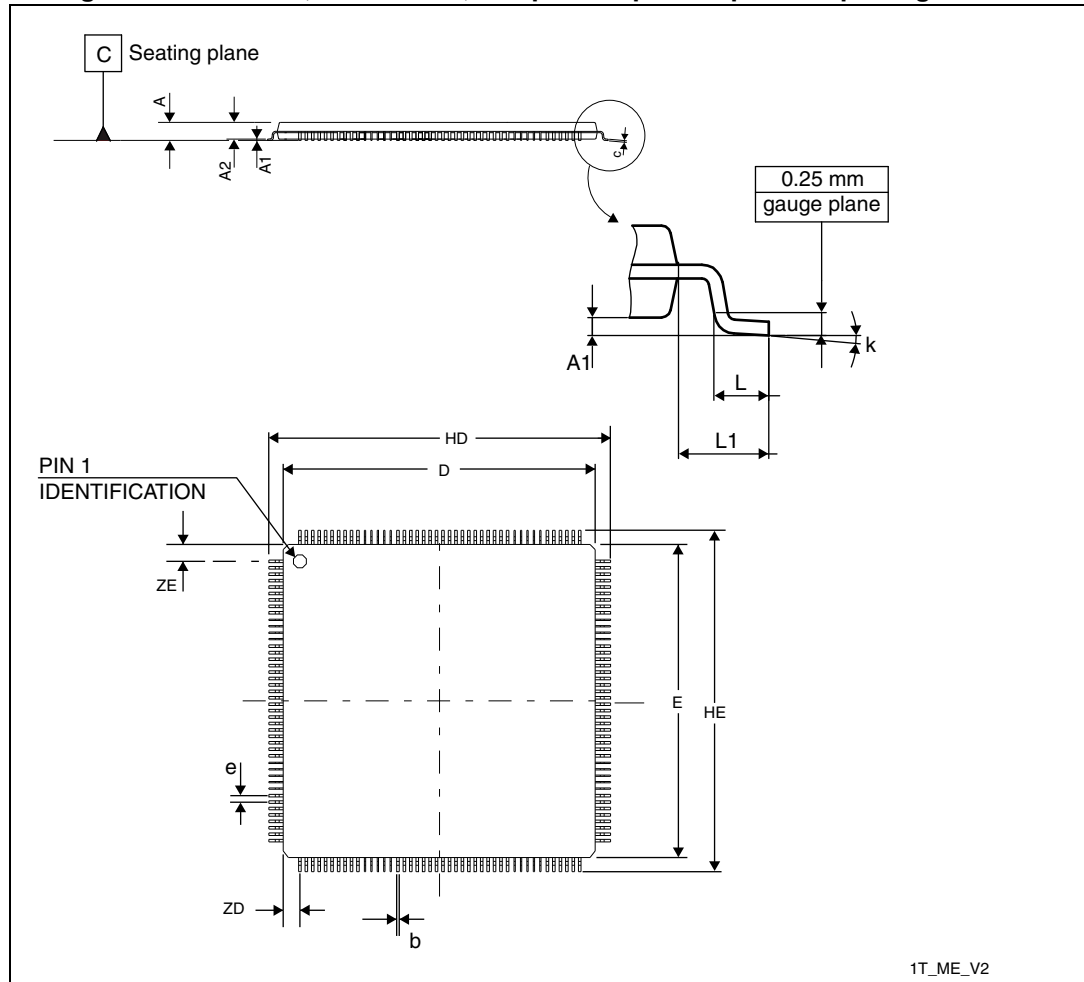


Figure 76. LCD-TFT vertical timing diagram



## 6.5 LQFP176, 24 x 24 mm low-profile quad flat package information

Figure 91. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 118. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488