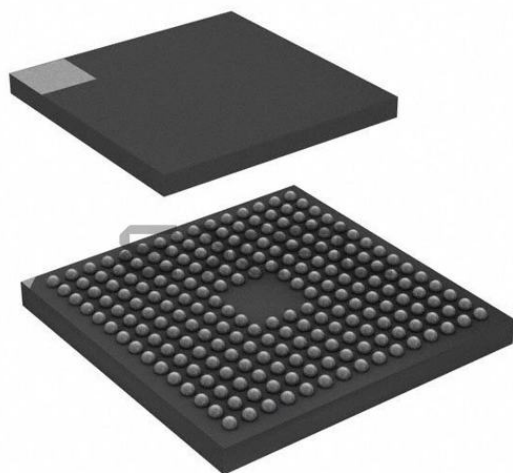




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	168
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	216-TFBGA
Supplier Device Package	216-TFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746ngh6e

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Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) ⁽¹⁾
Advanced-control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

Table 8. USART implementation (continued)

features ⁽¹⁾	USART1/2/3/6	UART4/5/7/8
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X

1. X: supported.

2.25 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 50 Mbits/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All SPIs can be served by the DMA controller.

Three standard I²S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

2.26 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

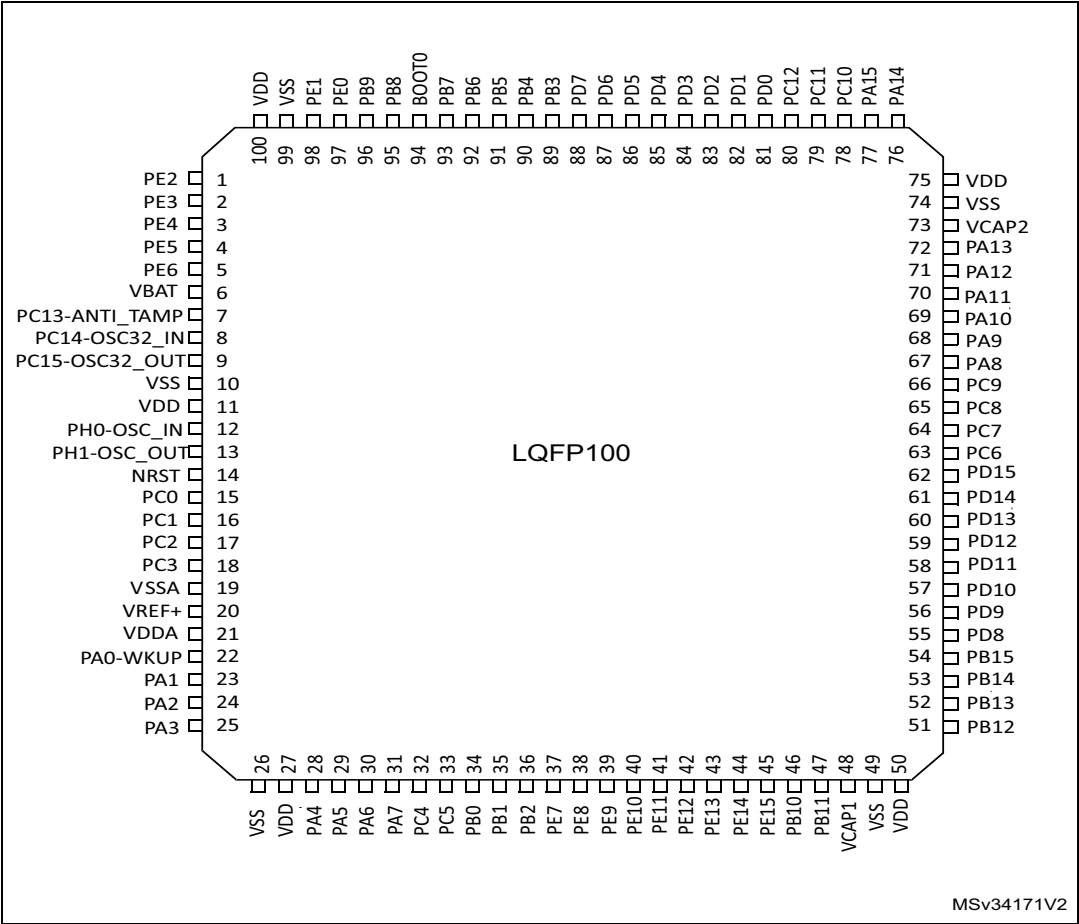
The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

3 Pinouts and pin description

Figure 11. STM32F74xVx LQFP100 pinout



2. The above figure shows the package top view.

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	E4	13	13	F3	PI11	I/O	FT	-	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	E7	-	F2	14	14	F2	VSS	S	-	-	-	-
-	-	E10	-	F3	15	15	F4	VDD	S	-	-	-	-
-	-	F11	10	E2	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	E9	11	H3	17	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	F10	12	H2	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	-	G11	13	J2	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	-	F9	14	J3	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	-	F8	15	K3	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	C2	H7	16	G2	22	25	H6	VSS	S	-	-	-	-
11	D2	-	17	G3	23	26	H5	VDD	S	-	-	-	-
-	-	G10	18	K2	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4
-	-	F7	19	K1	25	28	K1	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	-	-	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT	-
-	-	-	-	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	K2	M11	37	R2	47	50	R2	PA3	I/O	FT	(4)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
26	J1	-	38	-	-	51	K6	VSS	S	-	-	-	-
-	E6	N11	-	L4	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	K1	J8	39	K4	49	52	K5	VDD	S	-	-	-	-
28	G3	M10	40	N4	50	53	N4	PA4	I/O	TTa	(4)	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
29	H3	M9	41	P4	51	54	P4	PA5	I/O	TTa	(4)	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
30	J3	N10	42	P3	52	55	P3	PA6	I/O	FT	(4)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	G2	93	H14	112	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIFRX_IN2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT	-
-	-	D2	94	G12	113	136	G10	VSS	S	-	-	-	-
-	F6	G1	95	H13	114	137	G11	VDDUSB	S	-	-	-	-
63	F10	F2	96	H15	115	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	E10	F3	97	G15	116	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	F9	E4	98	G14	117	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	E9	E3	99	F14	118	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, DCMI_D3, EVENTOUT	-
67	D9	F1	100	F15	119	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
68	C9	E2	101	E15	120	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VB US

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SPI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVEN TOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	-	UART4_RTS	-	-	-	-	-	-	EVEN TOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	-	EVEN TOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	-	EVEN TOUT
	PB2	-	-	-	-	-	-	SAI1_SDA	SPI3_MOSI/I2S3_SD	-	QUADSPI_CLK	-	-	-	-	-	EVEN TOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	EVEN TOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-	EVEN TOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SD_CKE1	DCMI_D10	-	EVEN TOUT
	PB6	-	-	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	-	FMC_SD_NE1	DCMI_D5	-	EVEN TOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVEN TOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVEN TOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/ 11/LPTIM 1/CEC	I2C1/2/3/ 4/CEC	SPI1/2/3/ 4/5/6	SPI3/ SAI1	SPI2/3/U SART1/2/ 3/UART5/ SPDIFRX	SAI2/US ART6/UA RT4/5/7/8 /SPDIFR X	CAN1/2/T IM12/13/ 14/QUAD SPI/LCD	SAI2/QU ADSPI/O TG2_HS/ OTG1_FS	ETH/ OTG1_FS	FMC/SD MMC1/O TG2_FS	DCMI	LCD	SYS
Port H	PH8	-	-	-	-	I2C3_SD A	-	-	-	-	-	-	-	FMC_D1 6	DCMI_H SYNC	LCD_R2	EVEN TOUT
	PH9	-	-	-	-	I2C3_SM BA	-	-	-	-	TIM12_C H2	-	-	FMC_D1 7	DCMI_D 0	LCD_R3	EVEN TOUT
	PH10	-	-	TIM5_C H1	-	I2C4_SM BA	-	-	-	-	-	-	-	FMC_D1 8	DCMI_D 1	LCD_R4	EVEN TOUT
	PH11	-	-	TIM5_C H2	-	I2C4_SC L	-	-	-	-	-	-	-	FMC_D1 9	DCMI_D 2	LCD_R5	EVEN TOUT
	PH12	-	-	TIM5_C H3	-	I2C4_SD A	-	-	-	-	-	-	-	FMC_D2 0	DCMI_D 3	LCD_R6	EVEN TOUT
	PH13	-	-	-	TIM8_CH 1N	-	-	-	-	-	CAN1_T X	-	-	FMC_D2 1	-	LCD_G2	EVEN TOUT
	PH14	-	-	-	TIM8_CH 2N	-	-	-	-	-	-	-	-	FMC_D2 2	DCMI_D 4	LCD_G3	EVEN TOUT
	PH15	-	-	-	TIM8_CH 3N	-	-	-	-	-	-	-	-	FMC_D2 3	DCMI_D 11	LCD_G4	EVEN TOUT
Port I	PI0	-	-	TIM5_C H4	-	-	SPI2_NS S/I2S2_ WS	-	-	-	-	-	-	FMC_D2 4	DCMI_D 13	LCD_G5	EVEN TOUT
	PI1	-	-	-	TIM8_BKI N2	-	SPI2_SC K/I2S2_ CK	-	-	-	-	-	-	FMC_D2 5	DCMI_D 8	LCD_G6	EVEN TOUT
	PI2	-	-	-	TIM8_CH 4	-	SPI2_MI SO	-	-	-	-	-	-	FMC_D2 6	DCMI_D 9	LCD_G7	EVEN TOUT
	PI3	-	-	-	TIM8_ET R	-	SPI2_M OSI/I2S2_ _SD	-	-	-	-	-	-	FMC_D2 7	DCMI_D 10	-	EVEN TOUT
	PI4	-	-	-	TIM8_BKI N	-	-	-	-	-	-	SAI2_MC K_A	-	FMC_NB L2	DCMI_D 5	LCD_B4	EVEN TOUT
	PI5	-	-	-	TIM8_CH 1	-	-	-	-	-	-	SAI2_SC K_A	-	FMC_NB L3	DCMI_V SYNC	LCD_B5	EVEN TOUT
	PI6	-	-	-	TIM8_CH 2	-	-	-	-	-	-	SAI2_SD_ A	-	FMC_D2 8	DCMI_D 6	LCD_B6	EVEN TOUT

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000 - 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00 - 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	Chrom-ART (DMA2D)
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory or SRAM on AXI (L1-cache disabled), regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I _{DD}	Supply current in RUN mode	All peripherals enabled ⁽²⁾⁽³⁾	216	181	210	233	-	mA
			200	168	194	216	234	
			180	153	176	192	206	
			168	136	157	172	184	
			144	109	125	137	148	
			60	53	61	73	84	
			25	26	30	41	52	
		All peripherals disabled ⁽³⁾	216	105	121	145	-	
			200	98	112	134	153	
			180	90	103	119	132	
			168	81	93	107	120	
			144	67	76	88	89	
			60	34	40	51	62	
			25	17	20	31	42	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 56. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V _{IH}	FT, TTa and NRST I/O input high level voltage ⁽⁵⁾		1.7 V≤V _{DD} ≤3.6 V	0.45V _{DD} +0.3 ⁽¹⁾	-	-	V
				0.7V _{DD} ⁽²⁾			
	BOOT I/O input high level voltage		1.75 V≤V _{DD} ≤3.6 V, −40 °C≤T _A ≤105 °C	0.17V _{DD} +0.7 ⁽¹⁾	-	-	
1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C							
V _{HYS}	FT, TTa and NRST I/O input hysteresis		1.7 V≤V _{DD} ≤3.6 V	10%V _{DD} ⁽³⁾	-	-	V
	BOOT I/O input hysteresis		1.75 V≤V _{DD} ≤3.6 V, −40 °C≤T _A ≤105 °C	0.1	-	-	
			1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C				
I _{lkg}	I/O input leakage current ⁽⁴⁾		V _{SS} ≤V _{IN} ≤V _{DD}	-	-	±1	μA
	I/O FT input leakage current ⁽⁵⁾		V _{IN} = 5 V	-	-	3	
R _{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	V _{IN} = V _{SS}	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
R _{PD}	Weak pull-down equivalent resistor ⁽⁷⁾	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	V _{IN} = V _{DD}	30	40	50	
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
C _{IO} ⁽⁸⁾	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.

2. Tested in production.

3. With a minimum of 200 mV.

4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to [Table 55: I/O current injection susceptibility](#)5. To sustain a voltage higher than $V_{DD} + 0.3\text{ V}$, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 55: I/O current injection susceptibility](#)

6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).

Table 65. ADC static accuracy at $f_{\text{ADC}} = 36 \text{ MHz}$

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{\text{ADC}} = 36 \text{ MHz}$, $V_{\text{DDA}} = 2.4 \text{ to } 3.6 \text{ V}$, $V_{\text{REF}} = 1.7 \text{ to } 3.6 \text{ V}$ $V_{\text{DDA}} - V_{\text{REF}} < 1.2 \text{ V}$	± 4	± 7	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 3	± 6	
ED	Differential linearity error		± 2	± 3	
EL	Integral linearity error		± 3	± 6	

1. Guaranteed by characterization results.

Table 66. ADC dynamic accuracy at $f_{\text{ADC}} = 18 \text{ MHz}$ - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 18 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF+}} = 1.7 \text{ V}$ Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		- 67	- 72	-	

1. Guaranteed by characterization results.

Table 67. ADC dynamic accuracy at $f_{\text{ADC}} = 36 \text{ MHz}$ - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 36 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF+}} = 3.3 \text{ V}$ Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		- 70	- 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{\text{INJ(PIN)}}$ and $\Sigma I_{\text{INJ(PIN)}}$ in [Section 5.3.17](#) does not affect the ADC accuracy.

1. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+1.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}-0.5$	$7T_{HCLK}+0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+2$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 62 through Figure 65 represent synchronous waveforms and Table 96 through Table 99 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For $2.7 V \leq V_{DD} \leq 3.6 V$, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For $1.71 V \leq V_{DD} < 2.7 V$, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 63. Synchronous multiplexed PSRAM write timings

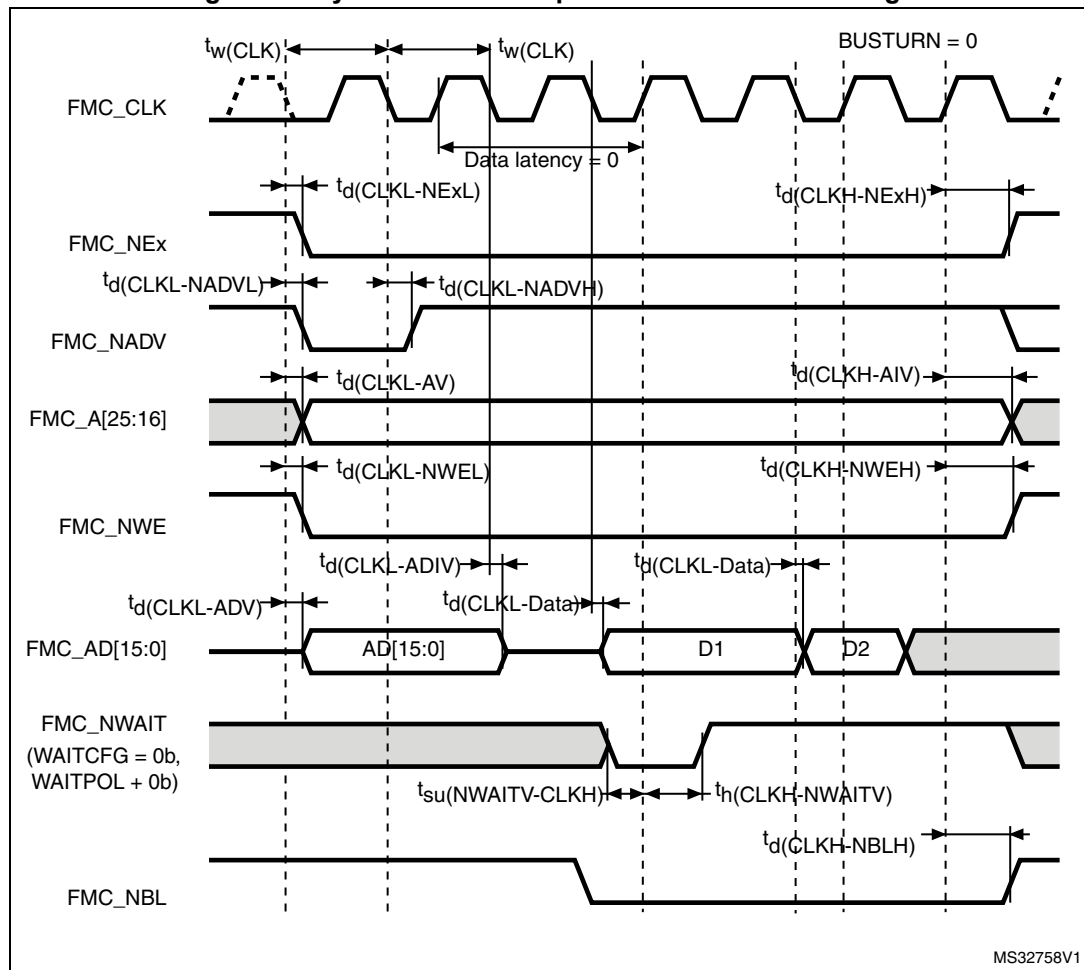


Table 99. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{CLK}	FMC_CLK period	$2T_{\text{HCLK}}-1$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low ($x=0..2$)	-	2.5	
$t_{\text{d}}(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high ($x=0..2$)	$T_{\text{HCLK}}+0.5$	-	
$t_{\text{d}}(\text{CLKL-NADV})$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{\text{d}}(\text{CLKL-NADVH})$	FMC_CLK low to FMC_NADV high	0	-	
$t_{\text{d}}(\text{CLKL-AV})$	FMC_CLK low to FMC_Ax valid ($x=16..25$)	-	2.5	
$t_{\text{d}}(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid ($x=16..25$)	0	-	
$t_{\text{d}}(\text{CLKL-NWEL})$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{\text{d}}(\text{CLKH-NWEH})$	FMC_CLK high to FMC_NWE high	$T_{\text{HCLK}}+1$	-	
$t_{\text{d}}(\text{CLKL-Data})$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{\text{d}}(\text{CLKL-NBLL})$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{\text{d}}(\text{CLKH-NBLH})$	FMC_CLK high to FMC_NBL high	$T_{\text{HCLK}}+0.5$	-	
$t_{\text{su}}(\text{NWAIT-CLKH})$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{\text{h}}(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 66 through Figure 69 represent synchronous waveforms, and Table 100 and Table 101 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 72. Quad-SPI timing diagram - SDR mode

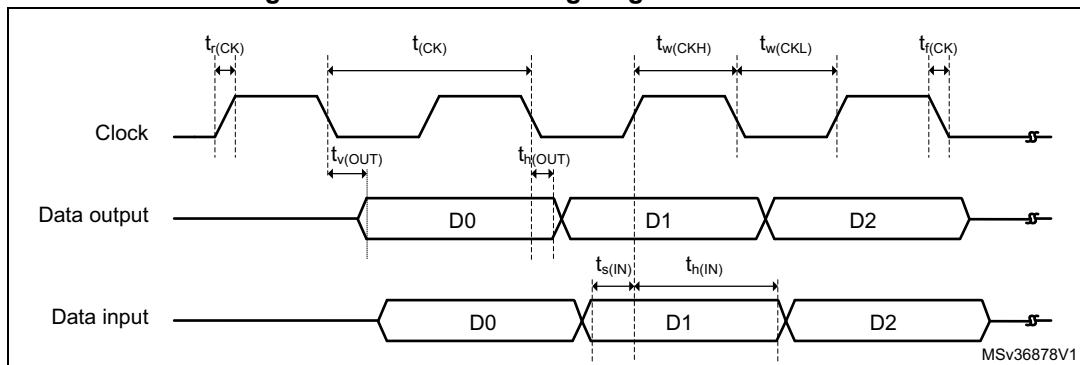
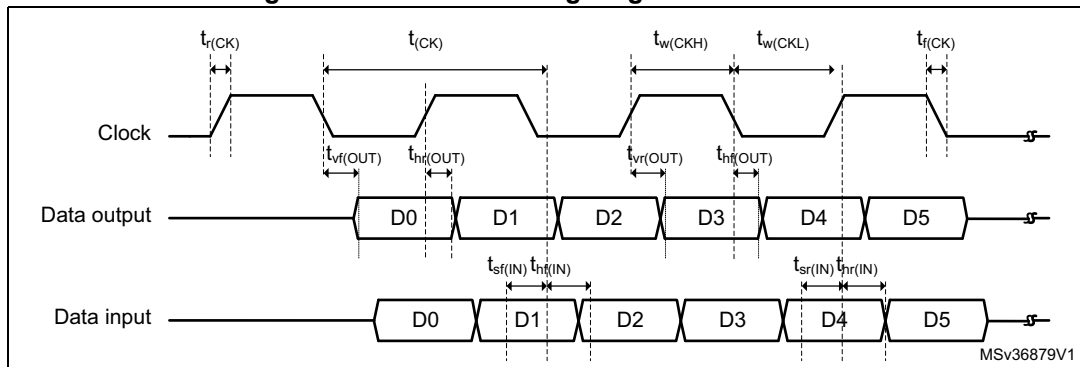


Figure 73. Quad-SPI timing diagram - DDR mode



5.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in [Table 108](#) for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in [Table 17](#), with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

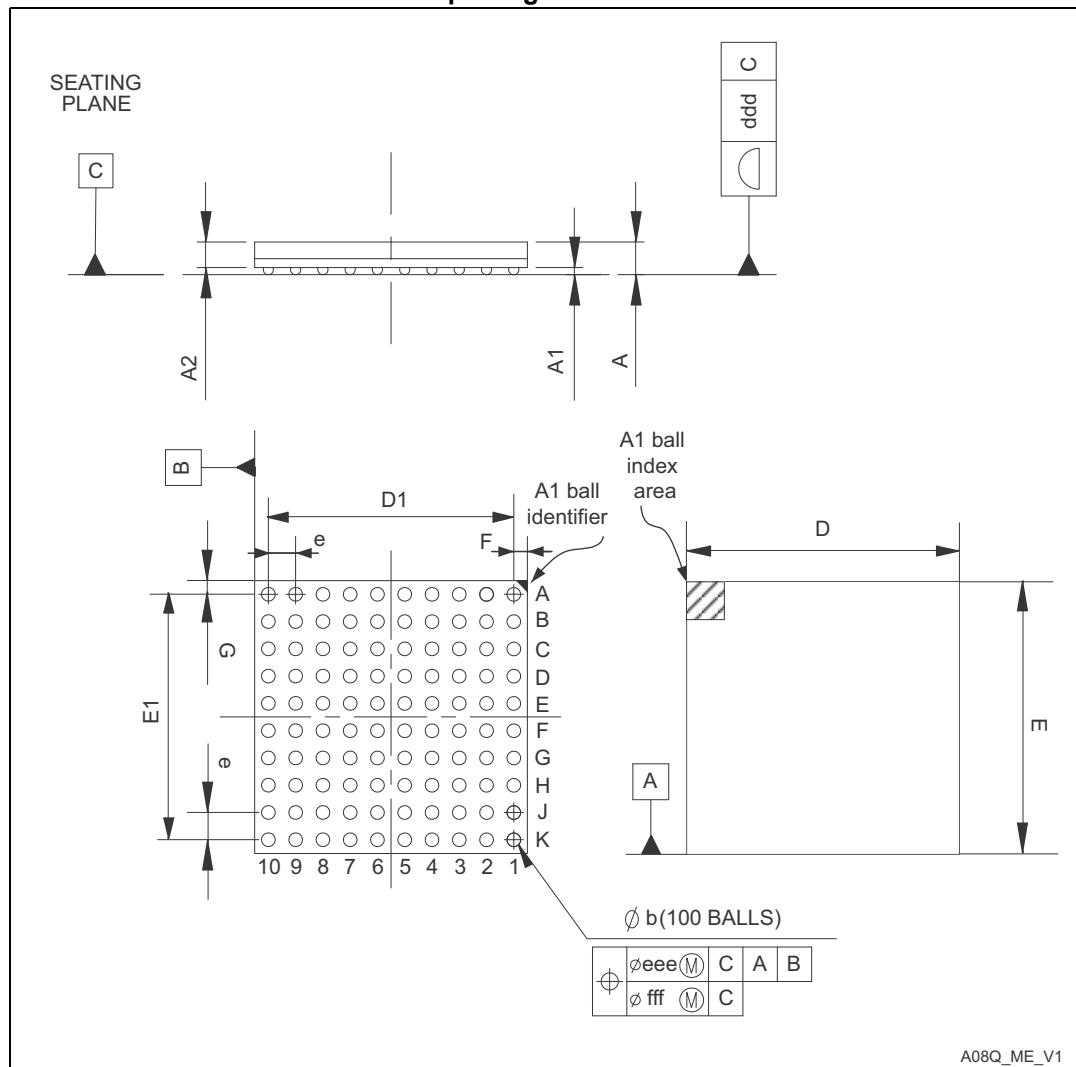
Table 108. DCMI characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/ f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su}(DATA)$	Data input setup time	3.5	-	ns
$t_h(DATA)$	Data input hold time	0	-	
$t_{su}(HSYNC)$ $t_{su}(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_h(HSYNC)$ $t_h(VSYNC)$	DCMI_HSYNC/DCMI_VSYNC input hold time	0	-	

1. Guaranteed by characterization results.

6.2 TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package information

Figure 82. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 113. TFBGA100, 8 x 8 x 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177

6.9 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 124. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient TFBGA100 - 8 × 8 mm / 0.8 mm pitch	57	
	Thermal resistance junction-ambient WLCSP143	31.2	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA176 - 10 × 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.