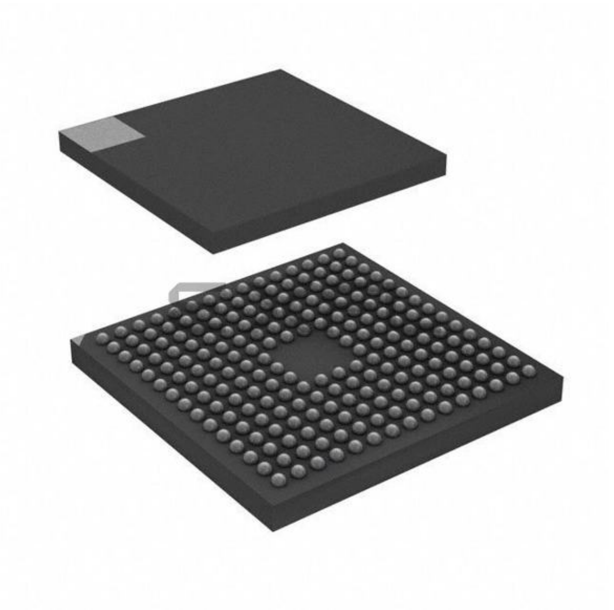

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

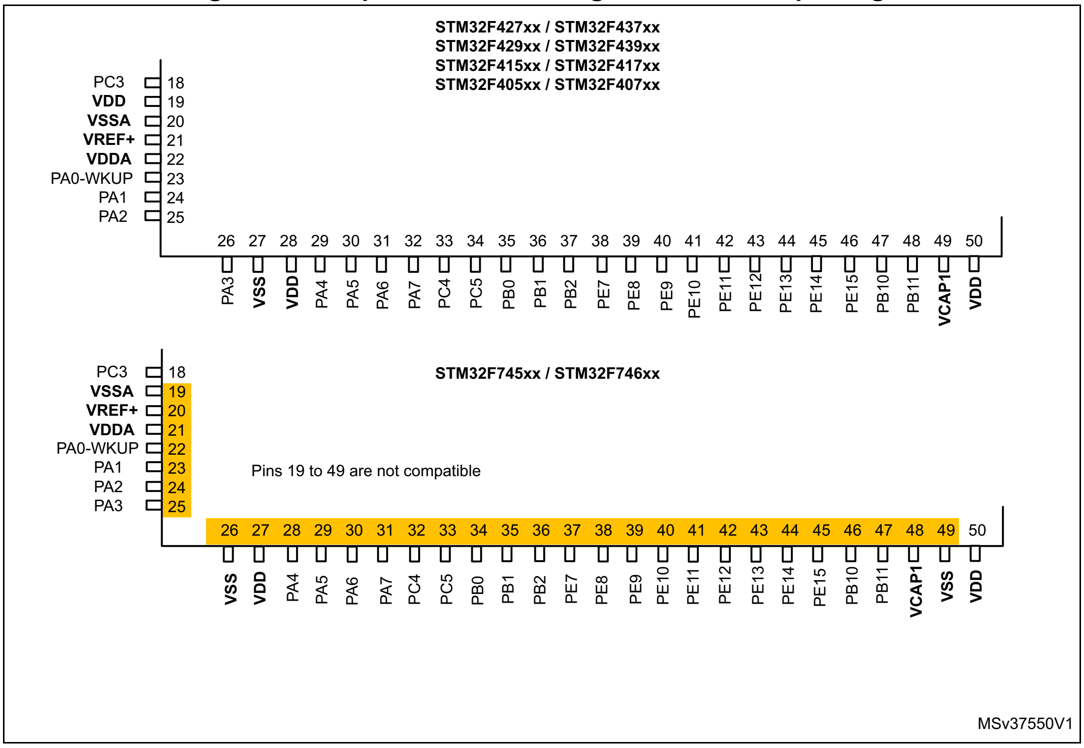
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 168 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 320K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 216-TFBGA |
| Supplier Device Package | 216-TFBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746ngh7 |

## 1.1 Full compatibility throughout the family

The STM32F745xx and STM32F746xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

*Figure 1* give compatible board designs between the STM32F4xx families.

**Figure 1. Compatible board design for LQFP100 package**




The STM32F745xx and STM32F746xx LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176, WLCSP143 packages are fully pin to pin compatible with STM32F4xxxx devices.

**Table 6. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Complementary output | Max interface clock (MHz) | Max timer clock (MHz)(1) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced-control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 108 | 216 |
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 54 | 108/216 |
| | TIM9 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 108 | 216 |
| | TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 108 | 216 |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 54 | 108/216 |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 54 | 108/216 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 54 | 108/216 |

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

Table 8. USART implementation (continued)

| features[1] | USART1/2/3/6 | UART4/5/7/8 |
|---|---|---|
| Smartcard mode | X | - |
| Single-wire half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | X |
| LIN mode | X | X |
| Dual clock domain | X | X |
| Receiver timeout interrupt | X | X |
| Modbus communication | X | X |
| Auto baud rate detection | X | X |
| Driver Enable | X | X |

1. X: supported.

## 2.25 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 50 Mbits/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All SPIs can be served by the DMA controller.

Three standard $I^2S$ interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

## 2.26 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be

configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

| Pin Number | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | WLCSP143 | LQFP144 | UFBGA176 | LQFP176 | LQFP208 | TFBGA216 | | | | | | |
| - | - | - | - | G4 | 44 | 47 | J4 | PH3 | I/O | FT | - | QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT | - |
| - | - | - | - | H4 | 45 | 48 | H4 | PH4 | I/O | FT | - | I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT | - |
| - | - | - | - | J4 | 46 | 49 | J3 | PH5 | I/O | FT | - | I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT | - |
| 25 | K2 | M11 | 37 | R2 | 47 | 50 | R2 | PA3 | I/O | FT | (4) | TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT | ADC123_IN3 |
| 26 | J1 | - | 38 | - | - | 51 | K6 | VSS | S | - | - | - | - |
| - | E6 | N11 | - | L4 | 48 | - | L5 | BYPASS_REG | I | FT | - | - | - |
| 27 | K1 | J8 | 39 | K4 | 49 | 52 | K5 | VDD | S | - | - | - | - |
| 28 | G3 | M10 | 40 | N4 | 50 | 53 | N4 | PA4 | I/O | TTa | (4) | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT | ADC12_IN4, DAC_OUT1 |
| 29 | H3 | M9 | 41 | P4 | 51 | 54 | P4 | PA5 | I/O | TTa | (4) | TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT | ADC12_IN5, DAC_OUT2 |
| 30 | J3 | N10 | 42 | P3 | 52 | 55 | P3 | PA6 | I/O | FT | (4) | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT | ADC12_IN6 |

**Table 11. FMC pin definition**

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF0 | A0 | - | - | A0 |
| PF1 | A1 | - | - | A1 |
| PF2 | A2 | - | - | A2 |
| PF3 | A3 | - | - | A3 |
| PF4 | A4 | - | - | A4 |
| PF5 | A5 | - | - | A5 |
| PF12 | A6 | - | - | A6 |
| PF13 | A7 | - | - | A7 |
| PF14 | A8 | - | - | A8 |
| PF15 | A9 | - | - | A9 |
| PG0 | A10 | - | - | A10 |
| PG1 | A11 | - | - | A11 |
| PG2 | A12 | - | - | A12 |
| PG3 | A13 | - | - | - |
| PG4 | A14 | - | - | BA0 |
| PG5 | A15 | - | - | BA1 |
| PD11 | A16 | A16 | CLE | - |
| PD12 | A17 | A17 | ALE | - |
| PD13 | A18 | A18 | - | - |
| PE3 | A19 | A19 | - | - |
| PE4 | A20 | A20 | - | - |
| PE5 | A21 | A21 | - | - |
| PE6 | A22 | A22 | - | - |
| PE2 | A23 | A23 | - | - |
| PG13 | A24 | A24 | - | - |
| PG14 | A25 | A25 | - | - |
| PD14 | D0 | DA0 | D0 | D0 |
| PD15 | D1 | DA1 | D1 | D1 |
| PD0 | D2 | DA2 | D2 | D2 |
| PD1 | D3 | DA3 | D3 | D3 |
| PE7 | D4 | DA4 | D4 | D4 |
| PE8 | D5 | DA5 | D5 | D5 |
| PE9 | D6 | DA6 | D6 | D6 |
| PE10 | D7 | DA7 | D7 | D7 |

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PE11 | D8 | DA8 | D8 | D8 |
| PE12 | D9 | DA9 | D9 | D9 |
| PE13 | D10 | DA10 | D10 | D10 |
| PE14 | D11 | DA11 | D11 | D11 |
| PE15 | D12 | DA12 | D12 | D12 |
| PD8 | D13 | DA13 | D13 | D13 |
| PD9 | D14 | DA14 | D14 | D14 |
| PD10 | D15 | DA15 | D15 | D15 |
| PH8 | D16 | - | - | D16 |
| PH9 | D17 | - | - | D17 |
| PH10 | D18 | - | - | D18 |
| PH11 | D19 | - | - | D19 |
| PH12 | D20 | - | - | D20 |
| PH13 | D21 | - | - | D21 |
| PH14 | D22 | - | - | D22 |
| PH15 | D23 | - | - | D23 |
| PI0 | D24 | - | - | D24 |
| PI1 | D25 | - | - | D25 |
| PI2 | D26 | - | - | D26 |
| PI3 | D27 | - | - | D27 |
| PI6 | D28 | - | - | D28 |
| PI7 | D29 | - | - | D29 |
| PI9 | D30 | - | - | D30 |
| PI10 | D31 | - | - | D31 |
| PD7 | NE1 | NE1 | - | - |
| PG9 | NE2 | NE2 | NCE | - |
| PG10 | NE3 | NE3 | - | - |
| PG11 | - | - | - | - |
| PG12 | NE4 | NE4 | - | - |
| PD3 | CLK | CLK | - | - |
| PD4 | NOE | NOE | NOE | - |
| PD5 | NWE | NWE | NWE | - |
| PD6 | NWAIT | NWAIT | NWAIT | - |
| PB7 | NADV | NADV | - | - |

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF6 | - | - | - | - |
| PF7 | - | - | - | - |
| PF8 | - | - | - | - |
| PF9 | - | - | - | - |
| PF10 | - | - | - | - |
| PG6 | - | - | - | - |
| PG7 | - | - | INT | - |
| PE0 | NBL0 | NBL0 | - | NBL0 |
| PE1 | NBL1 | NBL1 | - | NBL1 |
| PI4 | NBL2 | - | - | NBL2 |
| PI5 | NBL3 | - | - | NBL3 |
| PG8 | - | - | - | SDCLK |
| PC0 | - | - | - | SDNWE |
| PF11 | - | - | - | SDNRAS |
| PG15 | - | - | - | SDNCAS |
| PH2 | - | - | - | SDCKE0 |
| PH3 | - | - | - | SDNE0 |
| PH6 | - | - | - | SDNE1 |
| PH7 | - | - | - | SDCKE1 |
| PH5 | - | - | - | SDNWE |
| PC2 | - | - | - | SDNE0 |
| PC3 | - | - | - | SDCKE0 |
| PB5 | - | - | - | SDCKE1 |
| PB6 | - | - | - | SDNE1 |

## Table 12. STM32F745xx and STM32F746xx alternate function mapping

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port A | PA0 | - | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS | UART4_TX | - | SAI2_SD_B | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | UART4_RX | QUADSPI_BK1_IO3 | SAI2_MCK_B | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | LCD_R2 | EVENTOUT |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | SAI2_SCK_B | - | - | ETH_MDIO | - | - | LCD_R1 | EVENTOUT |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | LCD_B5 | EVENTOUT |
| | PA4 | - | - | - | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | - | - | - | - | OTG_HS_SOF | DCMI_HSYNC | LCD_VSYNC | EVENTOUT |
| | PA5 | - | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK/I2S1_CK | - | - | - | - | OTG_HS_ULPI_CK | - | - | - | LCD_R4 | EVENTOUT |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | - | SPI1_MISO | - | - | - | TIM13_CH1 | - | - | - | DCMI_PIXCLK | LCD_G2 | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI/I2S1_SD | - | - | - | TIM14_CH1 | - | ETH_MII_RX_DV/ETH_RMII_CRS_DV | FMC_SDNWE | - | - | EVENTOUT |
| | PA8 | MCO1 | TIM1_CH1 | - | TIM8_BKIN2 | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | - | - | - | LCD_R6 | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | SPI2_SCK/I2S2_CK | - | USART1_TX | - | - | - | - | - | DCMI_D0 | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | - | DCMI_D1 | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | - | - | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | LCD_R4 | EVENTOUT |

**Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4000 8000- 0x4000 FFFF | Reserved |
| APB1 | 0x4000 7C00 - 0x4000 7FFF | UART8 |
| | 0x4000 7800 - 0x4000 7BFF | UART7 |
| | 0x4000 7400 - 0x4000 77FF | DAC |
| | 0x4000 7000 - 0x4000 73FF | PWR |
| | 0x4000 6C00 - 0x4000 6FFF | HDMI-CEC |
| | 0x4000 6800 - 0x4000 6BFF | CAN2 |
| | 0x4000 6400 - 0x4000 67FF | CAN1 |
| | 0x4000 6000 - 0x4000 63FF | I2C4 |
| | 0x4000 5C00 - 0x4000 5FFF | I2C3 |
| | 0x4000 5800 - 0x4000 5BFF | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | I2C1 |
| | 0x4000 5000 - 0x4000 53FF | UART5 |
| | 0x4000 4C00 - 0x4000 4FFF | UART4 |
| | 0x4000 4800 - 0x4000 4BFF | USART3 |
| | 0x4000 4400 - 0x4000 47FF | USART2 |
| | 0x4000 4000 - 0x4000 43FF | SPDIFRX |
| | 0x4000 3C00 - 0x4000 3FFF | SPI3 / I2S3 |
| | 0x4000 3800 - 0x4000 3BFF | SPI2 / I2S2 |
| | 0x4000 3400 - 0x4000 37FF | Reserved |
| | 0x4000 3000 - 0x4000 33FF | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | RTC & BKP Registers |
| | 0x4000 2400 - 0x4000 27FF | LPTIM1 |
| | 0x4000 2000 - 0x4000 23FF | TIM14 |
| | 0x4000 1C00 - 0x4000 1FFF | TIM13 |
| | 0x4000 1800 - 0x4000 1BFF | TIM12 |
| | 0x4000 1400 - 0x4000 17FF | TIM7 |
| | 0x4000 1000 - 0x4000 13FF | TIM6 |
| | 0x4000 0C00 - 0x4000 0FFF | TIM5 |
| | 0x4000 0800 - 0x4000 0BFF | TIM4 |
| | 0x4000 0400 - 0x4000 07FF | TIM3 |
| | 0x4000 0000 - 0x4000 03FF | TIM2 |

Table 44. PLLI2S characteristics (continued)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Jitter(3) | Master I2S clock jitter | Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5 | RMS | - | 90 | - | |
| | | | peak to peak | - | ±280 | - | ps |
| | | Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples | | - | 90 | - | ps |
| | WS I2S clock jitter | Cycle to cycle at 48 KHz on 1000 samples | | - | 400 | - | ps |
| $I_{DD(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLLI2S)}$(4) | PLLI2S power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 45. PLLISAI characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLSAI\_IN}$ | PLLSAI input clock(1) | - | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLLSAIP\_OUT}$ | PLLSAI multiplier output clock for 48 MHz | - | - | 48 | 75 | MHz |
| $f_{PLLSAIQ\_OUT}$ | PLLSAI multiplier output clock for SAI | - | - | - | 216 | MHz |
| $f_{PLLSAIR\_OUT}$ | PLLSAI multiplier output clock for LCD-TFT | - | - | - | 216 | MHz |
| $f_{VCO\_OUT}$ | PLLSAI VCO output | - | 100 | - | 432 | MHz |
| $t_{LOCK}$ | PLLSAI lock time | VCO freq = 100 MHz | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | 100 | - | 300 | µs |

**Table 62. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | $V_{DDA}$ = 1.7(1) to 2.4 V | 0.6 | 15 | 18 | MHz |
| | | $V_{DDA}$ = 2.4 to 3.6 V | 0.6 | 30 | 36 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 30 MHz, 12-bit resolution | - | - | 1764 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2)(4) | Sampling switch resistance | - | - | - | 6 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | 4 | 7 | pF |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.100 | µs |
| | | | - | - | 3(5) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 30 MHz | - | - | 0.067 | µs |
| | | | - | - | 2(5) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 30 MHz | 0.100 | - | 16 | µs |
| | | - | 3 | - | 480 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | - | 2 | 3 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 30 MHz 12-bit resolution | 0.50 | - | 16.40 | µs |
| | | $f_{ADC}$ = 30 MHz 10-bit resolution | 0.43 | - | 16.34 | µs |
| | | $f_{ADC}$ = 30 MHz 8-bit resolution | 0.37 | - | 16.27 | µs |
| | | $f_{ADC}$ = 30 MHz 6-bit resolution | 0.30 | - | 16.20 | µs |
| | | 9 to 492 ($t_S$ for sampling +n-bit resolution for successive approximation) | | | | $1/f_{ADC}$ |
| $f_S$(2) | Sampling rate ($f_{ADC}$ = 30 MHz, and $t_S$ = 3 ADC cycles) | 12-bit resolution Single ADC | - | - | 2 | Msps |
| | | 12-bit resolution Interleave Dual ADC mode | - | - | 3.75 | Msps |
| | | 12-bit resolution Interleave Triple ADC mode | - | - | 6 | Msps |

**Figure 51. SAI master timing waveforms**

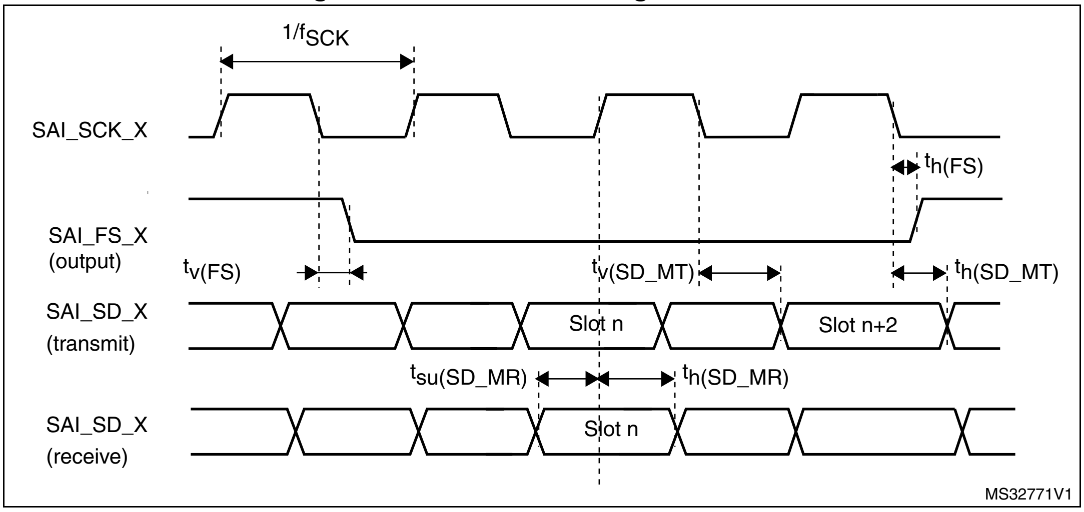



**Figure 52. SAI slave timing waveforms**

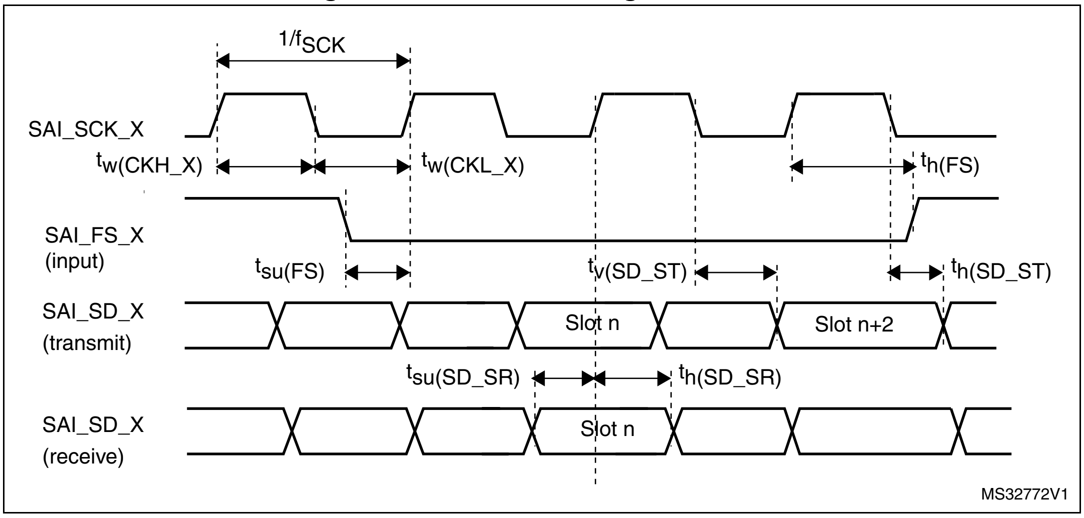
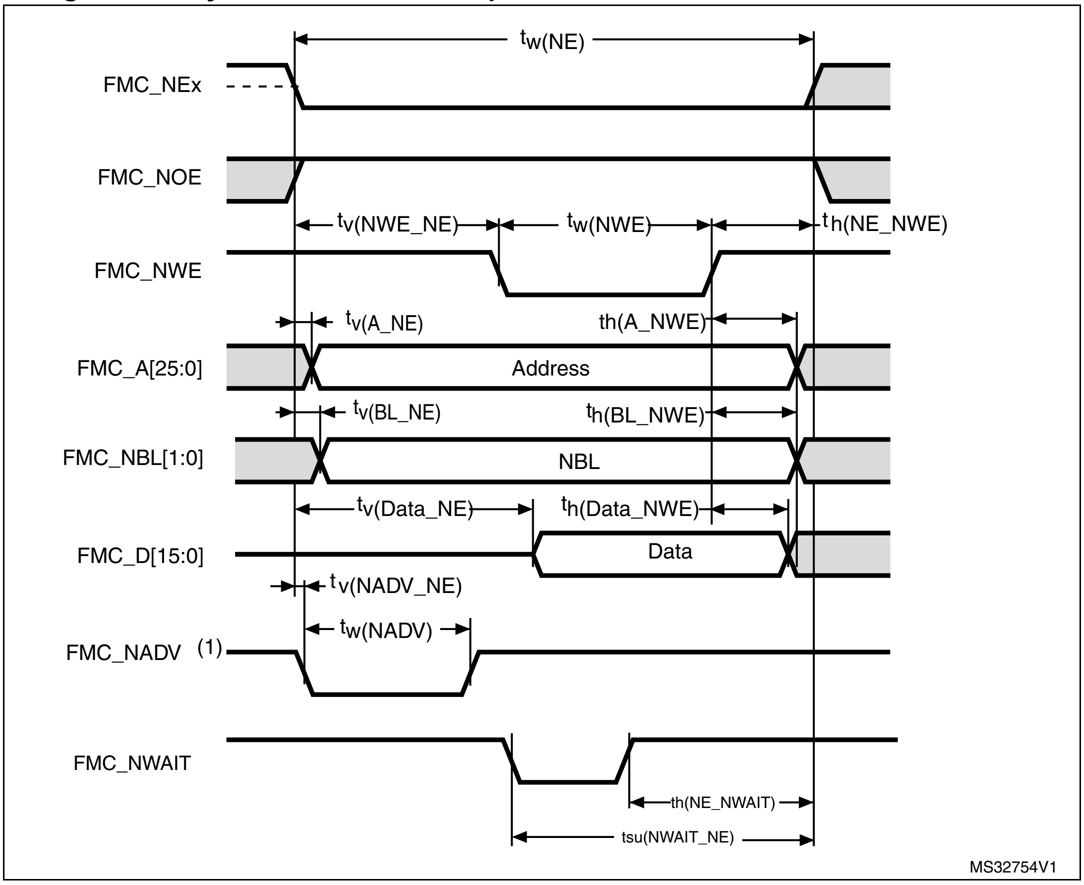


**Figure 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}-0.5$ | $3T_{HCLK}+1.5$ | ns |
| $t_{v(NWE\_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{HCLK}-0.5$ | $T_{HCLK}+1$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $T_{HCLK}-0.5$ | $T_{HCLK}+1$ | |
| $t_{h(NE\_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{HCLK}-0.5$ | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0 | |
| $t_{h(A\_NWE)}$ | Address hold time after FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0 | |
| $t_{h(BL\_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{HCLK}-0.5$ | - | |
| $t_{v(Data\_NE)}$ | Data to FMC_NEx low to Data valid | - | $T_{HCLK}+3$ | |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high | $T_{HCLK}+0.5$ | - | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{HCLK}+0.5$ | |

1. Guaranteed by characterization results.

**Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}-0.5$ | $8T_{HCLK}+1.5$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $6T_{HCLK}-0.5$ | $6T_{HCLK}+1$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $6T_{HCLK}-1$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+2$ | - | |

1. Guaranteed by characterization results.

**Figure 60. Asynchronous multiplexed PSRAM/NOR read waveforms**

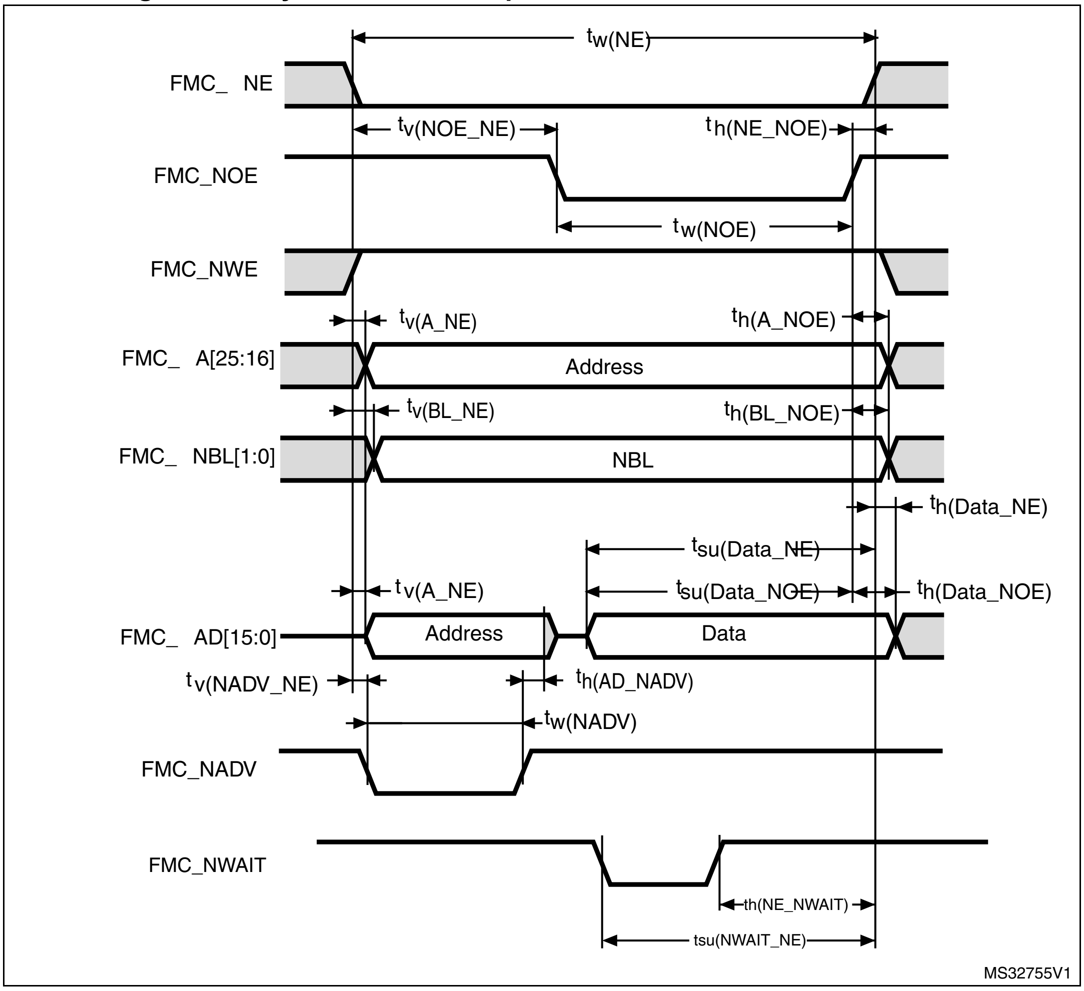


Table 92. Asynchronous multiplexed PSRAM/NOR read timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{HCLK}-0.5$ | $3T_{HCLK}+1.5$ | ns |
| $t_{v(NOE\_NE)}$ | FMC_NEx low to FMC_NOE low | $2T_{HCLK}-1$ | $2T_{HCLK}+0.5$ | |
| $t_{tw(NOE)}$ | FMC_NOE low time | $T_{HCLK}-0.5$ | $T_{HCLK}+0.5$ | |
| $t_{h(NE\_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{HCLK}-0.5$ | $T_{HCLK}+1.5$ | |
| $t_{h(AD\_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high) | 0 | - | |
| $t_{h(A\_NOE)}$ | Address hold time after FMC_NOE high | $T_{HCLK}-0.5$ | - | |
| $t_{h(BL\_NOE)}$ | FMC_BL time after FMC_NOE high | 0 | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | $T_{HCLK}-2$ | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time | $T_{HCLK}-2$ | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. Guaranteed by characterization results.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings[1]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{HCLK}-1$ | $8T_{HCLK}+2$ | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{HCLK}-1$ | $5T_{HCLK}+1$ | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{HCLK}+1.5$ | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{HCLK}+1$ | - | |

1. Guaranteed by characterization results.

**Figure 62. Synchronous multiplexed NOR/PSRAM read timings**

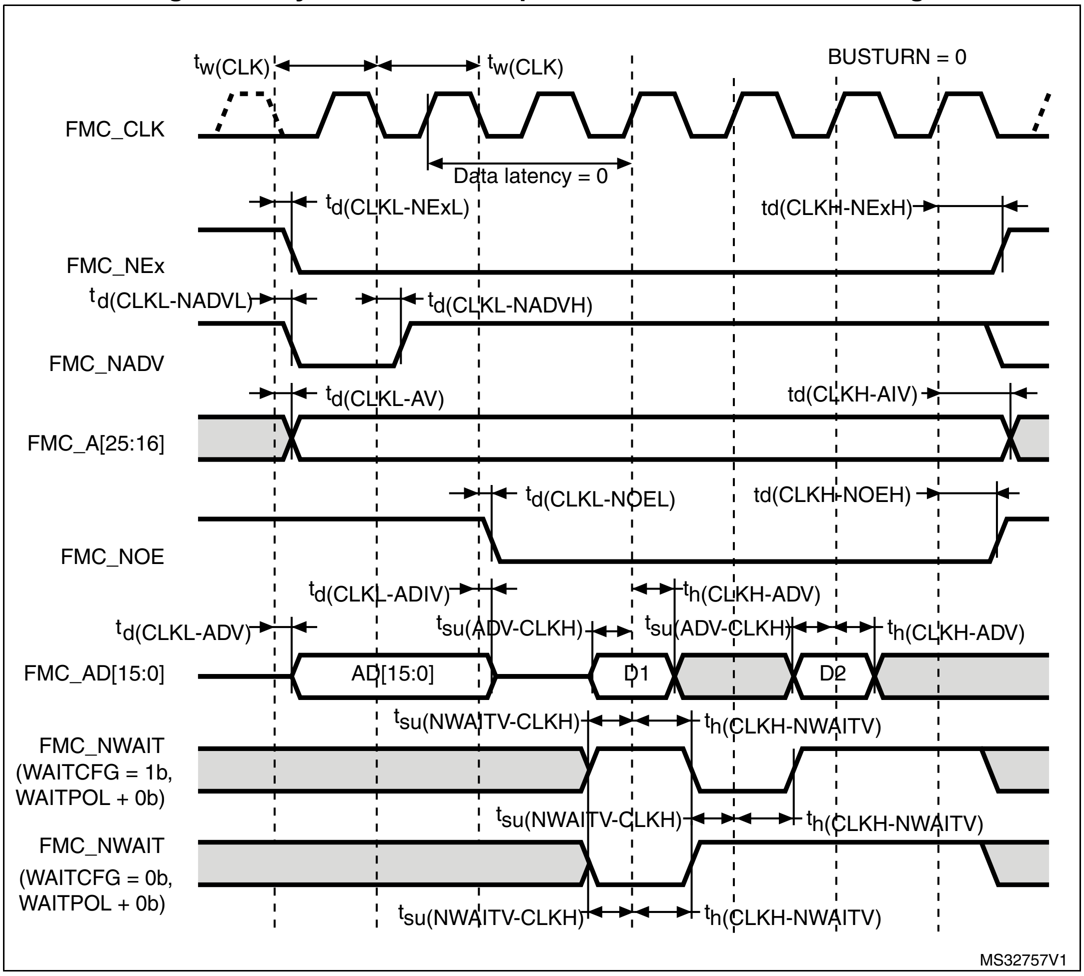


Table 99. Synchronous non-multiplexed PSRAM write timings[(1)]

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{(CLK)}$ | FMC_CLK period | $2T_{HCLK}-1$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2.5 | |
| $t_{(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{HCLK}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | 0 | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{d(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{HCLK}+1$ | - | |
| $t_{d(CLKL-Data)}$ | FMC_D[15:0] valid data after FMC_CLK low | - | 3 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | 1.5 | - | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{HCLK}+0.5$ | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

### NAND controller waveforms and timings

*Figure 66* through *Figure 69* represent synchronous waveforms, and *Table 100* and *Table 101* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

**Figure 75. LCD-TFT horizontal timing diagram**

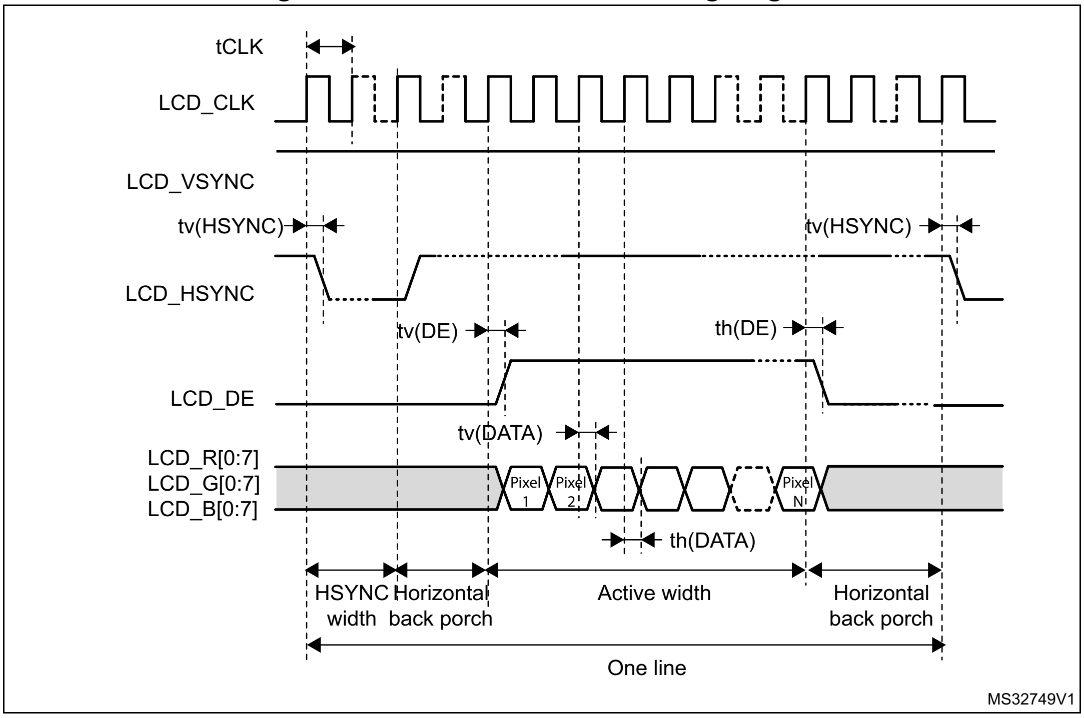



**Figure 76. LCD-TFT vertical timing diagram**

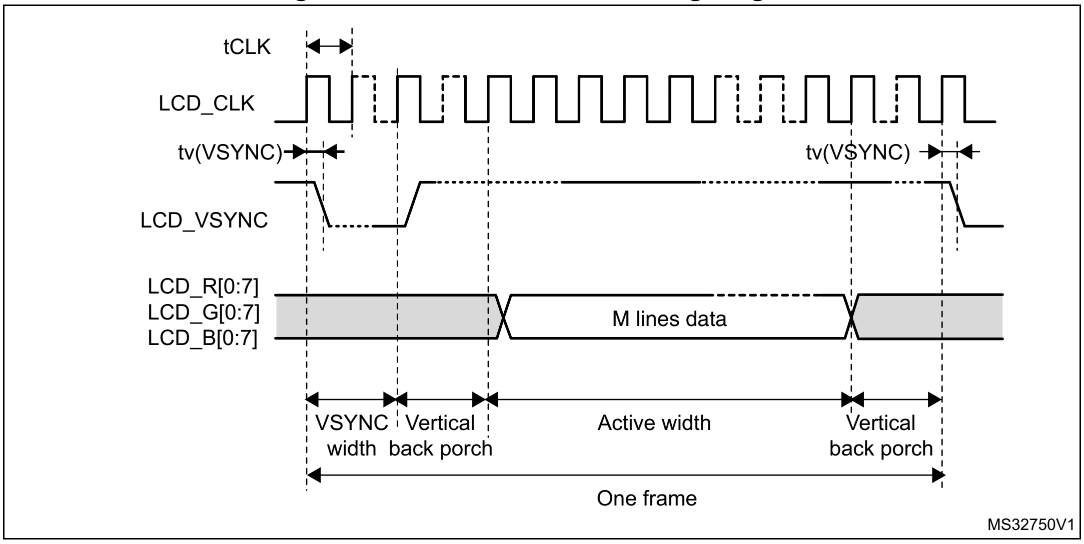


**Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| G | - | 0.900 | - | - | 0.0354 | - |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 101. TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint**

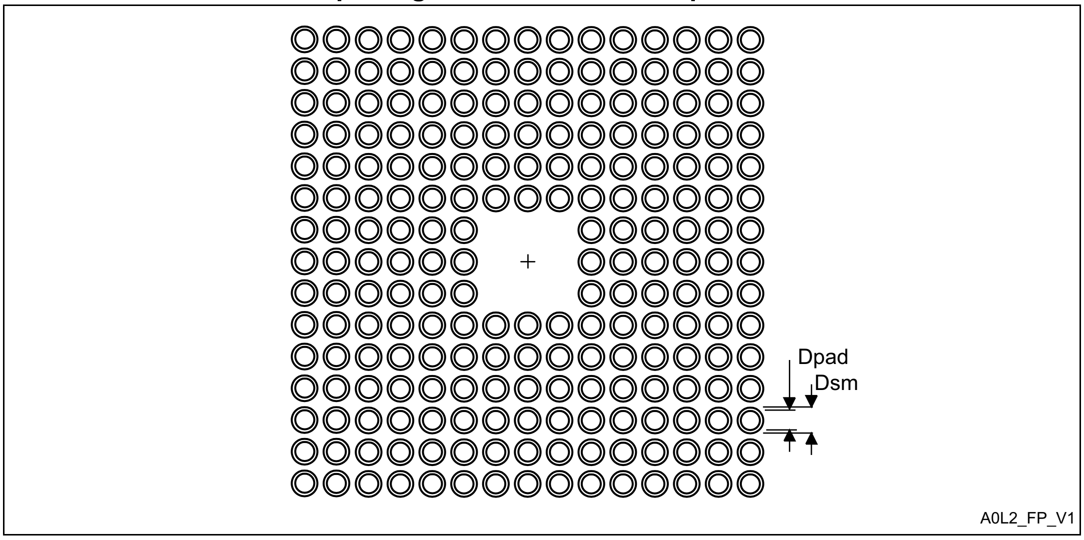



**Table 123. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.8 |
| Dpad | 0.400 mm |
| Dsm | 0.470 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.400 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.120 mm |

# Revision history

**Table 127. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-May-2015 | 1 | Initial release. |
| 20-Oct-2015 | 2 | Updated *Table 53: ESD absolute maximum ratings* adding packages.<br>Updated note of *Table 32: Typical and maximum current consumptions in Standby mode*.<br>Updated *Figure 11: STM32F74xVx LQFP100 pinout* replacing PB13 and PB14 by PE13 and PE14.<br>Updated *Table 51: EMS characteristics* replacing 168 MHz by 216 MHz.<br>Updated *Section 2.9: Quad-SPI memory interface (QUADSPI)* removing ‘STM32F75xx’.<br>Updated *Section 2.22.2: General-purpose timers (TIMx)* and *Section 2.43: Embedded Trace Macrocell™* modifying STM32F756xx by STM32F74xxx.<br>Updated *Section 2.1: ARM® Cortex®-M7 with FPU* modifying STM32F756xx family by STM32F745xx and STM32F746xx devices.<br>Removed Table 86. Ethernet DC electrical characteristics.<br>Updated all the notes removing ‘not tested in production’.<br>Updated *Table 43: Main PLL characteristics*, *Table 44: PLLI2S characteristics* and *Table 45: PLLISAI characteristics* fVCO_OUT output at min value ‘100’ and VCO freq at 100 MHz.<br>Updated *Table 13: STM32F745xx and STM32F746xx register boundary addresses* replacing cortex-M4 by Cortex-M7.<br>Updated *Table 87: Dynamics characteristics: Ethernet MAC signals for MII* td (TXEN) and td (TXD) min value at 6.5 ns. |