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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746vgt6

These features make the STM32F745xx and STM32F746xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

Figure 2 shows the general block diagram of the device family.

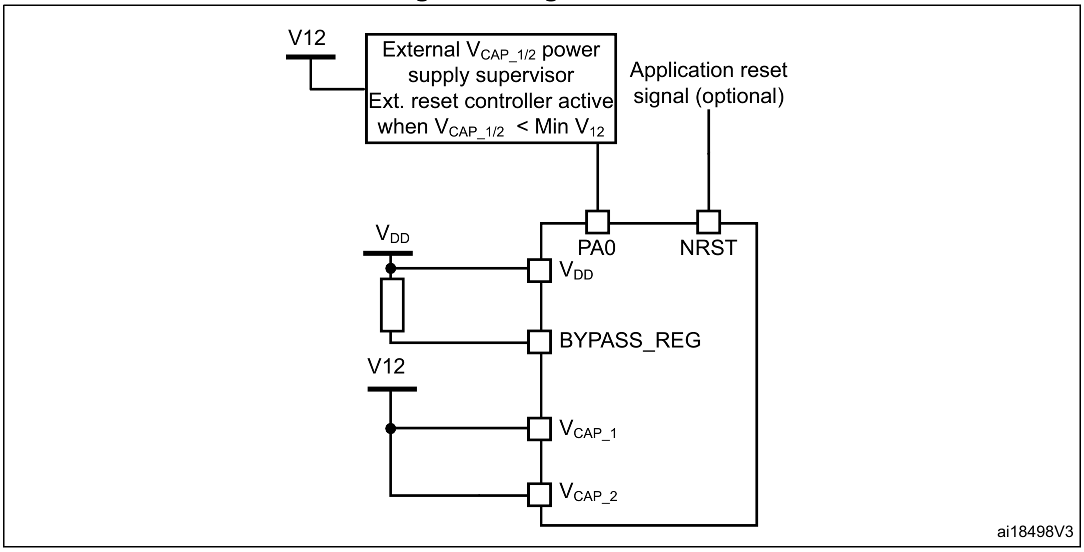
Table 2. STM32F745xx and STM32F746xx features and peripheral counts

Peripherals		STM32F745Vx		STM32F746Vx		STM32F745Zx		STM32F746Zx		STM32F745Ix		STM32F746Ix		STM32F745Bx		STM32F746Bx		STM32F745Nx		STM32F746Nx	
Flash memory in Kbytes		512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024	512	1024
SRAM in Kbytes	System	320(240+16+64)																			
	Instruction	16																			
	Backup	4																			
FMC memory controller		Yes(1)																			
Ethernet		Yes																			
Timers	General-purpose	10																			
	Advanced-control	2																			
	Basic	2																			
	Low-power	1																			
Random number generator		Yes																			

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 8. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

2.23 Inter-integrated circuit interface (I^2C)

The device embeds 4 I2C. Refer to *Table 7: I2C implementation* for the features implementation.

The I^2C bus interface handles communication between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

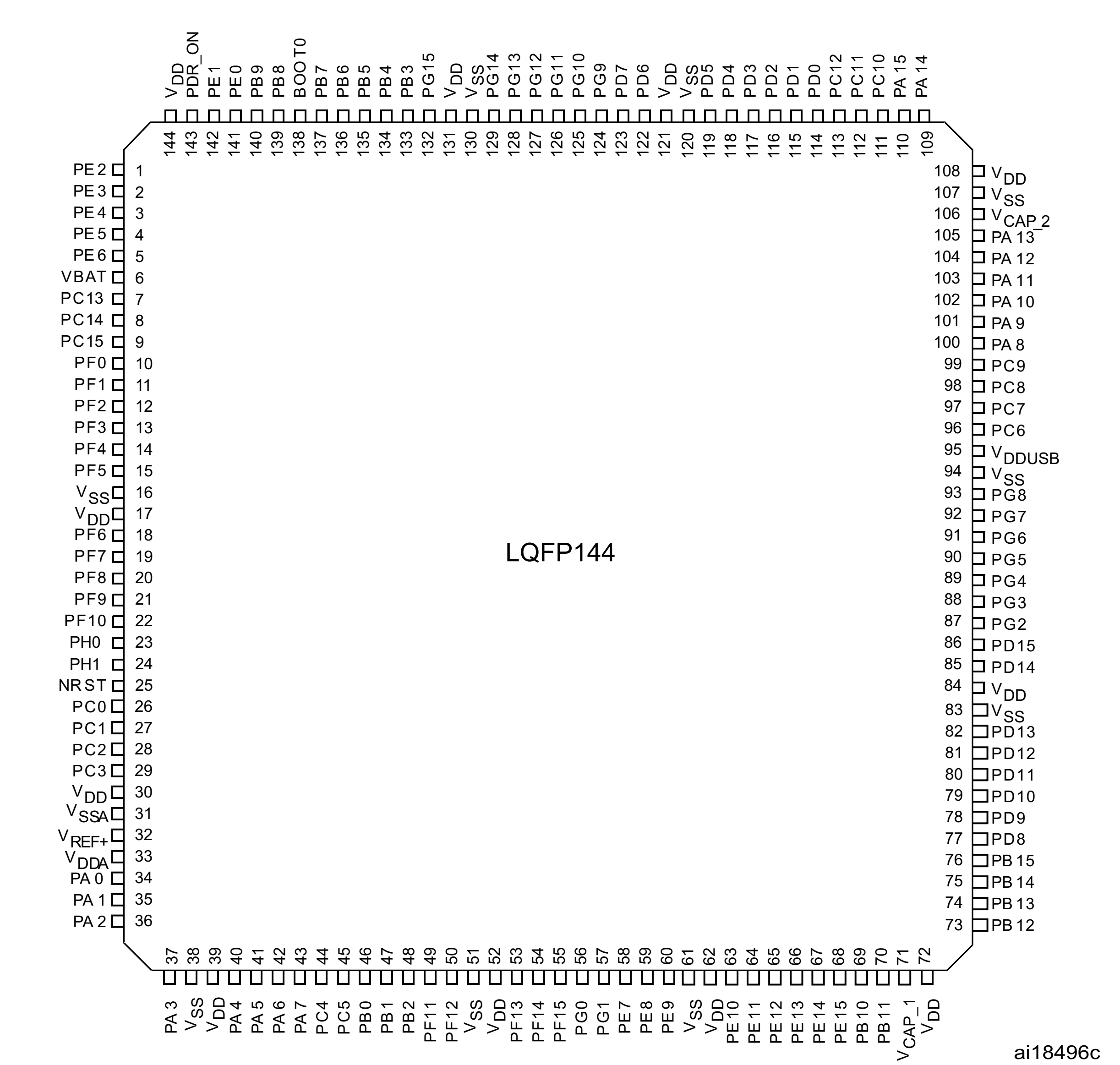
- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features[1]	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X

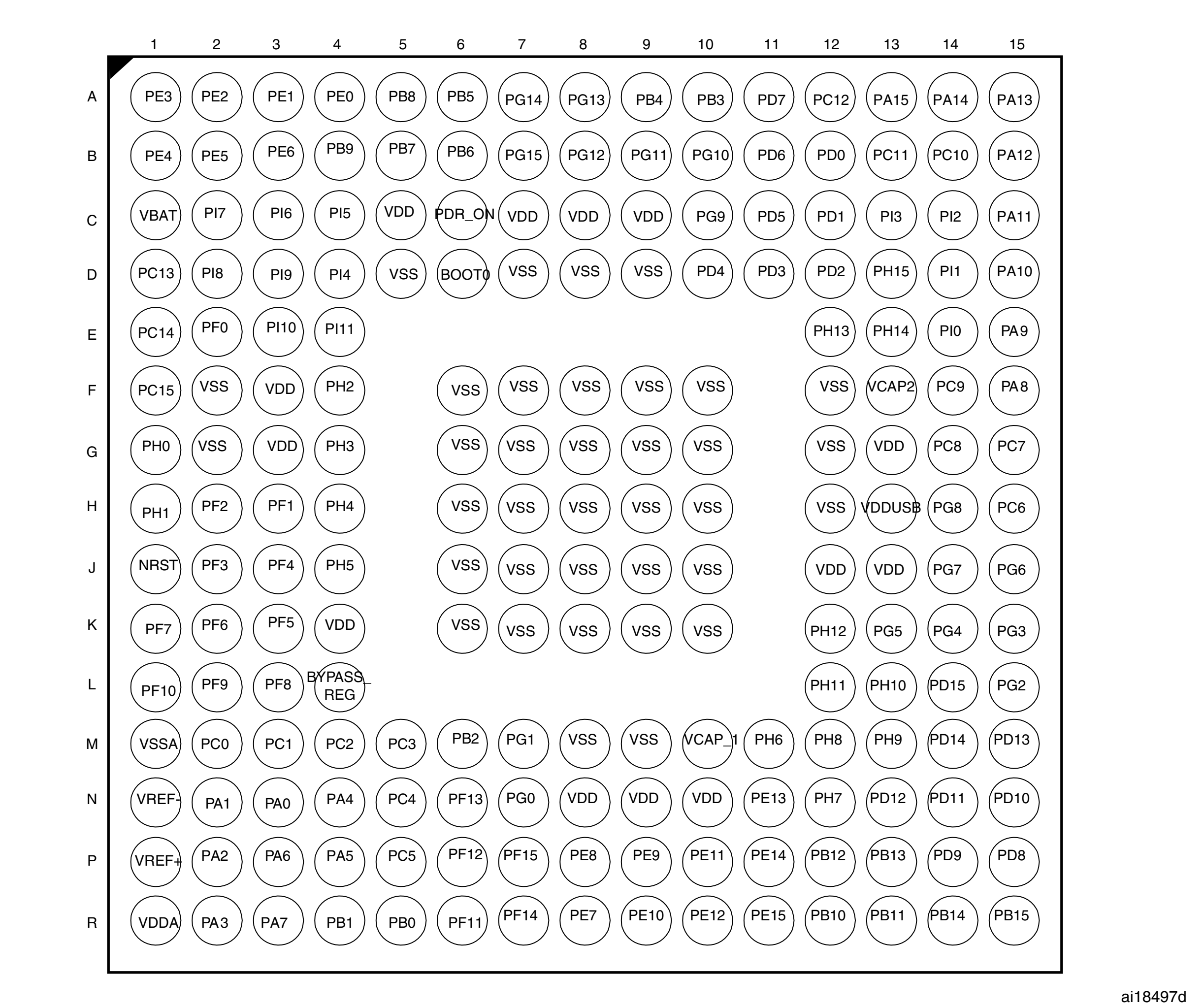
1. X: supported

Figure 14. STM32F74xZx LQFP144 pinout



1. The above figure shows the package top view.

Figure 17. STM32F74xIx UFBGA176 ballout



1. The above figure shows the package top view.

Figure 18. STM32F74xNx TFBGA216 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE4	PE3	PE2	PG14	PE1	PE0	PB8	PB5	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE5	PE6	PG13	PB9	PB7	PB6	PG15	PG11	PJ13	PJ12	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI8	PI4	PK7	PK6	PK5	PG12	PG10	PJ14	PD5	PD3	PD1	PI3	PI2	PA11
D	PC13	PF0	PI5	PI7	PI10	PI6	PK4	PK3	PG9	PJ15	PD4	PD2	PH15	PI1	PA10
E	PC14	PF1	PI12	PI9	PDR_ON	BOOT0	VDD	VDD	VDD	VDD	VCAP_2	PH13	PH14	PI0	PA9
F	PC15	VSS	PI11	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PK1	PK2	PC9	PA8
G	PH0	PF2	PI13	PI15	VDD	VSS				VSS	VDDUSB	PJ11	PK0	PC8	PC7
H	PH1	PF3	PI14	PH4	VDD	VSS				VSS	VDD	PJ8	PJ10	PG8	PC6
J	NRST	PF4	PH5	PH3	VDD	VSS				VSS	VDD	PJ7	PJ9	PG7	PG6
K	PF7	PF6	PF5	PH2	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PJ6	PD15	PB13	PD10
L	PF10	PF9	PF8	PC3	BYPASS-REG	VSS	VDD	VDD	VDD	VDD	VCAP_1	PD14	PB12	PD9	PD8
M	VSSA	PC0	PC1	PC2	PB2	PF12	PG1	PF15	PJ4	PD12	PD13	PG3	PG2	PJ5	PH12
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	PJ3	PE8	PD11	PG5	PG4	PH7	PH9	PH11
P	VREF+	PA2	PA6	PA5	PC5	PF14	PJ2	PF11	PE9	PE11	PE14	PB10	PH6	PH8	PH10
R	VDDA	PA3	PA7	PB1	PB0	PJ0	PJ1	PE7	PE10	PE12	PE15	PE13	PB11	PB14	PB15

MSv41004V1

1. The above figure shows the package top view.

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port E	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	LCD_R7	EVENTOUT
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	-	EVENTOUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	UART7_RTS	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENTOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	UART7_CTS	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENTOUT

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V_{CAP_1}/V_{CAP_2} pins(7)	Max frequency 144 MHz	1.10	1.14	1.20	
		Max frequency 168MHz	1.20	1.26	1.32	
		Max frequency 180 MHz	1.26	1.32	1.38	
V_{IN}	Input voltage on RST and FT pins(8)	$2\ V \leq V_{DD} \leq 3.6\ V$	− 0.3	-	5.5	
		$V_{DD} \leq 2\ V$	− 0.3	-	5.2	
	Input voltage on TTa pins	-	− 0.3	-	V_{DDA}+ 0.3	
	Input voltage on BOOT pin	-	0	-	9	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(9)	LQFP100	-	-	465	mW
		TFBGA100	-	-	351	
		WLCSP143	-	-	641	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	− 40	-	85	°C
		Low power dissipation(10)	− 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	− 40	-	105	°C
		Low power dissipation(10)	− 40	-	125	
TJ	Junction temperature range	6 suffix version	− 40	-	105	°C
		7 suffix version	− 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. 216 MHz maximum frequency for 6 suffix version (200 MHz maximum frequency for 7 suffix version).
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.17.2: Internal reset OFF*).
4. When the ADC is used, refer to *Table 62: ADC characteristics*.
5. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.

Table 19. VCAP1/VCAP2 operating conditions(1)

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 µF V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 21. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

5.3.5 Reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 33. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions(1)	Typ			Max(2)		Unit
			T_A =25 °C			T_A =85 °C	T_A =105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT}= 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC and LSE OFF	0.03	0.03	0.04	0.2	0.4	µA
		Backup SRAM ON, RTC and LSE OFF	0.74	0.75	0.78	3.0	7.0	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	0.40	0.52	0.72	2.8	6.5	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	0.40	0.52	0.72	2.8	6.5	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	0.54	0.64	0.85	3.3	7.6	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	0.62	0.73	0.94	3.6	8.4	
		Backup SRAM ON, RTC ON and LSE in low drive mode	1.06	1.18	1.41	5.4	12.7	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	1.16	1.28	1.51	5.8	13.6	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	1.18	1.3	1.54	5.9	13.8	
		Backup SRAM ON, RTC ON and LSE in High drive mode	1.36	1.48	1.73	6.7	15.5	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

Table 38. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 30. High-speed external clock source AC timing diagram

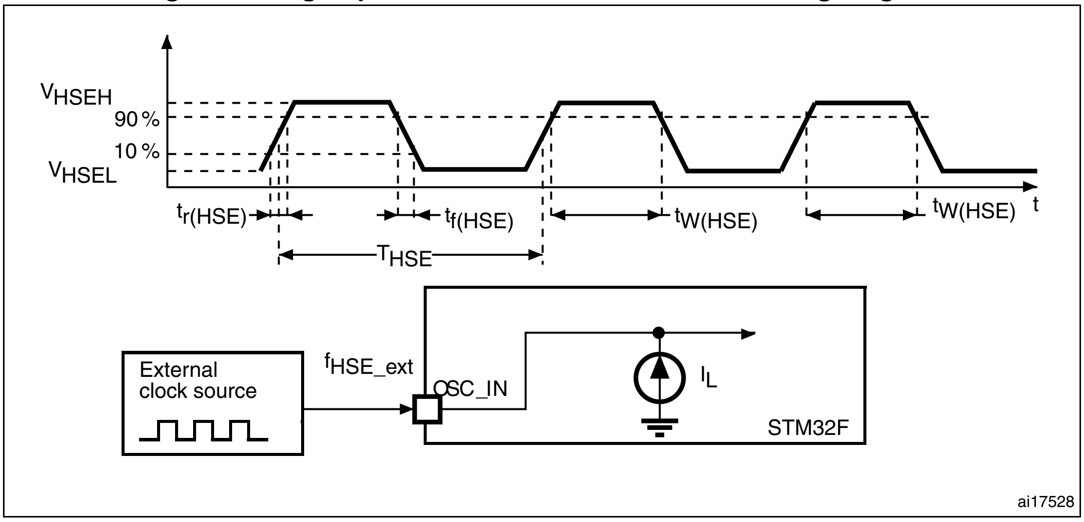
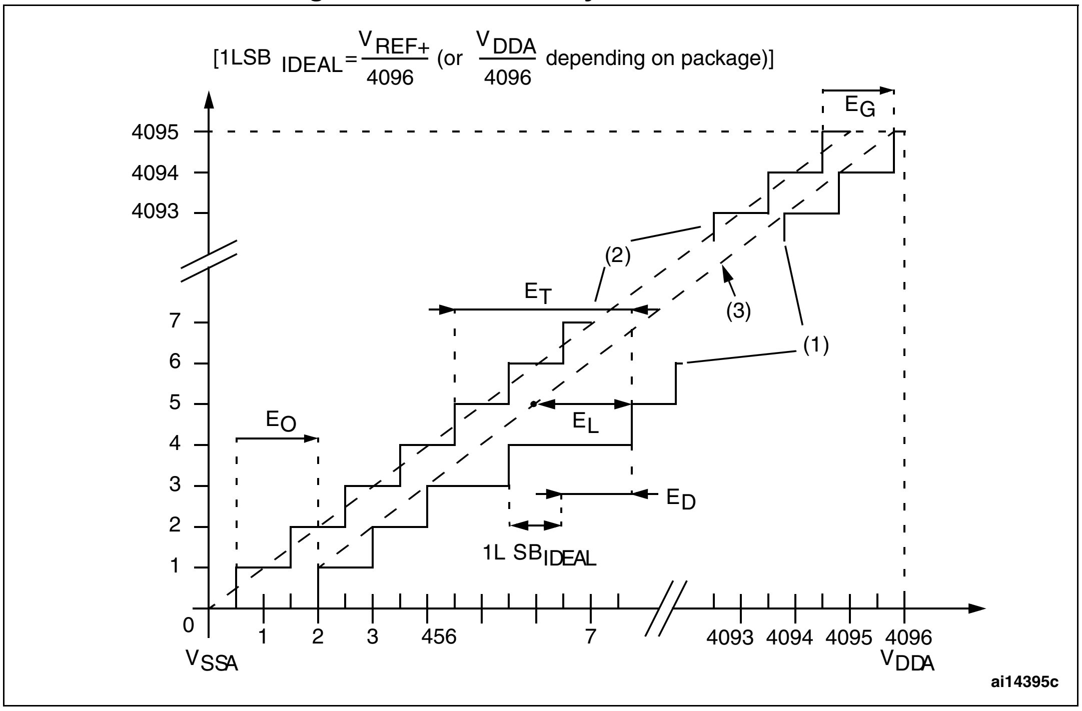
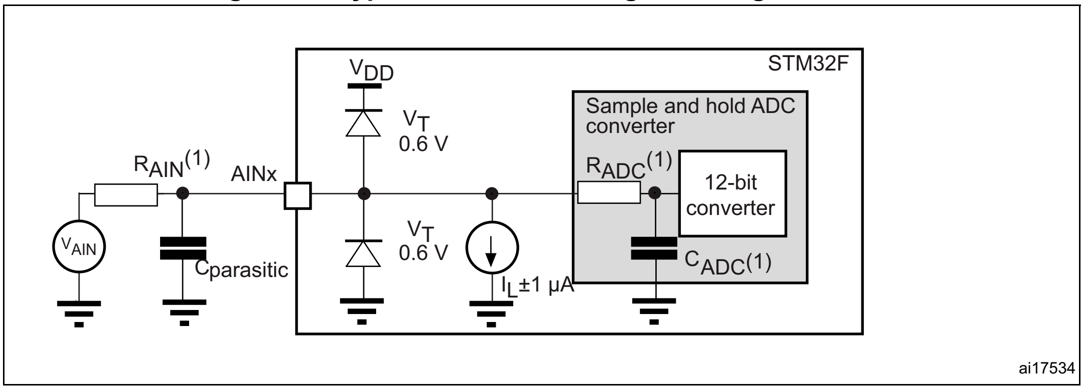


Figure 41. ADC accuracy characteristics



1. See also *Table 64*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 42. Typical connection diagram using the ADC



1. Refer to *Table 62* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

5.3.22 Temperature sensor characteristics

Table 68. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 69. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FF0 F44C - 0x1FF0 F44D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FF0 F44E - 0x1FF0 F44F

5.3.23 V_{BAT} monitoring characteristics

Table 70. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

5.3.24 Reference voltage

The parameters given in *Table 71* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 71. internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Figure 47. SPI timing diagram - slave mode and CPHA = 1

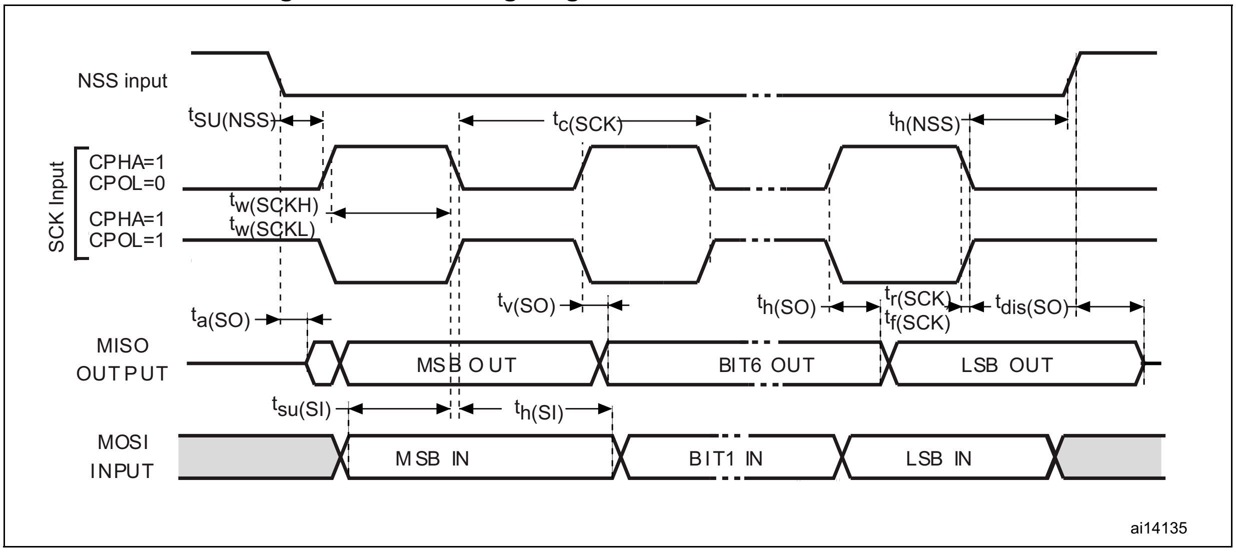
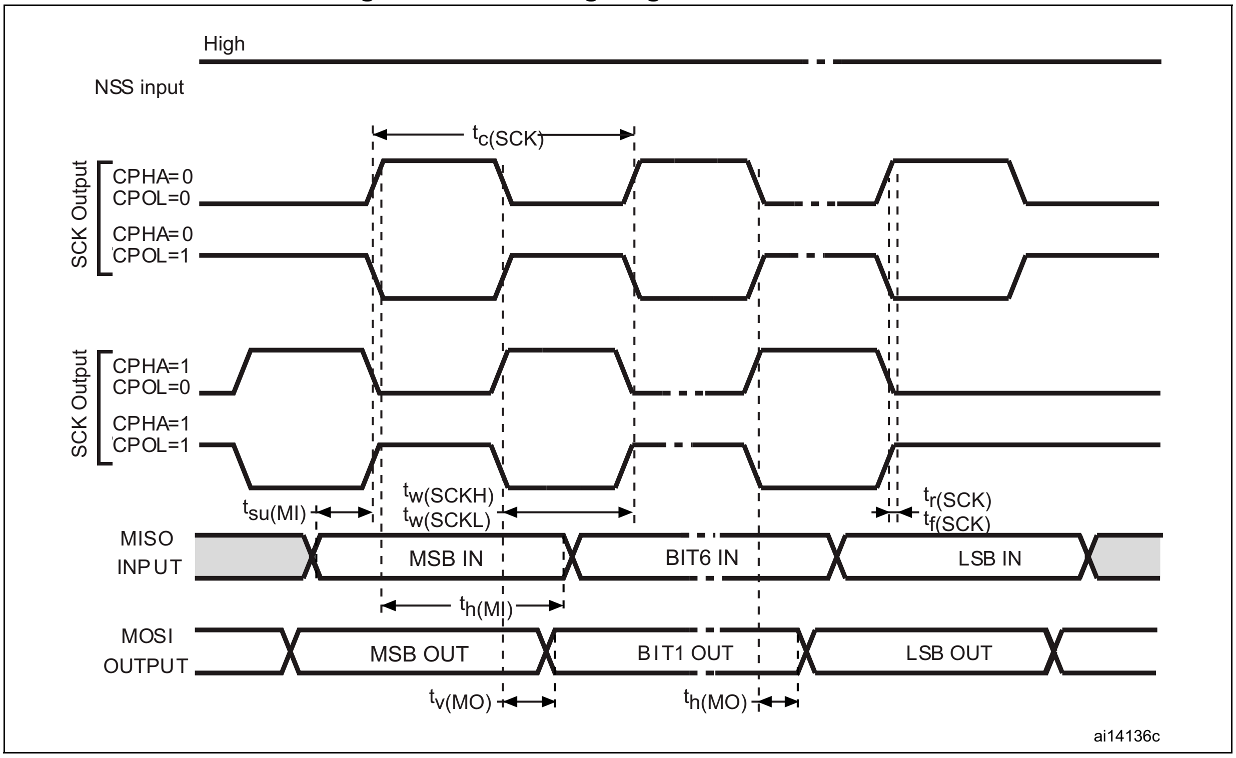


Figure 48. SPI timing diagram - master mode



I^2S interface characteristics

Unless otherwise specified, the parameters given in *Table 77* for the I^2S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Table 96. Synchronous multiplexed NOR/PSRAM read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}-0.5$	-	ns
$t_{d(CLKL\text{-}NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK}+0.5$	-	
$t_{d(CLKL\text{-}NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL\text{-}NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL\text{-}AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH\text{-}AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL\text{-}NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH\text{-}NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK}-0.5$	-	
$t_{d(CLKL\text{-}ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL\text{-}ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV\text{-}CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_{h(CLKH\text{-}ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT\text{-}CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH\text{-}NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 70. SDRAM read access waveforms (CL = 1)

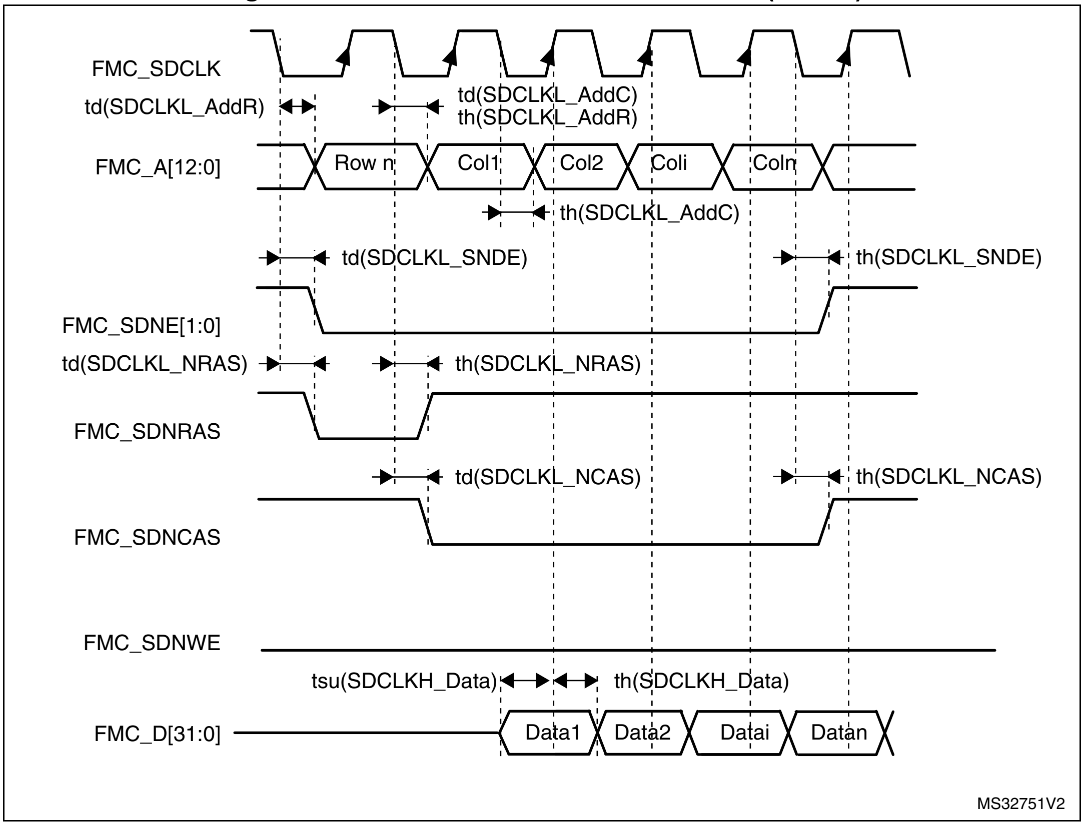


Figure 72. Quad-SPI timing diagram - SDR mode

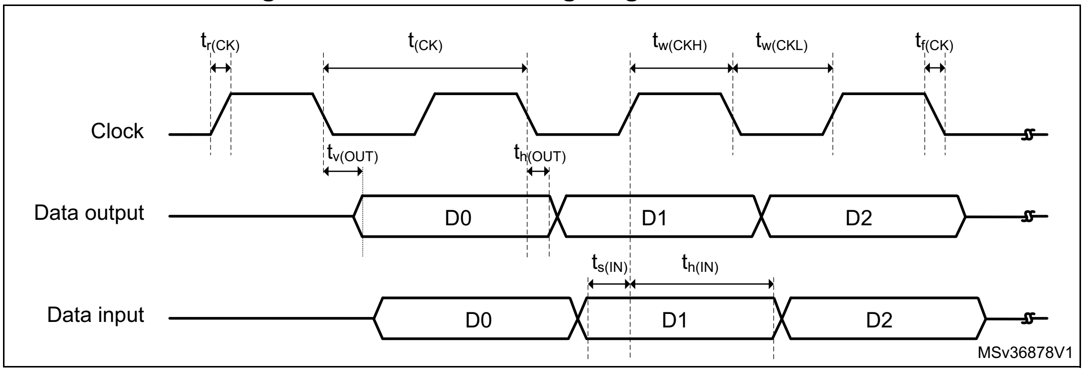
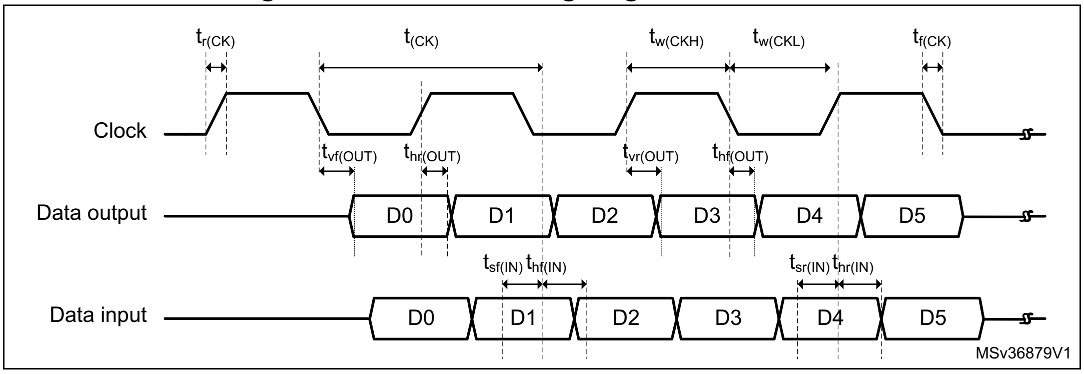


Figure 73. Quad-SPI timing diagram - DDR mode



5.3.29 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 108* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 17*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits

Table 108. DCMI characteristics[1]

Symbol	Parameter	Min	Max	Unit
-	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	54	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	3.5	-	ns
$t_{h(DATA)}$	Data input hold time	0	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	2.5	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	0	-	

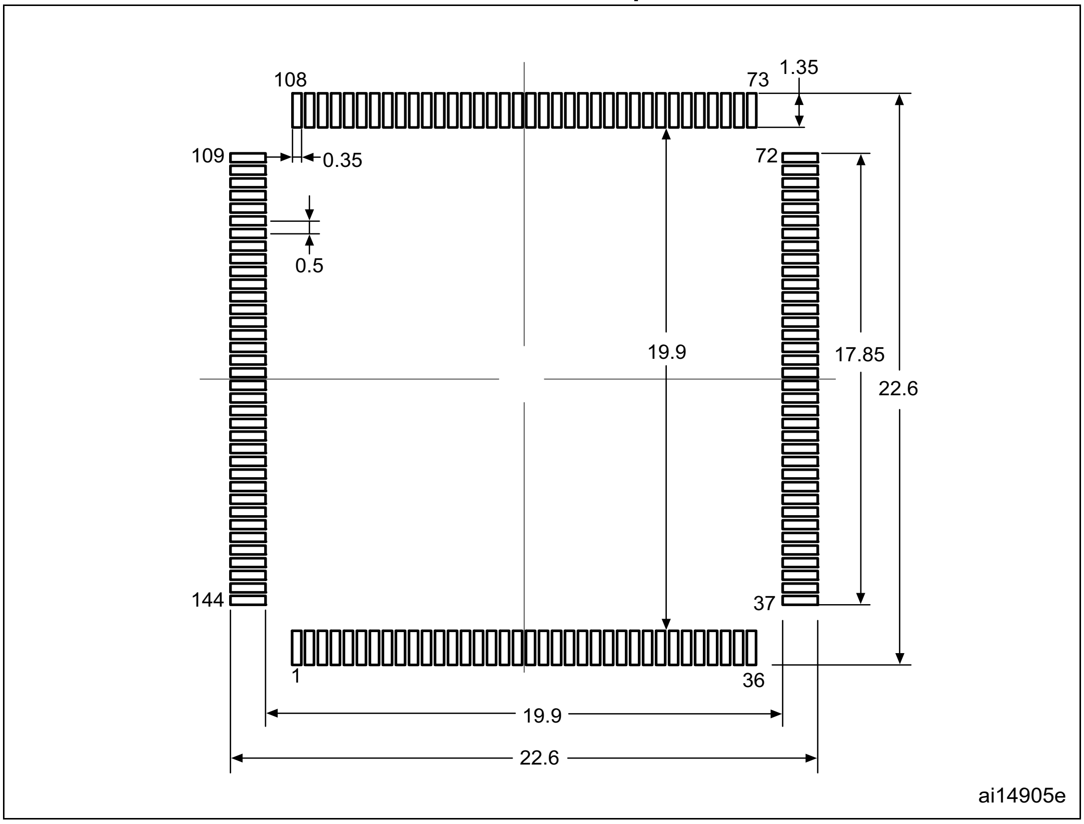
1. Guaranteed by characterization results.

Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 89. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 101. TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint

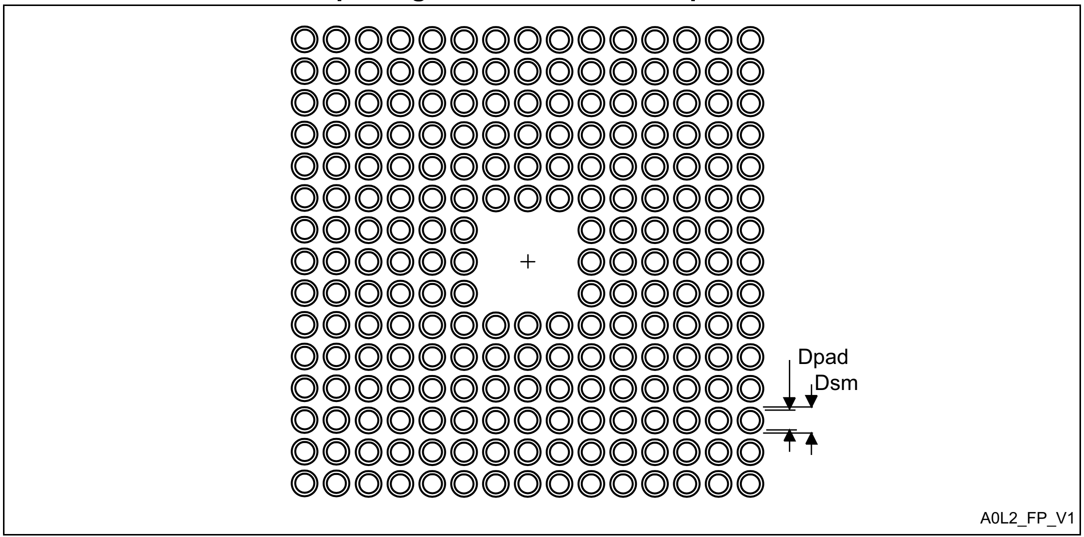


Table 123. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm