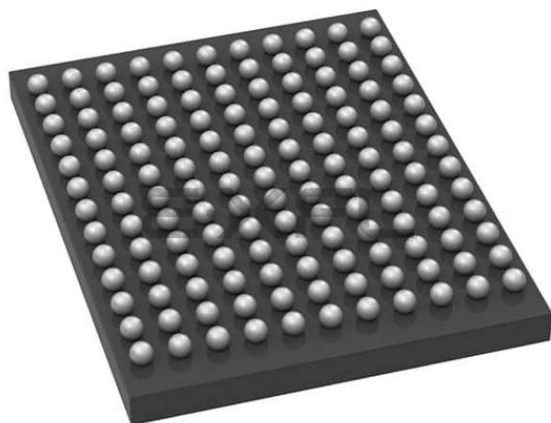




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	143-UFBGA, WLCSP
Supplier Device Package	143-WLCSP (4.54x5.85)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746zey6tr

Pin	Signal	Signal	Pin
1	PE2	156	PI2
2	PE3	155	PI1
3	PE4	154	PI0
4	PE5	153	PH15
5	PE6	152	PH14
6	VBAT	151	PH13
7	PI8	150	VDD
8	PC13	149	VSS
9	PC14	148	VCAP_2
10	PC15	147	PA13
11	PI9	146	PA12
12	PI10	145	PA11
13	PI11	144	PA10
14	VSS	143	PA9
15	VDD	142	PA8
16	PF0	141	PC9
17	PF1	140	PC8
18	PF2	139	PC7
19	PI12	138	PC6
20	PI13	137	VDDUSB
21	PI14	136	VSS
22	PF3	135	PG8
23	PF4	134	PG7
24	PF5	133	PG6
25	VSS	132	PG5
26	VDD	131	PG4
27	PF6	130	PG3
28	PF7	129	PG2
29	PF8	128	PK2
30	PF9	127	PK1
31	PF10	126	PK0
32	PH0	125	VSS
33	PH1	124	VDD
34	NRST	123	PI11
35	PC0	122	PI10
36	PC1	121	PI9
37	PC2	120	PI8
38	PC3	119	PI7
39	VDD	118	PI6
40	VSSA	117	PD15
41	VREF+	116	PD14
42	VDDA	115	VDD
43	PA0	114	VSS
44	PA1	113	PD13
45	PA2	112	PD12
46	PH2	111	PD11
47	PH3	110	PD10
48	PH4	109	PD9
49	PH5	108	PD8
50	PA3	107	PB15
51	VSS	106	PB14
52	VDD	105	PB13

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Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F745xx and STM32F746xx pin and ball definition

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
1	A3	D8	1	A2	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	B3	C10	2	A1	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
3	C3	B11	3	B1	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	-	-	N12	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	-	-	M12	85	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNCR, LCD_R2, EVENTOUT	-
-	-	-	-	M13	86	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	-	-	L13	87	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	-	-	L12	88	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	-	-	K12	89	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	-	H12	90	-	K10	VSS	S	-	-	-	-
-	-	-	-	J12	91	103	K11	VDD	S	-	-	-	-
51	K8	M2	73	P12	92	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	J8	N1	74	P13	93	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	E5	124	C10	152	178	D9	PG9	I/O	FT	-	SPDIFRX_IN3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	-	C6	125	B10	153	179	C8	PG10	I/O	FT	-	LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	--	B6	126	B9	154	180	B8	PG11	I/O	FT	-	SPDIFRX_IN0, ETH_MII_TX_EN/ETH_R MII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	-	A6	127	B8	155	181	C7	PG12	I/O	FT	-	LPTIM1_IN1, SPI6_MISO, SPDIFRX_IN1, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	D6	128	A8	156	182	B3	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RM II_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	-	F6	129	A7	157	183	A4	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RM II_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	-	-	130	D7	158	184	F7	VSS	S	-	-	-	-
-	-	E6	131	C7	159	185	E8	VDD	S	-	-	-	-

Table 13. STM32F745xx and STM32F746xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4000 8000 - 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I _{DD}	Supply current in RUN mode	All peripherals enabled ⁽²⁾⁽³⁾	216	205	237	261	-	mA
			200	191	219	241	260	
			180	176	202	218	232	
			168	158	181	196	209	
			144	130	148	161	172	
			60	58	67	79	89	
			25	27	32	43	54	
		All peripherals disabled ⁽³⁾	216	130	149	173	-	
			200	121	138	160	179	
			180	113	129	145	159	
			168	102	116	131	144	
			144	88	100	112	123	
			60	40	45	57	68	
			25	19	22	33	44	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 35. Peripheral current consumption

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 216 MHz)	GPIOA	2.2	2.1	1.9	μA/MHz
	GPIOB	2.1	1.8	1.7	
	GPIOC	2.3	2.0	1.9	
	GPIOD	2.2	1.9	1.8	
	GPIOE	2.2	1.9	1.8	
	GPIOF	2.2	1.9	1.8	
	GPIOG	2.1	1.8	1.7	
	GPIOH	2.0	1.7	1.7	
	GPIOI	2.3	2.0	1.7	
	GPIOJ	2.2	1.9	1.7	
	GPIOK	2.0	1.7	1.7	
	CRC	1.0	0.9	0.8	
	BKPSRAM	0.8	0.7	0.6	
	DMA1	2.7 x N + 5.1	2.6 x N + 4.7	2.2 x N + 4	
	DMA2	2.2 x N + 4.9	2.6 x N + 4.4	2.2 x N + 4.1	
	DMA2D	87.1	82.5	69.6	
	ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	42.1	39.7	34.1	
OTG_HS	57.5	54.4	47.6		
OTG_HS+ULPI					
AHB2 (up to 216 MHz)	DCMI	5.1	4.7	4.0	μA/MHz
	RNG	2.8	2.4	2.3	
	USB_OTG_FS	31.8	29.9	25.8	
AHB3 (up to 216 MHz)	FMC	18.9	17.7	15.2	μA/MHz
	QSPI	23.2	21.8	18.5	
Bus matrix ⁽²⁾		21.06	20.3	17.2	μA/MHz

5.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 36](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3$ V.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	13	13	CPU clock cycles
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	μs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
$t_{WUSTDBY}^{(2)}$	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.

2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 43. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter ⁽³⁾	Cycle-to-cycle jitter	System clock 216 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
	Main clock output (MCO) for RMII Ethernet	Cycle to cycle at 50 MHz on 1000 samples		-	32	-	
	Main clock output (MCO) for MII Ethernet	Cycle to cycle at 25 MHz on 1000 samples		-	40	-	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples		-	330	-	
I _{DD(PLL)} ⁽⁴⁾	PLL power consumption on V _{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
I _{DDA(PLL)} ⁽⁴⁾	PLL power consumption on V _{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 44. PLLI2S characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{PLLI2S_IN}}$	PLLI2S input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10	MHz
$f_{\text{PLLI2SP_OUT}}$	PLLI2S multiplier output clock for SPDIFRX	-	-	-	216	
$f_{\text{PLLI2SQ_OUT}}$	PLLI2S multiplier output clock for SAI	-	-	-	216	
$f_{\text{PLLI2SR_OUT}}$	PLLI2S multiplier output clock for I2S	-	-	-	216	
$f_{\text{VCO_OUT}}$	PLLI2S VCO output	-	100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times \text{md} \times \text{PLLN}] / (100 \times 5 \times \text{MODEPER})$$

$f_{\text{VCO_OUT}}$ must be expressed in MHz.

With a modulation depth (md) = $\pm 2\%$ (4 % peak to peak), and PLLN = 240 (in MHz):

$$\text{INCSTEP} = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126 \text{md}(\text{quantitized})\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$\text{md}_{\text{quantized}}\% = (\text{MODEPER} \times \text{INCSTEP} \times 100 \times 5) / ((2^{15} - 1) \times \text{PLLN})$$

As a result:

$$\text{md}_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

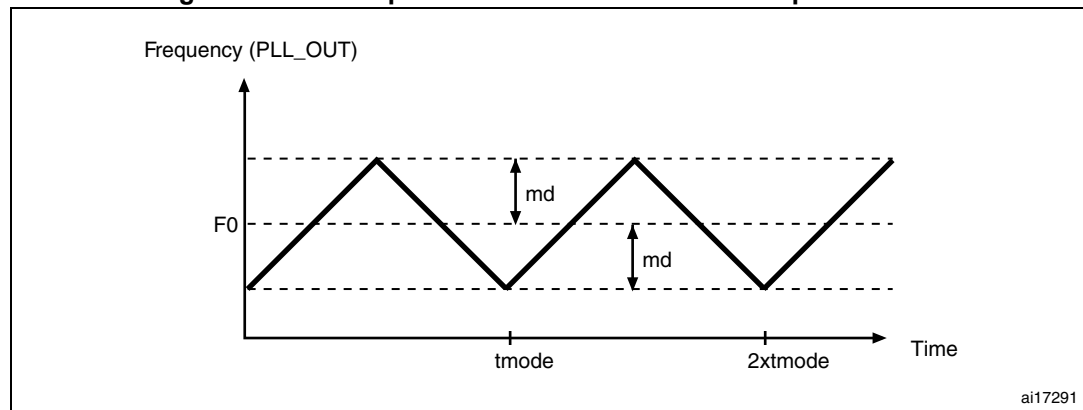
[Figure 36](#) and [Figure 37](#) show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{\text{PLL_OUT}}$ nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 36. PLL output clock waveforms in center spread mode



Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 52. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{HSE}/f_{CPU}]$	Unit
				25/200 MHz	
S _{EMI}	Peak level	V _{DD} = 3.6 V, T _A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache OFF, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	- 4	dBμV
			30 to 130 MHz	9	
			130 MHz to 1GHz	11	
			EMI Level	3	-
		V _{DD} = 3.6 V, T _A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	4	dBμV
			30 to 130 MHz	5	
			130 MHz to 1GHz	14	
			EMI level	3	-
		V _{DD} = 3.6 V, T _A = 25 °C, TFBGA216 package, conforming to IEC61967-2 ART/L1-cache ON, over-drive ON, all peripheral clocks enabled, clock dithering enabled.	0.1 to 30 MHz	- 9	dBμV
			30 to 130 MHz	-7	
			130 MHz to 1GHz	-5	
			EMI level	1.5	-

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 39](#) and [Table 58](#), respectively.

Unless otherwise specified, the parameters given in [Table 58](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 58. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	4	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	3	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V to}$ 3.6 V	-	-	100	ns
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	25	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	12.5	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	12.5	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	10	ns
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	50 ⁽⁴⁾	MHz
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	100 ⁽⁴⁾	
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	25	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.8 \text{ V}$	-	-	50	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	42.5	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	6	ns
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	4	
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6	

Figure 47. SPI timing diagram - slave mode and CPHA = 1

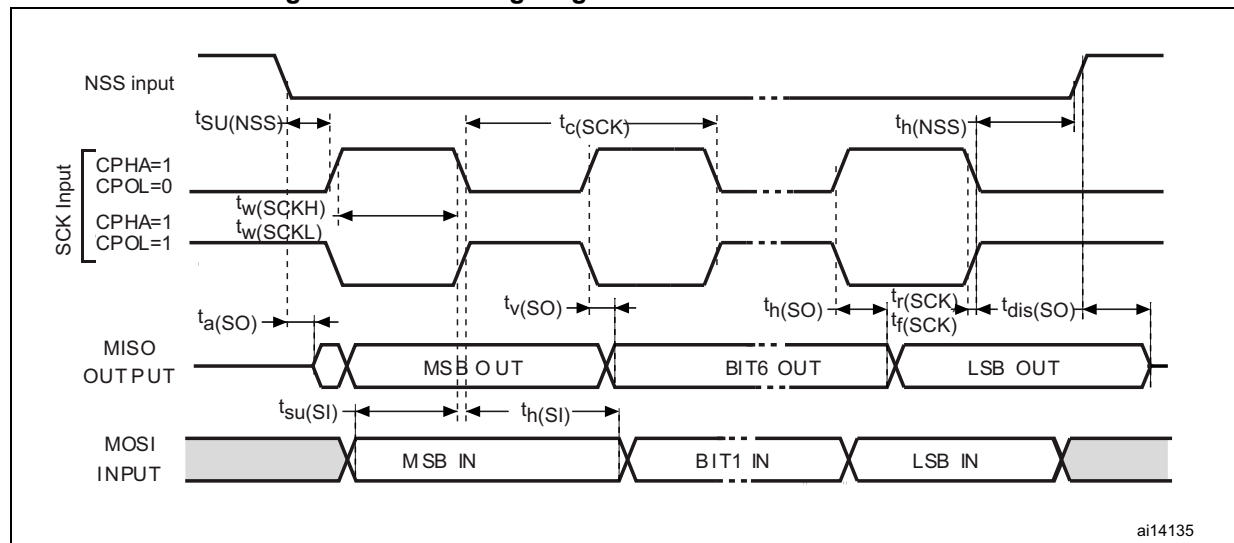
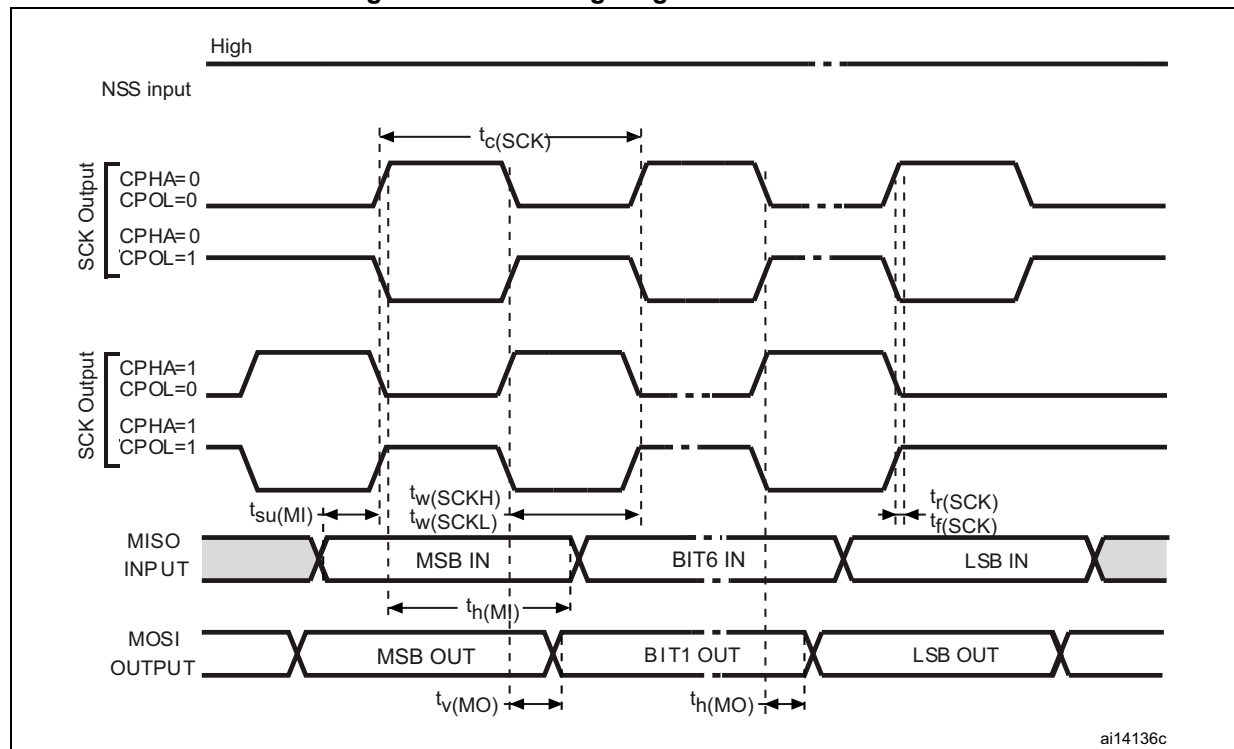


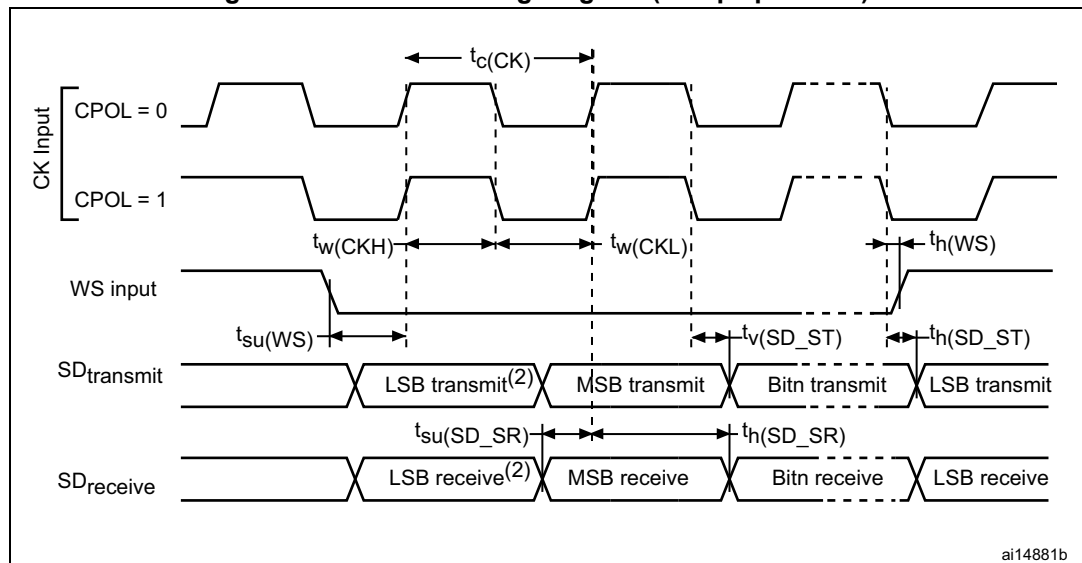
Figure 48. SPI timing diagram - master mode



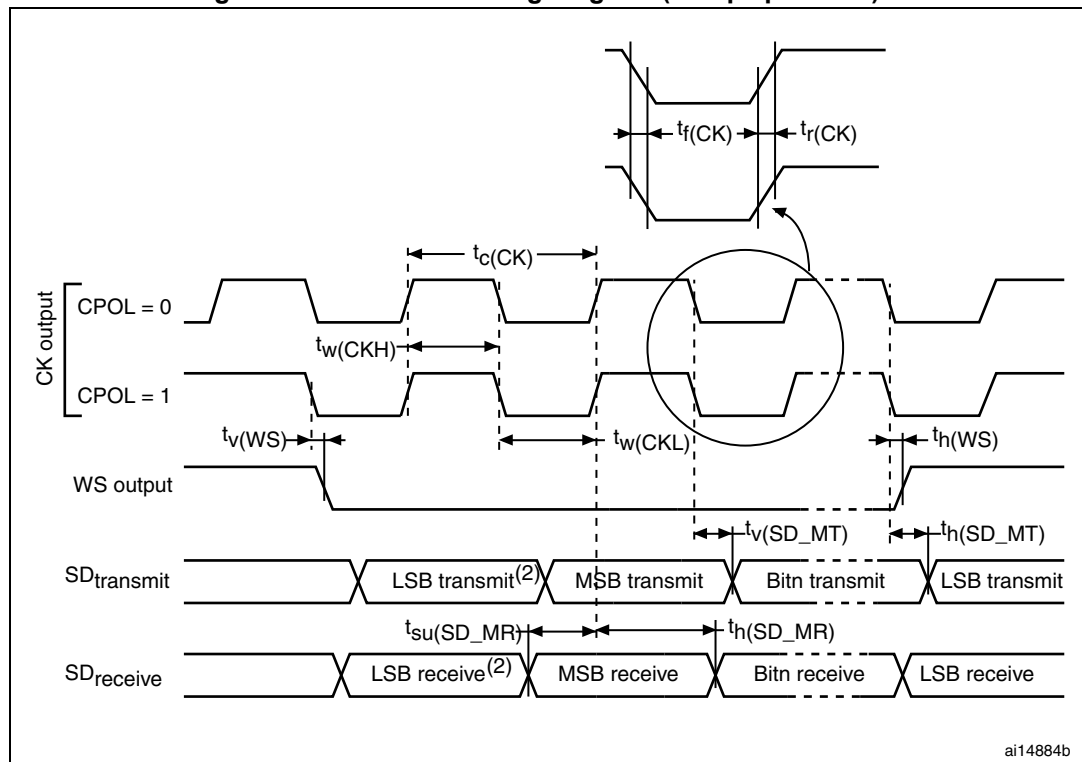
I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 77](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Figure 49. I²S slave timing diagram (Philips protocol)⁽¹⁾

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 50. I²S master timing diagram (Philips protocol)⁽¹⁾

1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 96. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}-0.5$	-	ns
$t_{d(CLKL-NEXL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NEXH)}$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{HCLK}+0.5$	-	
$t_{d(CLKL-NADV L)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADV H)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16...25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{HCLK}-0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1.5	-	
$t_h(CLKH-ADV)$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_h(CLKH-NWAIT)$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

Table 99. Synchronous non-multiplexed PSRAM write timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{CLK}	FMC_CLK period	$2T_{\text{HCLK}}-1$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{\text{d}}(\text{CLKH-NExH})$	FMC_CLK high to FMC_NEx high (x= 0...2)	$T_{\text{HCLK}}+0.5$	-	
$t_{\text{d}}(\text{CLKL-NADV})$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{\text{d}}(\text{CLKL-NADVH})$	FMC_CLK low to FMC_NADV high	0	-	
$t_{\text{d}}(\text{CLKL-AV})$	FMC_CLK low to FMC_Ax valid (x=16...25)	-	2.5	
$t_{\text{d}}(\text{CLKH-AIV})$	FMC_CLK high to FMC_Ax invalid (x=16...25)	0	-	
$t_{\text{d}}(\text{CLKL-NWEL})$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{\text{d}}(\text{CLKH-NWEH})$	FMC_CLK high to FMC_NWE high	$T_{\text{HCLK}}+1$	-	
$t_{\text{d}}(\text{CLKL-Data})$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{\text{d}}(\text{CLKL-NBLL})$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{\text{d}}(\text{CLKH-NBLH})$	FMC_CLK high to FMC_NBL high	$T_{\text{HCLK}}+0.5$	-	
$t_{\text{su}}(\text{NWAIT-CLKH})$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{\text{h}}(\text{CLKH-NWAIT})$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 66 through Figure 69 represent synchronous waveforms, and Table 100 and Table 101 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Table 102. SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3.5	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	4	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

Table 103. LPSPDR SDRAM read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{HCLK}-0.5$	$2T_{HCLK}+0.5$	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLKH_Data)}$	Data input hold time	1.5	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	3.5	
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	0.5	
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL_SDNRAS)}$	SDNRAS valid time	-	0.5	
$t_{h(SDCLKL_SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL_SDNCAS)}$	SDNCAS valid time	-	0.5	
$t_{h(SDCLKL_SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

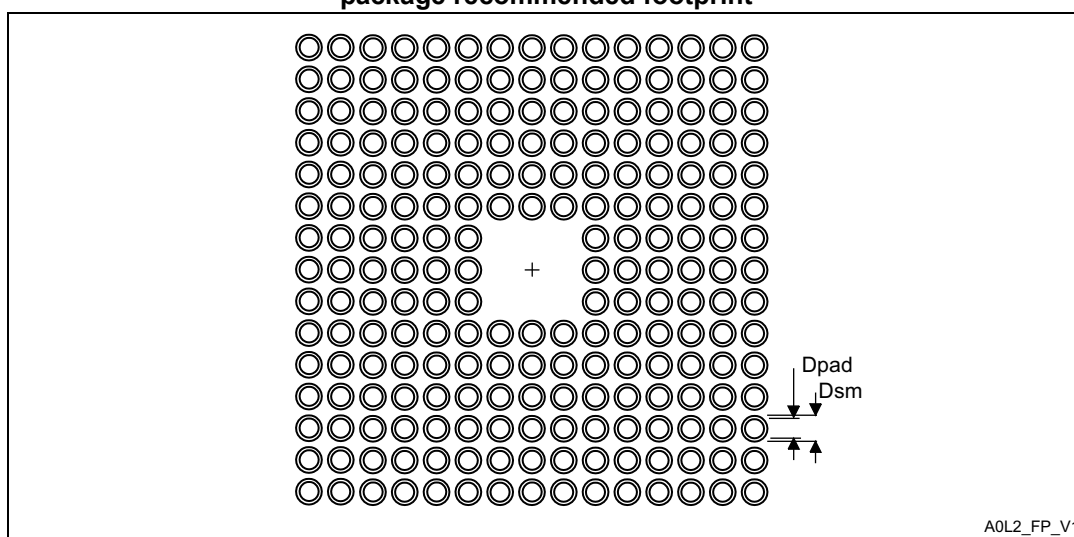
Technical drawing of a square plate with dimensions and labels. The overall dimensions are 26.7 by 26.7. The inner square area is 21.8 by 21.8. The plate has a central square hole with a diameter of 176. The plate is divided into four quadrants by a vertical and a horizontal centerline. The labels 1, 176, 133, 132, 0.5, 0.3, 44, 45, 89, 88, and 1.2 are present. The labels 1, 176, 133, 132, 0.5, 0.3, 44, 45, 89, 88, and 1.2 are present.

1. Dimensions are expressed in millimeters.

Table 122. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 101. TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package recommended footprint**Table 123. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD} .
- The over-drive mode is not supported.

A.1 Operating conditions

Table 126. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to $2.1 V^{(3)}$	Conversion time up to 1.2 Msps	20 MHz	180 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 2.17.1: Internal reset ON](#)).