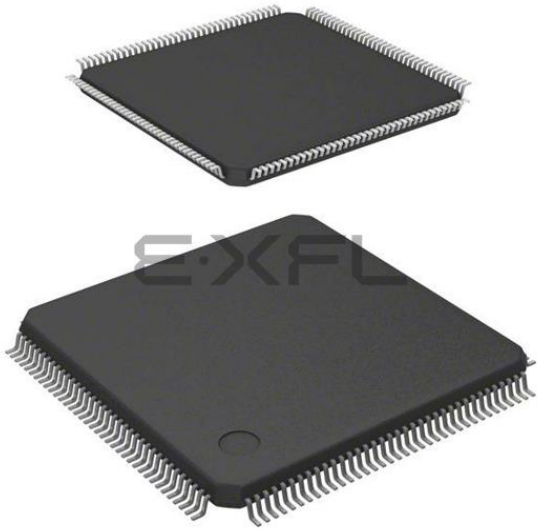

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SAI, SD, SPDIF-Rx, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f746zgt6e

consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

– In Stop modes

The MR can be configured in two ways during Stop mode:

MR operates in normal mode (default mode of MR in Stop mode)

MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during Stop mode:

  – LPR operates in normal mode (default mode when LPR is ON)

  – LPR operates in under-drive mode (reduced leakage mode).

- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

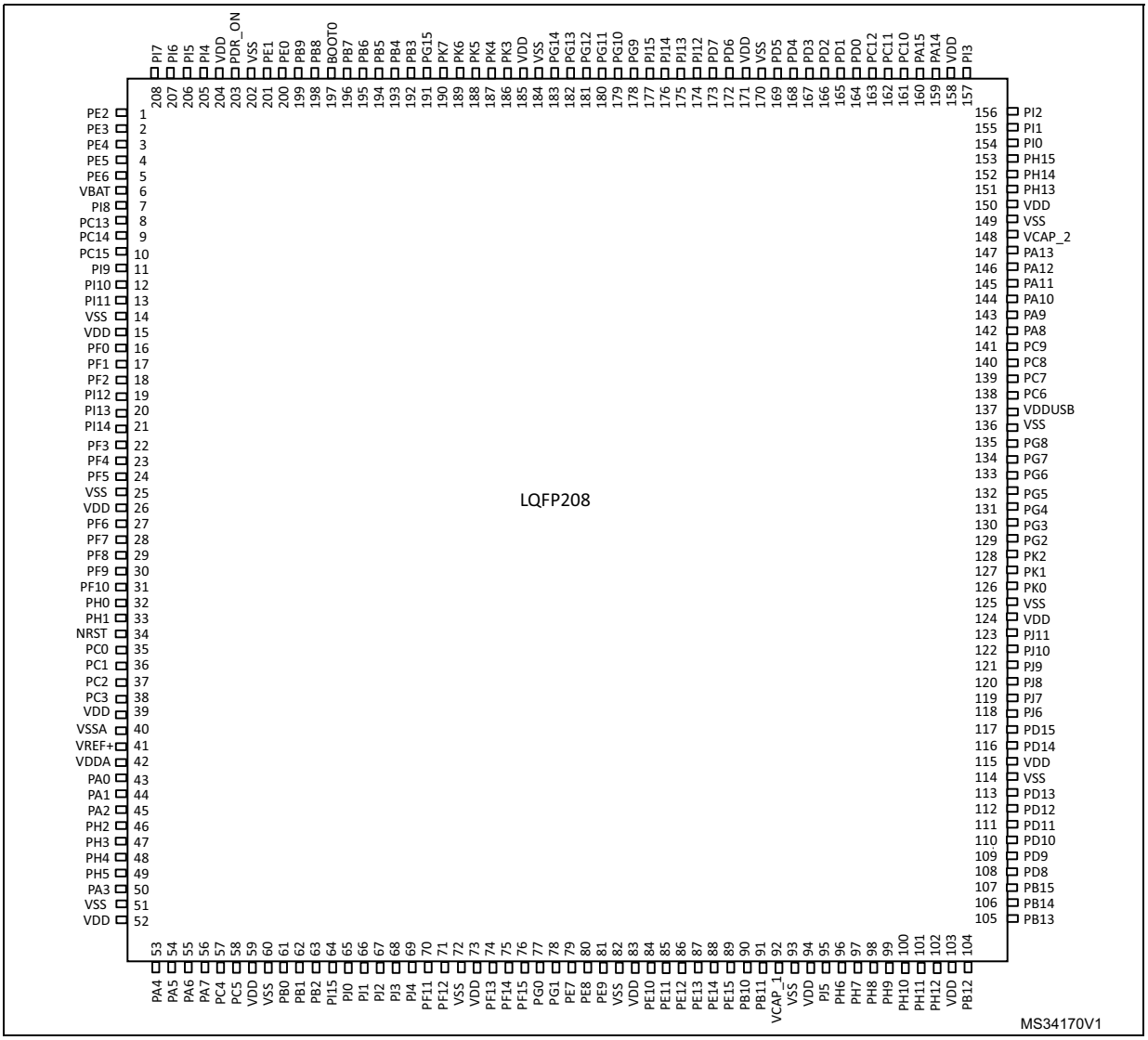
2.18.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

Figure 16. STM32F74xBx LQFP208 pinout



1. The above figure shows the package top view.

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
31	K3	L8	43	R3	53	56	R3	PA7	I/O	FT	(4)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
32	G4	M8	44	N5	54	57	N5	PC4	I/O	FT	(4)	I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
33	H4	N9	45	P5	55	58	P5	PC5	I/O	FT	(4)	SPDIFRX_IN3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	J7	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-
34	J4	N8	46	R5	56	61	R5	PB0	I/O	FT	(4)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT	ADC12_IN8
35	K4	K7	47	R4	57	62	R4	PB1	I/O	FT	(4)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT	ADC12_IN9
36	G5	L7	48	M6	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-

Table 10. STM32F745xx and STM32F746xx pin and ball definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	WLCSP143	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216						
69	D10	D5	102	D15	121	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
70	C10	D4	103	C15	122	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
71	B10	E1	104	B15	123	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	A10	D3	105	A15	124	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	E7	D1	106	F13	125	148	E11	VCAP_2	S	-	-	-	-
74	E5	D2	107	F12	126	149	F10	VSS	S	-	-	-	-
75	F5	C1	108	G13	127	150	F11	VDD	S	-	-	-	-
-	-	-	-	E12	128	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	-	-	E13	129	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	-	-	D13	130	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	-	-	E14	131	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	-	-	D14	132	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port D	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	LPTIM1_ETR	-	-	-	-	UART8_Rx	-	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	LPTIM1_IN2	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	SAI2_MCK_B	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	UART7_RTS	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	UART7_CTS	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	SAI2_SCK_B	-	FMC_D9	-	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10	-	LCD_DE	EVENTOUT

Table 12. STM32F745xx and STM32F746xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/CEC	I2C1/2/3/4/CEC	SPI1/2/3/4/5/6	SPI3/SAI1	SPI2/3/USART1/2/3/UART5/SPDIFRX	SAI2/USART6/UART4/5/7/8/SPDIFRX	CAN1/2/TIM12/13/14/QUADSPI/LCD	SAI2/QUADSPI/OTG2_HS/OTG1_FS	ETH/OTG1_FS	FMC/SDMMC1/OTG2_FS	DCMI	LCD	SYS
Port F	PF13	-	-	-	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	DCMI_D12	LCD_R7	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENTOUT
	PG8	-	-	-	-	-	SPI6_NSS	-	SPDIFRX_IN2	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	-	SPDIFRX_IN3	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	-	FMC_NE2/FMC_NCE	DCMI_VSYNC	-	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	LCD_G3	SAI2_SD_B	-	FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	144	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	180	
			Over-drive ON		-	216[2]	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	45	
		Over-drive ON		0	-	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	90	
		Over-drive ON		0	-	108	
V_{DD}	Standard operating voltage	-		1.7[3]	-	3.6	V
V_{DDA}[4][5]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[6]		1.7[3]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)			2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins)	USB not used		1.7	3.3	3.6	
		USB used		3.0	-	3.6	
V_{BAT}	Backup operating voltage	-		1.65	-	3.6	

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V ≤ V_{DD} ≤ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	178	208(4)	230(4)	-	mA
			200	165	193	212	230	
			180	147	171(4)	185(4)	198(4)	
			168	130	152	164	177	
			144	100	116	127	137	
			60	44	52	63	73	
			25	21	25	36	46	
		All peripherals disabled(3)	216	102	120(4)	141(4)	-	
			200	95	111	131	149	
			180	84	98(4)	112(4)	125(4)	
			168	75	87	100	112	
			144	58	67	77	88	
			60	25	30	41	51	
			25	12	15	25	36	

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART ON except prefetch / L1-cache ON) or SRAM on AXI (L1-cache ON), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	186	213	234	-	mA
			200	172	197	217	235	
			180	152	175	189	202	
			168	135	155	168	180	
			144	104	119	130	140	
			60	46	53	64	74	
			25	22	25	36	47	
		All peripherals disabled(3)	216	108	124	146	-	
			200	100	115	135	154	
			180	89	102	116	129	
			168	79	90	103	115	
			144	61	69	80	90	
			60	27	31	42	52	
			25	12	15	26	36	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 32. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.7	1.9	2.3	5(3)	15(3)	31(3)	µA
		Backup SRAM ON, RTC and LSE OFF	2.4	2.6	3.0	6(3)	20(3)	40(3)	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	2.1	2.4	2.9	6	19	39	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	2.1	2.4	2.9	6	19	39	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	2.2	2.5	3.0	7	20	40	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	2.3	2.6	3.1	7	20	42	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.7	3.0	3.6	8	23	49	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	2.7	3.0	3.6	8	23	49	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	2.8	3.1	3.7	8	24	50	
		Backup SRAM ON, RTC ON and LSE in High drive mode	2.9	3.2	3.8	8	25	51	

1. PDR is OFF for V_{DD}=1.7V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results.
3. Based on characterization, tested in production.

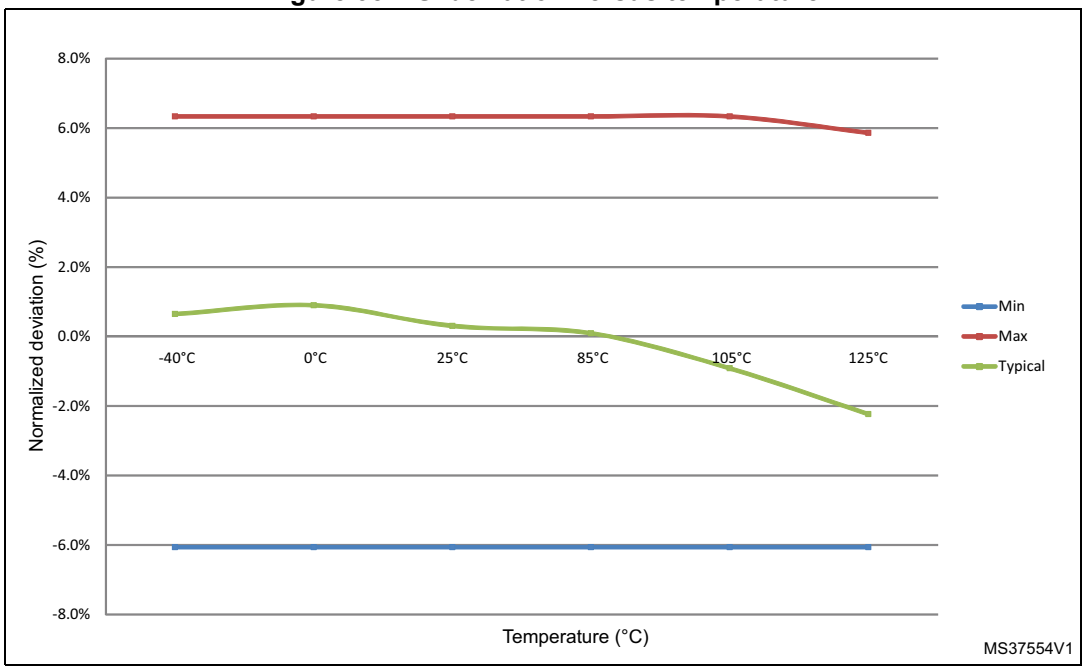
Low-speed internal (LSI) RC oscillator

Table 42. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 35. LSI deviation versus temperature



5.3.11 PLL characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 43. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	216	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	

Table 48. Flash memory programming (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
$t_{ERASE256KB}$	Sector (256 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2.1	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.5	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	8	16	s
		Program/erase parallelism (PSIZE) = x 16	-	5.6	11.2	
		Program/erase parallelism (PSIZE) = x 32	-	4	8	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 100K erase operations.

Table 49. Flash memory programming with V_{PP}

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Double word programming	T_A = 0 to +40 °C V_{DD} = 3.3 V V_{PP} = 8.5 V	-	16	100(2)	µs
$t_{ERASE32KB}$	Sector (32 KB) erase time		-	180	-	ms
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	450	-	
$t_{ERASE256KB}$	Sector (256 KB) erase time		-	900	-	
t_{ME}	Mass erase time		-	6.9	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 65. ADC static accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization results.

Table 66. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz V_{DDA} = V_{REF+}= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		− 67	− 72	-	

1. Guaranteed by characterization results.

Table 67. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

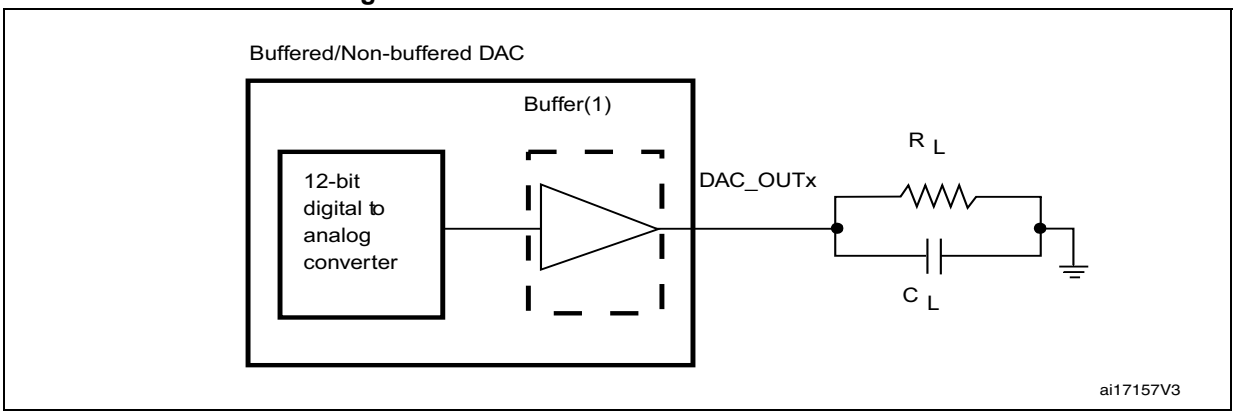
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =36 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		− 70	− 72	-	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.17* does not affect the ADC accuracy.

Figure 45. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.26 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0385 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

Table 74. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode		2	MHz
		Fast-mode	Analog Filtre ON DNF=0	10	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	22.5	
			Analog Filtre OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

5.3.27 FMC characteristics

Unless otherwise specified, the parameters given in *Table 88* to *Table 101* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 58 through *Figure 61* represent asynchronous waveforms and *Table 88* through *Table 95* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

1. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$	$9T_{HCLK}+1.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}-0.5$	$7T_{HCLK}+0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}+2$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}-1$	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 62 through *Figure 65* represent synchronous waveforms and *Table 96* through *Table 99* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

– For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

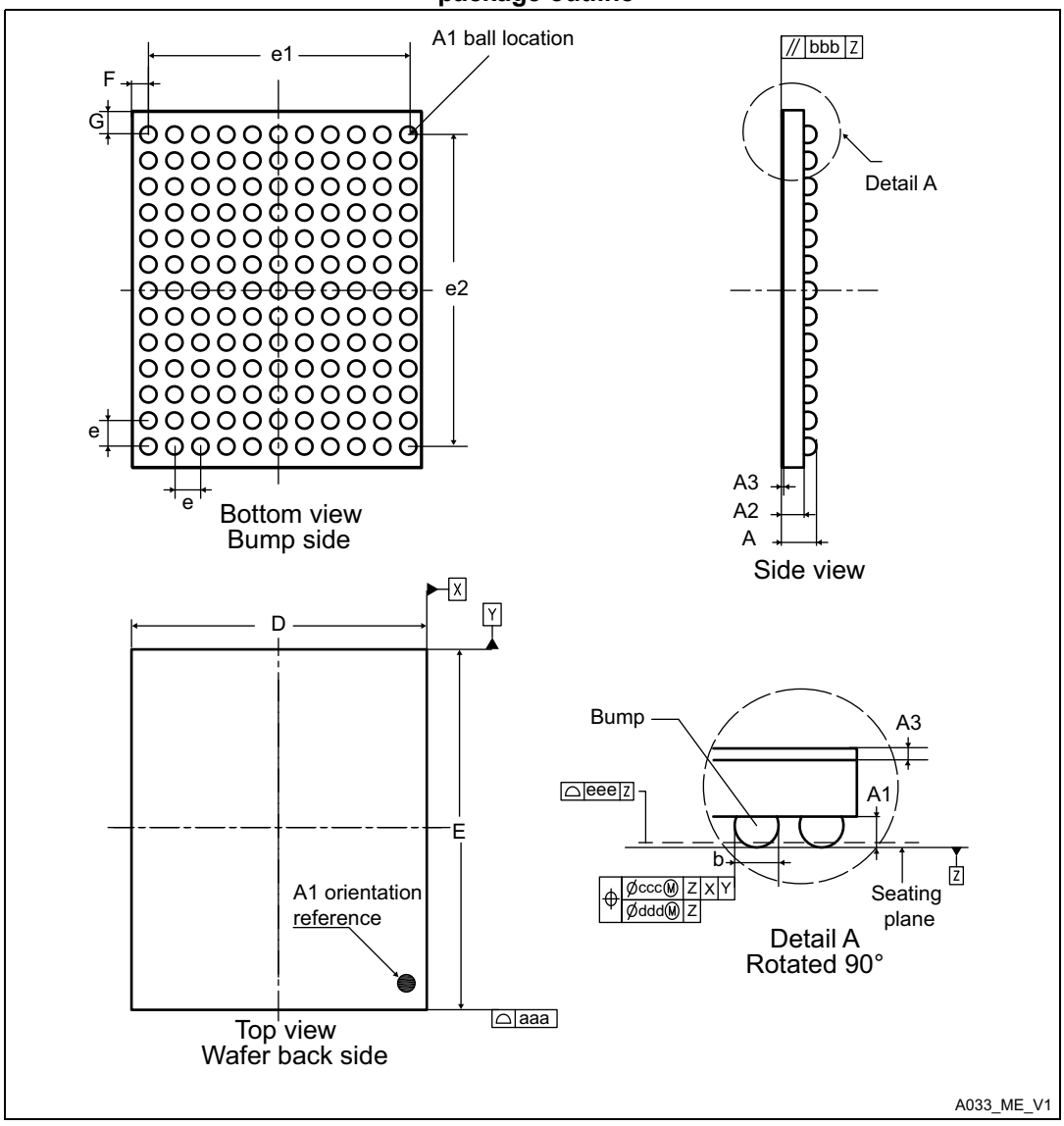
Table 97. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}-0.5$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{HCLK}+0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$T_{HCLK}-0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$T_{HCLK}+0.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

6.3 WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package information

Figure 85. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 115. WLCSP143, 4.539x 5.849 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-

Figure 98. UFBGA176+25, 10 x 10 x 0.65 mm, ultra fine-pitch ball grid array package recommended footprint

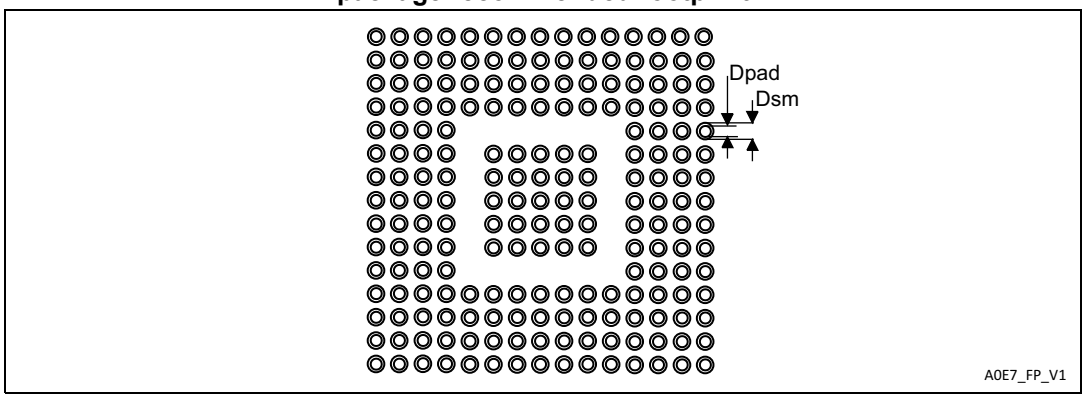


Table 121. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Table 127. Document revision history (continued)

Date	Revision	Changes
10-Dec-2015	3	Updated *Table 10: STM32F745xx and STM32F746xx pin and ball definition* additional functions column: WKUP1, 2, 3, 4, 5, 6 must be respectively PA0, PA2, PC1, PC13, PI8, PI11. Updated *Table 62: ADC characteristics* adding V_{REF-} negative voltage reference. Update *Table 14: Voltage characteristics* adding table note 3. Updated *Table 69: Temperature sensor calibration values* memory addresses. Updated *Table 72: Internal reference voltage calibration values* memory addresses.
18-Feb-2016	4	Updated *Table 52: EMI characteristics* modifying 25/180 MHz by 25/200 MHz. Updated *Figure 13: STM32F74xZx WLCSP143 ballout*. Added TFBGA100 8 x 8 mm package: – Updated Cover page. – Updated *Section 1: Description*. – Updated *Table 2: STM32F745xx and STM32F746xx features and peripheral counts*. – Updated *Table 4: Regulator ON/OFF and internal reset ON/OFF availability*. – Updated *Section 3: Pinouts and pin description* adding *Figure 12: STM32F74xVx TFBGA100 ballout* and adding TFBGA100 ball description in *Table 10: STM32F745xx and STM32F746xx pin and ball definition*. – Updated *Table 17: General operating conditions*. – Updated *Table 53: ESD absolute maximum ratings*. – Updated notes below *Figure 43* and *Figure 44*. – Updated *Section 6: Package information* adding TFBGA100 package information and adding thermal resistance in *Table 124: Package thermal characteristics*. – Updated *Table 10: STM32F745xx and STM32F746xx pin and ball definition* note 5. Updated *Table 35: Peripheral current consumption* peripheral consumption on APB1 and APB2. Updated *Figure 18: STM32F74xNx TFBGA216 ballout*.