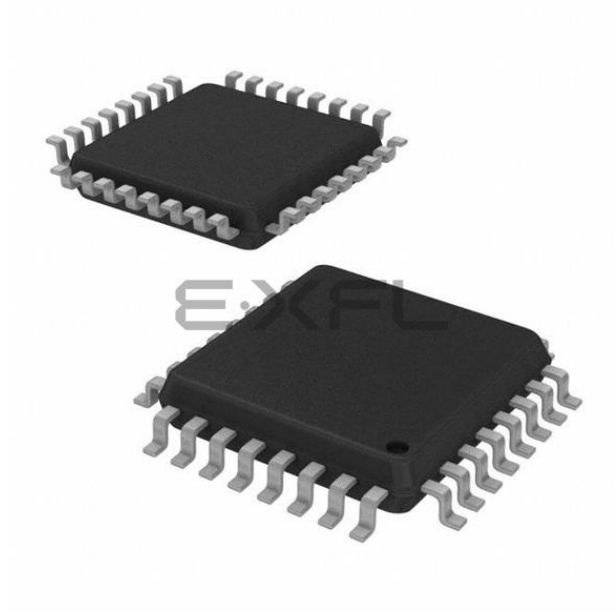

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	7.5KB (7.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908gr8cfa

List of Figures

19-3 CGM Clock Signals. 275
19-4 External Reset Timing 277
19-5 Internal Reset Timing 278
19-6 Sources of Internal Reset 278
19-7 POR Recovery 279
19-8 Interrupt Entry Timing 283
19-9 Interrupt Recovery Timing 283
19-10 Interrupt Processing 284
19-11 Interrupt Recognition Example 285
19-12 Interrupt Status Register 1 (INT1). 288
19-13 Interrupt Status Register 2 (INT2). 288
19-14 Interrupt Status Register 3 (INT3). 289
19-15 Wait Mode Entry Timing 291
19-16 Wait Recovery from Interrupt or Break 291
19-17 Wait Recovery from Internal Reset. 292
19-18 Stop Mode Entry Timing 293
19-19 Stop Mode Recovery from Interrupt or Break 293
19-20 SIM Break Status Register (SBSR) 294
19-21 SIM Reset Status Register (SRSR) 295
19-22 SIM Break Flag Control Register (SBFCR) 296
20-1 SPI I/O Register Summary 299
20-2 SPI Module Block Diagram. 300
20-3 Full-Duplex Master-Slave Connections 301
20-4 Transmission Format (CPHA = 0) 305
20-5 CPHA/$\overline{SS}$ Timing 305
20-6 Transmission Format (CPHA = 1) 306
20-7 Transmission Start Delay (Master) 308
20-8 .SPRF/SPTE CPU Interrupt Timing 309
20-9 Missed Read of Overflow Condition 311
20-10 Clearing SPRF When OVRF Interrupt Is Not Enabled 312
20-11 SPI Interrupt Request Generation 315
20-12 CPHA/$\overline{SS}$ Timing 320
20-13 SPI Control Register (SPCR) 322
20-14 SPI Status and Control Register (SPSCR). 325
20-15 SPI Data Register (SPDR) 328
21-1 Timebase Block Diagram 330
21-2 Timebase Control Register (TBCR) 331
22-1 TIM Block Diagram 338

Memory Map

If the external clock (CGMXCLK) is equal to or greater than 1 MHz, CGMXCLK can be used as the clock source for the ADC. If CGMXCLK is less than 1 MHz, use the PLL-generated bus clock as the clock source. As long as the internal ADC clock is at approximately 1 MHz, correct operation can be guaranteed.

1 = Internal bus clock

0 = External clock (CGMXCLK)

$$\frac{\text{ADC input clock frequency}}{\text{ADIV2–ADIV0}} = 1\text{MHz}$$

Table 10-1. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
TST *opr* TSTA TSTX TST *opr*,X TST ,X TST *opr*,SP	Test for Negative or Zero	(A) – $00 or (X) – $00 or (M) – $00	0	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	–	–	–	–	–	–	INH	95		2
TXA	Transfer X to A	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) – 1	–	–	–	–	–	–	INH	94		2

A Accumulator*n* Any bit
C Carry/borrow bit*opr* Operand (one or two bytes)
CCR Condition code register PC Program counter
dd Direct address of operand PCH Program counter high byte
dd rr Direct address of operand and relative offset of branch instruction PCL Program counter low byte
DD Direct to direct addressing mode REL Relative addressing mode
DIR Direct addressing mode *rel* Relative program counter offset byte
DIX+ Direct to indexed with post increment addressing mode rr Relative program counter offset byte
ee ff High and low bytes of offset in indexed, 16-bit offset addressing SP1 Stack pointer, 8-bit offset addressing mode
EXT Extended addressing mode SP2 Stack pointer 16-bit offset addressing mode
ff Offset byte in indexed, 8-bit offset addressing SP Stack pointer
H Half-carry bit U Undefined
H Index register high byte V Overflow bit
hh ll High and low bytes of operand address in extended addressing X Index register low byte
I Interrupt mask Z Zero bit
ii Immediate operand byte & Logical AND
IMD Immediate source to direct destination addressing mode | Logical OR
IMM Immediate addressing mode ⊕ Logical EXCLUSIVE OR
INH Inherent addressing mode ( ) Contents of
IX Indexed, no offset addressing mode – ( ) Negation (two's complement)
IX+ Indexed, no offset, post increment addressing mode # Immediate value
IX+D Indexed with post increment to direct addressing mode « Sign extend
IX1 Indexed, 8-bit offset addressing mode ← Loaded with
IX1+ Indexed, 8-bit offset, post increment addressing mode ? If
IX2 Indexed, 16-bit offset addressing mode : Concatenated with
M Memory location ↕ Set or cleared
N Negative bit — Not affected

10.9 Opcode Map

See Table 10-2.

External Interrupt (IRQ)

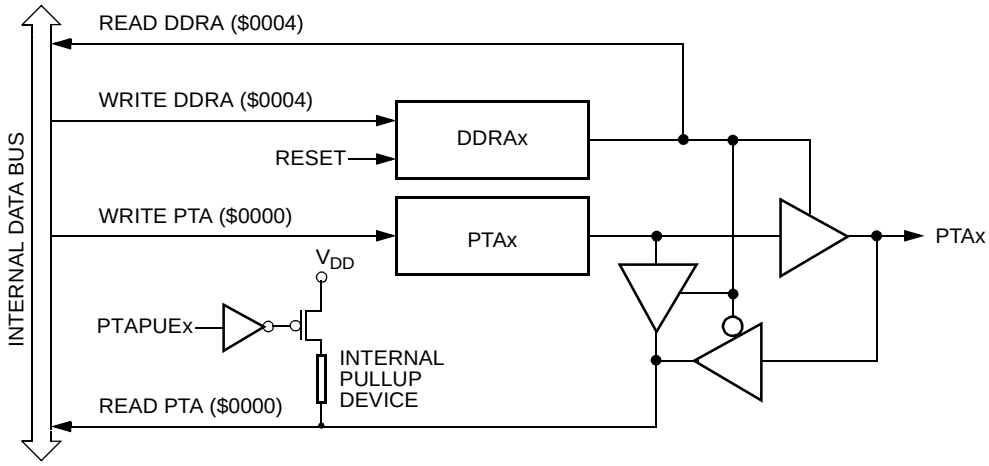


Figure 16-4. Port A I/O Circuit

When bit DDRAx is a logic 1, reading address $0000 reads the PTAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 16-2 summarizes the operation of the port A pins.

Table 16-2. Port A Pin Functions

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X(1)	Input, V_{DD}(4)	DDRA3–DDRA0	Pin	PTA3–PTA0(3)
0	0	X	Input, Hi-Z(2)	DDRA3–DDRA0	Pin	PTA3–PTA0(3)
X	1	X	Output	DDRA3–DDRA0	PTA3–PTA0	PTA3–PTA0

NOTES:
1. X = Don't care
2. Hi-Z = High impedance
3. Writing affects data register, but does not affect input.
4. I/O pin pulled up to V_{DD} by internal pullup device

T1CH1 and T1CH0 — Timer 1 Channel I/O Bits

The PTD5/T1CH1–PTD4/T1CH0 pins are the TIM1 input capture/output compare pins. The edge/level select bits, ELSxB and ELSxA, determine whether the PTD5/T1CH1–PTD4/T1CH0 pins are timer channel I/O pins or general-purpose I/O pins. See Timer Interface Module (TIM).

SPSCK — SPI Serial Clock

The PTD3/SPSCK pin is the serial clock input of the SPI module. When the SPE bit is clear, the PTD3/SPSCK pin is available for general-purpose I/O.

MOSI — Master Out/Slave In

The PTD2/MOSI pin is the master out/slave in terminal of the SPI module. When the SPE bit is clear, the PTD2/MOSI pin is available for general-purpose I/O.

MISO — Master In/Slave Out

The PTD1/MISO pin is the master in/slave out terminal of the SPI module. When the SPI enable bit, SPE, is clear, the SPI module is disabled, and the PTD0/$\overline{SS}$ pin is available for general-purpose I/O.

Data direction register D (DDRD) does not affect the data direction of port D pins that are being used by the SPI module. However, the DDRD bits always determine whether reading port D returns the states of the latches or the states of the pins. See Table 16-5.

$\overline{SS}$ — Slave Select

The PTD0/$\overline{SS}$ pin is the slave select input of the SPI module. When the SPE bit is clear, or when the SPI master bit, SPMSTR, is set, the PTD0/$\overline{SS}$ pin is available for general-purpose I/O. When the SPI is enabled, the DDRB0 bit in data direction register B (DDRB) has no effect on the PTD0/$\overline{SS}$ pin.

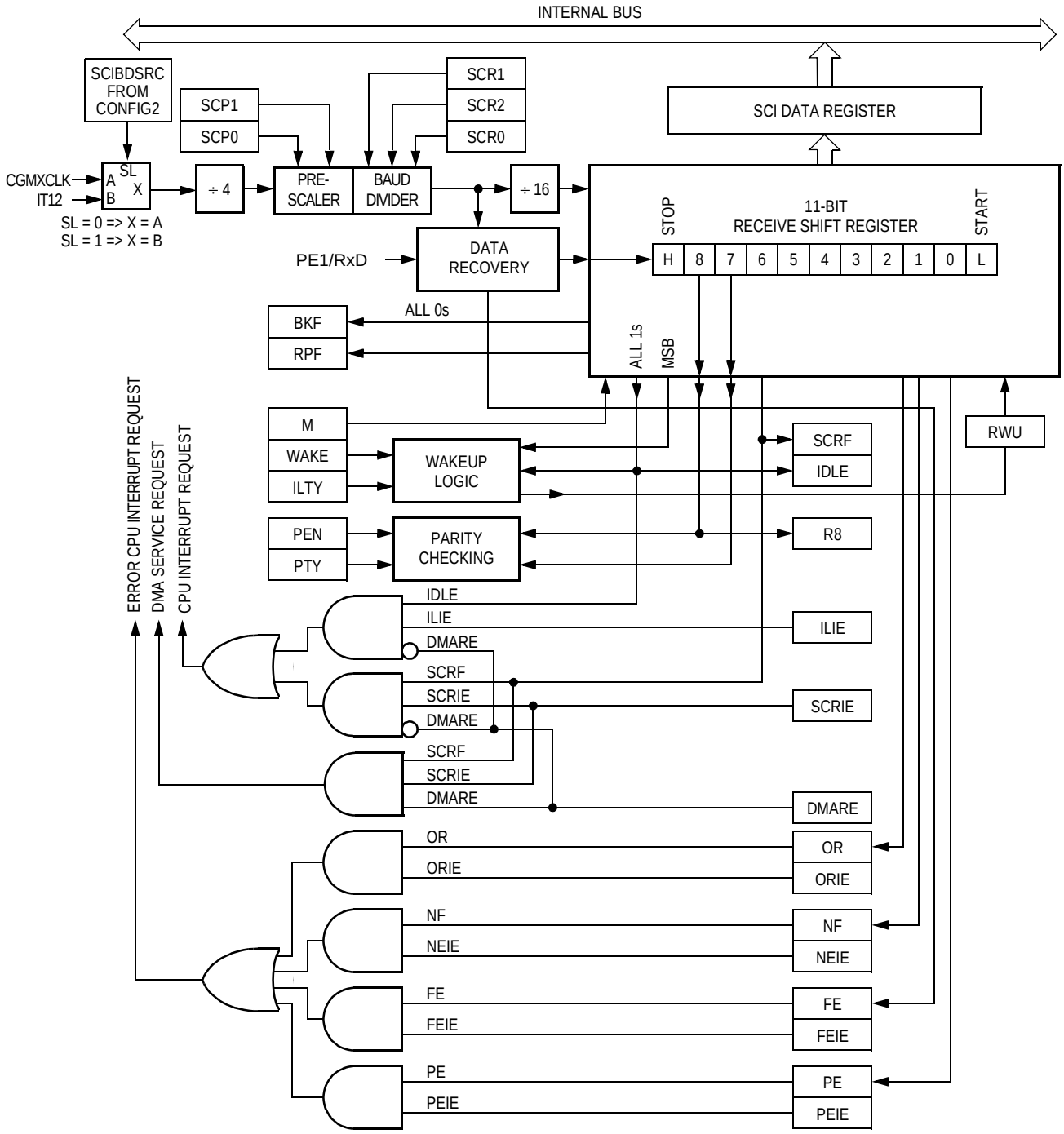


Figure 18-5. SCI Receiver Block Diagram

19.3.2 Clock Startup from POR or LVI Reset

When the power-on reset module or the low-voltage inhibit module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 CGMXCLK cycle POR timeout has completed. The $\overline{\text{RST}}$ pin is driven low by the SIM during this entire period. The IBUS clocks start upon completion of the timeout.

19.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows CGMXCLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. This timeout is selectable as 4096 or 32 CGMXCLK cycles. See Stop Mode.

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

19.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE:$FFFF ($FEFE:$FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

Table 19-3. Interrupt Sources

Priority	Interrupt Source	Interrupt Status Register Flag
	SWI instruction	—
	$\overline{\text{IRQ}}$ pin	I1
	PLL	I2
	TIM1 channel 0	I3
	TIM1 channel 1	I4
	TIM1 overflow	I5
	TIM2 channel 0	I6
	Reserved	I7
	TIM2 overflow	I8
	SPI receiver full	I9
	SPI transmitter empty	I10
	SCI receive error	I11
	SCI receive	I12
	SCI transmit	I13
	Keyboard	I14
	ADC conversion complete	I15
Lowest	Timebase module	I16

19.6.1.6 Interrupt Status Register 3

Address: $FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	I16	I15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 19-14. Interrupt Status Register 3 (INT3)

Bits 7–2 — Always read 0

I16–I15 — Interrupt Flags 16–15

These flags indicate the presence of an interrupt request from the source shown in Table 19-3.

1 = Interrupt request present
0 = No interrupt request present

19.6.2 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

19.6.3 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output. See Timer Interface Module (TIM). The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

NOTE: *References to either timer 1 or timer 2 may be made in the following text by omitting the timer number. For example, TCH0 may refer generically to T1CH0 and T2CH0, and TCH1 will refer to T1CH1.*

NOTE: *The Timer Interface Module in MC68HC908GR8 is constructed by TIM1 which is contained channel 0 and 1, and TIM2 which is contained channel 0 only.*

22.5 Functional Description

NOTE: *References to TCLK and external TIM clock input are only valid if the MCU has an external TCLK pin. If the MCU has no external TCLK pin, the TIM module must use the internal bus clock prescaler selections.*

Figure 22-1 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The TIM channels (per timer) are programmable independently as input capture or output compare channels. If a channel is configured as input capture, then an internal pullup device may be enabled for that channel. See Port D Input Pullup Enable Register.

22.5.8 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the ones written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE: *In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

22.5.9 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIM status and control register (TSC):
   a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
   b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH:TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH:TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):

0 = Input capture operation

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin. See Table 22-3. Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

NOTE: *Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).*

ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to port D, and pin PTDx/TCHx is available as a general-purpose I/O pin. Table 22-3 shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

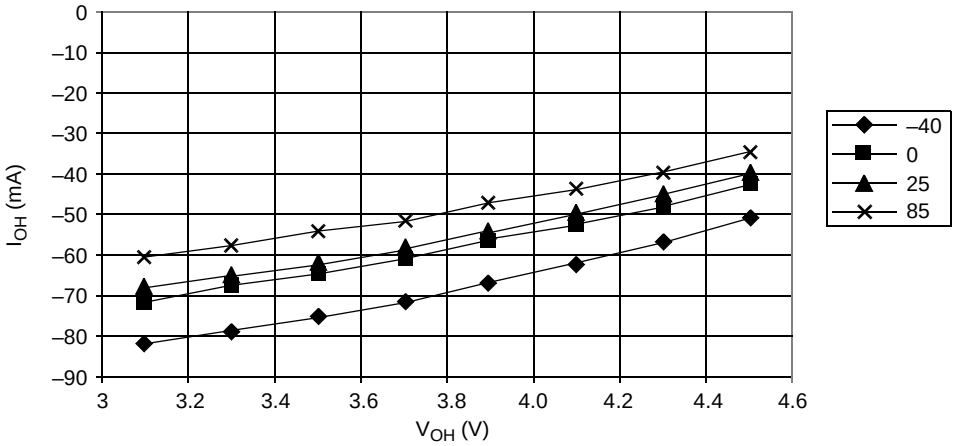
23.8 3.0 V Control Timing

Table 23-7. 3.0 V Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation[2] Crystal option External clock option[3]	f_{osc}	32 dc[4]	100 16.4	kHz MHz
Internal operating frequency	f_{op}	—	4.1	MHz
Internal clock period ($1/f_{OP}$)	t_{cyc}	244	—	ns
$\overline{\text{RESET}}$ input pulse width low[5]	t_{IRL}	125	—	ns
$\overline{\text{IRQ}}$ interrupt pulse width low[6] (edge-triggered)	t_{ILIH}	125	—	ns
$\overline{\text{IRQ}}$ interrupt pulse period	t_{ILIL}	Note 8	—	t_{cyc}
16-bit timer[7] Input capture pulse width Input capture period	 t_{TH},t_{TL} t_{TLTL}	 Note 8	 — —	 ns t_{cyc}

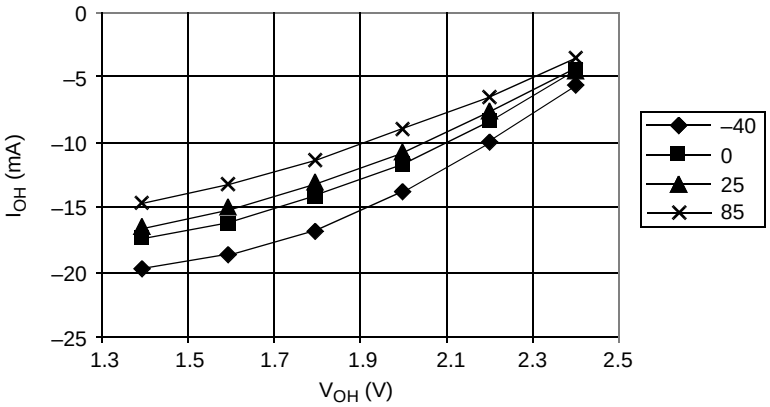
Notes:

1. V_{SS} = 0 Vdc; timing shown with respect to 20% V_{DD} and 70% V_{SS} unless otherwise noted.
2. See Clock Generation Module Characteristics for more information.
3. No more than 10% duty cycle deviation from 50%
4. Some modules may require a minimum frequency greater than dc for proper operation. See appropriate table for this information.
5. Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.
6. Minimum pulse width is for guaranteed interrupt. It is possible for a smaller pulse width to be recognized.
7. Minimum pulse width is for guaranteed interrupt. It is possible for a smaller pulse width to be recognized.
8. The minimum period, t_{ILIL} or t_{TLTL}, should not be less than the number of cycles it takes to execute the interrupt service routine plus t_{CYC}.



$V_{OH} > V_{DD} –0.8$ V @ $I_{OH} = –2.0$ mA
$V_{OH} > V_{DD} –1.5$ V @ $I_{OH} = –10.0$ mA

Figure 23-5. Typical High-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 (V_{DD} = 5.5 Vdc)



$V_{OH} > V_{DD} –0.3$ V @ $I_{OH} = –0.6$ mA
$V_{OH} > V_{DD} –1.0$ V @ $I_{OH} = –4.0$ mA

Figure 23-6. Typical High-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 (V_{DD} = 2.7 Vdc)

23.16.2 CGM Electrical Specifications

Description	Symbol	Min	Typ	Max	Unit
Operating voltage	V_{DD}	2.7	—	5.5	V
Operating temperature	T	–40	25	125	^{o}C
Crystal reference frequency	f_{RCLK}	30	32.768	100	kHz
Range nominal multiplier	f_{NOM}	—	38.4	—	kHz
VCO center-of-range frequency(1)	f_{VRS}	38.4 k	—	40.0 M	Hz
Medium-voltage VCO center-of-range frequency(2)	f_{VRS}	38.4 k	—	40.0 M	Hz
VCO range linear range multiplier	L	1	—	255	
VCO power-of-two range multiplier	2^E	1	—	4	
VCO multiply factor	N	1	—	4095	
VCO prescale multiplier	2^P	1	1	8	
Reference divider factor	R	1	1	15	
VCO operating frequency	f_{VCLK}	38.4 k	—	40.0 M	Hz
Bus operating frequency(1)	f_{BUS}	—	—	8.2	MHz
Bus frequency @ medium voltage(2)	f_{BUS}	—	—	4.1	MHz
Manual acquisition time	t_{Lock}	—	—	50	ms
Automatic lock time	t_{Lock}	—	—	50	ms
PLL jitter(3)	f_J	0	—	f_{RCLK} x 0.025% x 2^P N/4	Hz
External clock input frequency PLL disabled	f_{OSC}	dc	—	32.8 M	Hz
External clock input frequency PLL enabled	f_{OSC}	30 k	—	1.5 M	Hz

Notes:

1. 5.0 V ± 10% V_{DD}
2. 3.0 V ± 10% V_{DD}
3. Deviation of average bus frequency over 2 ms. N = VCO multiplier.

serial communications interface module (SCI) — A module in the M68HC08 Family that supports asynchronous communication.

serial peripheral interface module (SPI) — A module in the M68HC08 Family that supports synchronous communication.

set — To change a bit from logic 0 to logic 1; opposite of clear.

shift register — A chain of circuits that can retain the logic levels (logic 1 or logic 0) written to them and that can shift the logic levels to the right or left through adjacent circuits in the chain.

signed — A binary number notation that accommodates both positive and negative numbers. The most significant bit is used to indicate whether the number is positive or negative, normally logic 0 for positive and logic 1 for negative. The other seven bits indicate the magnitude of the number.

software — Instructions and data that control the operation of a microcontroller.

software interrupt (SWI) — An instruction that causes an interrupt and its associated vector fetch.

SPI — See "serial peripheral interface module (SPI)."

stack — A portion of RAM reserved for storage of CPU register contents and subroutine return addresses.

stack pointer (SP) — A 16-bit register in the CPU08 containing the address of the next available storage location on the stack.

start bit — A bit that signals the beginning of an asynchronous serial transmission.

status bit — A register bit that indicates the condition of a device.

stop bit — A bit that signals the end of an asynchronous serial transmission.

subroutine — A sequence of instructions to be used more than once in the course of a program. The last instruction in a subroutine is a return from subroutine (RTS) instruction. At each place in the main program where the subroutine instructions are needed, a jump or branch to subroutine (JSR or BSR) instruction is used to call the subroutine. The CPU leaves the flow of the main program to execute the instructions in the subroutine. When the RTS instruction is executed, the CPU returns to the main program where it left off.

synchronous — Refers to logic circuits and operations that are synchronized by a common reference signal.

TIM — See "timer interface module (TIM)."

Revision History

Contents

Introduction 405

Changes from Rev 3.0 published in February 2002 to Rev 4.0 published in June 2002 405

Changes from Rev 2.0 published in January 2002 to Rev 3.0 published in February 2002 406

Changes from Rev 1.0 published in April 2001 to Rev 2.0 published in December 2001 406

Introduction

This section contains the revision history for the MC68HC908GR8 technical data book.

Changes from Rev 3.0 published in February 2002 to Rev 4.0 published in June 2002

Section	Page (in Rev 3.0)	Description of change
All references to the ROM MC68HC08GR8 removed. Appendix A removed.		
Electrical Specifications	363	Maximum junction temperature increased to 140°C
	364	Input High Voltage for OSC1 changed Stop I_{DD} for temperatures >85°C added
	366	Input High Voltage for OSC1 changed Input Low Voltage for OSC1 changed Stop I_{DD} for temperatures >85°C added