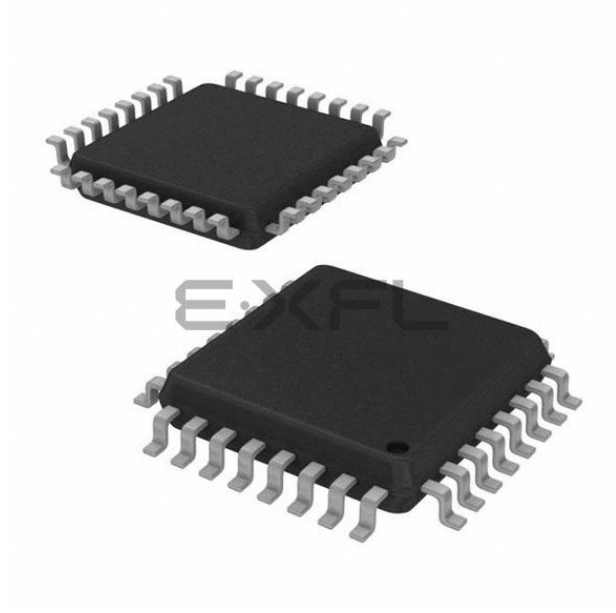

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	7.5KB (7.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908gr8cfae

Section 2. Memory Map

2.1 Contents

2.2 Introduction

The CPU08 can address 64K bytes of memory space. The memory map, shown in Figure 2-1, includes:

- 8K bytes of FLASH memory, 7680 bytes of user space on the MC68HC908GR8 or
  4K bytes of FLASH memory, 4096 bytes of user space on the MC68HC908GR4
- 384 bytes of random-access memory (RAM)
- 36 bytes of user-defined vectors
- 310 bytes of monitor routines in read-only memory (ROM)
- 544 bytes of integrated FLASH burn-in routines in ROM

2.3 Unimplemented Memory Locations

Accessing an unimplemented location can cause an illegal address reset if illegal address resets are enabled. In the memory map (Figure 2-1) and in register figures in this document, unimplemented locations are shaded.

  - $FFEC and $FFED; TIM2 overflow
  - $FFF0 and $FFF1; TIM2 channel 0
- Serial peripheral interface module (SPI) interrupt — A CPU interrupt request from the SPI loads the program counter with the contents of:
  - $FFE8 and $FFE9; SPI transmitter
  - $FFEA and $FFEB; SPI receiver
- Serial communications interface module (SCI) interrupt — A CPU interrupt request from the SCI loads the program counter with the contents of:
  - $FFE2 and $FFE3; SCI transmitter
  - $FFE4 and $FFE5; SCI receiver
  - $FFE6 and $FFE7; SCI receiver error
- Analog-to-digital converter module (ADC) interrupt — A CPU interrupt request from the ADC loads the program counter with the contents of: $FFDE and $FFDF; ADC conversion complete.
- Timebase module (TBM) interrupt — A CPU interrupt request from the TBM loads the program counter with the contents of: $FFDC and $FFDD; TBM interrupt.

3.16 Exiting Stop Mode

These events restart the system clocks and load the program counter with the reset vector or with an interrupt vector:

- External reset — A logic 0 on the $\overline{\text{RST}}$ pin resets the MCU and loads the program counter with the contents of locations $FFFE and $FFFF.
- External interrupt — A high-to-low transition on an external interrupt pin loads the program counter with the contents of locations:
  - $FFFA and $FFFB; $\overline{\text{IRQ}}$ pin
  - $FFDE and $FFDF; keyboard interrupt pins

ILOP — Illegal Opcode Reset Bit

1 = Last reset caused by an illegal opcode
0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit

1 = Last reset caused by an opcode fetch from an illegal address
0 = POR or read of SRSR

LVI — Low-Voltage Inhibit Reset Bit

1 = Last reset caused by low-power supply voltage
0 = POR or read of SRSR

4.4 Interrupts

An interrupt temporarily changes the sequence of program execution to respond to a particular event. An interrupt does not stop the operation of the instruction being executed, but begins when the current instruction completes its operation.

4.4.1 Effects

An interrupt:

- Saves the CPU registers on the stack. At the end of the interrupt, the RTI instruction recovers the CPU registers from the stack so that normal processing can resume.
- Sets the interrupt mask (I bit) to prevent additional interrupts. Once an interrupt is latched, no other interrupt can take precedence, regardless of its priority.
- Loads the program counter with a user-defined vector address

4.4.2.6 TIM2

TIM2 CPU interrupt sources:

- TIM2 overflow flag (TOF) — The TOF bit is set when the TIM2 counter value rolls over to $0000 after matching the value in the TIM2 counter modulo registers. The TIM2 overflow interrupt enable bit, TOIE, enables TIM2 overflow CPU interrupt requests. TOF and TOIE are in the TIM2 status and control register.
- TIM2 channel flag (CH0F) — The CH0F bit is set when an input capture or output compare occurs on channel 0. The channel 0 interrupt enable bit, CH0IE, enables channel 0 TIM2 CPU interrupt requests. CH0F and CH0IE are in the TIM2 channel 0 status and control register.

4.4.2.7 SPI

SPI CPU interrupt sources:

- SPI receiver full bit (SPRF) — The SPRF bit is set every time a byte transfers from the shift register to the receive data register. The SPI receiver interrupt enable bit, SPRIE, enables SPRF CPU interrupt requests. SPRF is in the SPI status and control register and SPRIE is in the SPI control register.
- SPI transmitter empty (SPTE) — The SPTE bit is set every time a byte transfers from the transmit data register to the shift register. The SPI transmit interrupt enable bit, SPTIE, enables SPTE CPU interrupt requests. SPTE is in the SPI status and control register and SPTIE is in the SPI control register.
- Mode fault bit (MODF) — The MODF bit is set in a slave SPI if the $\overline{SS}$ pin goes high during a transmission with the mode fault enable bit (MODFEN) set. In a master SPI, the MODF bit is set if the $\overline{SS}$ pin goes low at any time with the MODFEN bit set. The error interrupt enable bit, ERRIE, enables MODF CPU interrupt requests. MODF, MODFEN, and ERRIE are in the SPI status and control register.

- Break address register low (BRKL)
- SIM break status register (SBSR)
- SIM break flag control register (SBFCR)

6.6.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

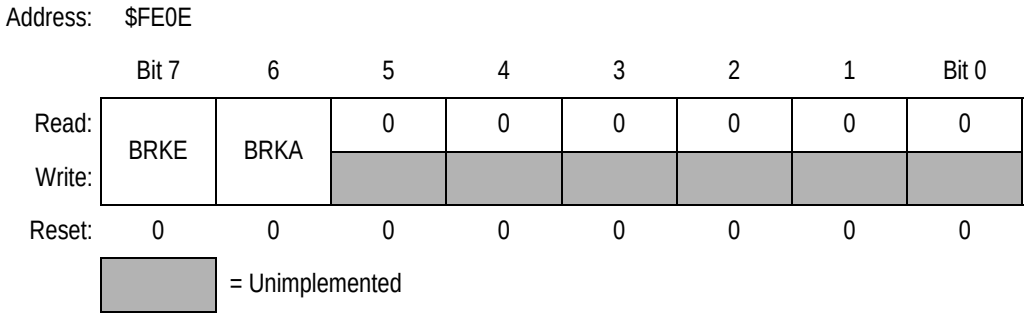


Figure 6-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a logic 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled on 16-bit address match

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a logic 1 to BRKA generates a break interrupt. Clear BRKA by writing a logic 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = (When read) Break address match
0 = (When read) No break address match

Section 11. Flash Memory

11.1 Contents

11.2 Introduction

This section describes the operation of the embedded FLASH memory. This memory can be read, programmed, and erased from a single external supply. The program, erase, and read operations are enabled through the use of an internal charge pump.

11.3 Functional Description

The FLASH memory is an array of 7,680 bytes for the MC68HC908GR8 or 4,096 bytes for the MC68HC908GR4 with an additional 36 bytes of user vectors and one byte used for block protection. *An erased bit reads as logic 1 and a programmed bit reads as a logic 0*. The program and erase operations are facilitated through control bits in the Flash Control

PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

1 = Program operation selected
0 = Program operation unselected

11.5 FLASH Page Erase Operation

Use this step-by-step procedure to erase a page (64 bytes) of FLASH memory to read as logic 1:

1. Set the ERASE bit, and clear the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH address within the page address range desired.
4. Wait for a time, t_{nvs} (min. 10µs)
5. Set the HVEN bit.
6. Wait for a time, t_{Erase} (min. 1ms)
7. Clear the ERASE bit.
8. Wait for a time, t_{nvh} (min. 5µs)
9. Clear the HVEN bit.
10. After a time, t_{rcv} (typ. 1µs), the memory can be accessed again in read mode.

NOTE: *While these operations must be performed in the order shown, other unrelated operations may occur between the steps.*

MODE — IRQ Edge/Level Select Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ1}}$ pin. Reset clears MODE.

1 = $\overline{\text{IRQ1}}$ interrupt requests on falling edges and low levels
0 = $\overline{\text{IRQ1}}$ interrupt requests on falling edges only

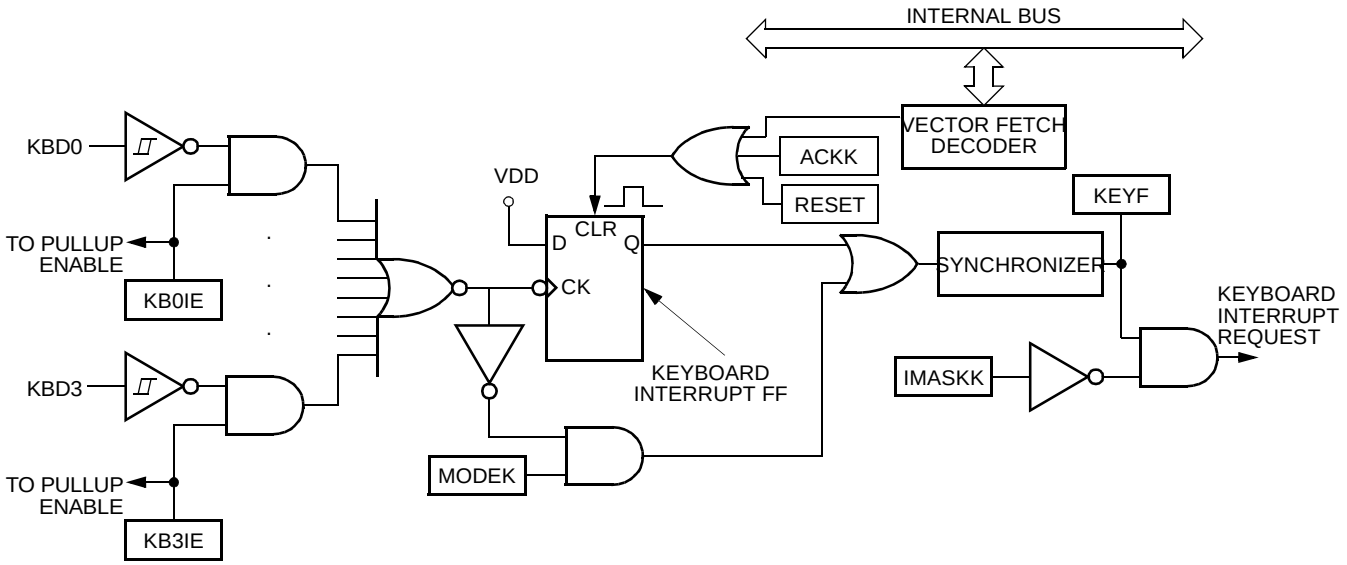


Figure 13-1. Keyboard Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	Keyboard Status and Control Register (INTKBSCR)	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:						ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (INTKBIER)	Read:					KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:					0	0	0	0

= Unimplemented

Figure 13-2. I/O Register Summary

NOTE: *Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a logic 0 for software to read the pin.*

13.5 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the internal pullup to reach a logic 1. Therefore, a false interrupt can occur as soon as the pin is enabled.

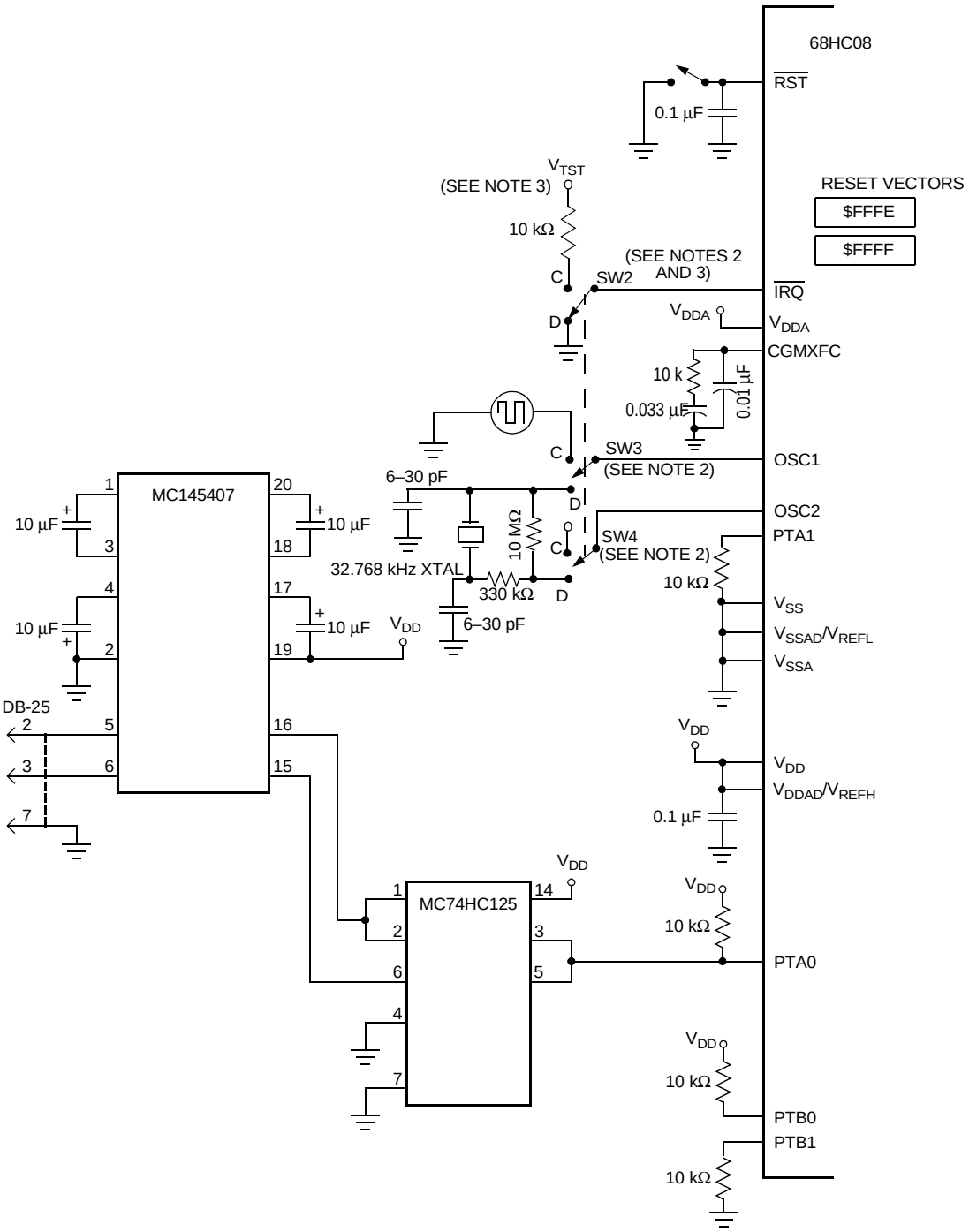
To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting the IMASKK bit in the keyboard status and control register.
2. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.
3. Write to the ACKK bit in the keyboard status and control register to clear any false interrupts.
4. Clear the IMASKK bit.

An interrupt signal on an edge-triggered pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge- and level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt is:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in data direction register A.
2. Write logic 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.



Notes:
1. SW2, SW3, and SW4: Position C — Enter monitor mode using external oscillator.
   SW2, SW3, and SW4: Position D — Enter monitor mode using external XTAL and internal PLL.
2. See . Monitor Mode Signal Requirements and Options for $\overline{IRQ}$ voltage level requirements.

Figure 15-1. Monitor Mode Circuit

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0008	Port E Data Register (PTE)	Read:	0	0	0	0	0	0	PTE1	PTE0
		Write:								
		Reset:	Unaffected by reset							
$000C	Data Direction Register E (DDRE)	Read:	0	0	0	0	0	0	DDRE1	DDRE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000D	Port A Input Pullup Enable Register (PTAPUE)	Read:	0	0	0	0	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000E	Port C Input Pullup Enable Register (PTCPUE)	Read:	0	0	0	0	0	0	PTCPUE1	PTCPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000F	Port D Input Pullup Enable Register (PTDPUE)	Read:	0	PTDPUE6	PTDPUE5	PTDPUE4	PTDPUE3	PTDPUE2	PTDPUE1	PTDPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-1. I/O Port Register Summary (Continued)

tolerance is much more than the degree of misalignment that is likely to occur.

As the receiver samples an incoming character, it resynchronizes the RT clock on any valid falling edge within the character. Resynchronization within characters corrects misalignments between transmitter bit times and receiver bit times.

18.5.3.6 Slow Data Tolerance

Figure 18-7 shows how much a slow received character can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

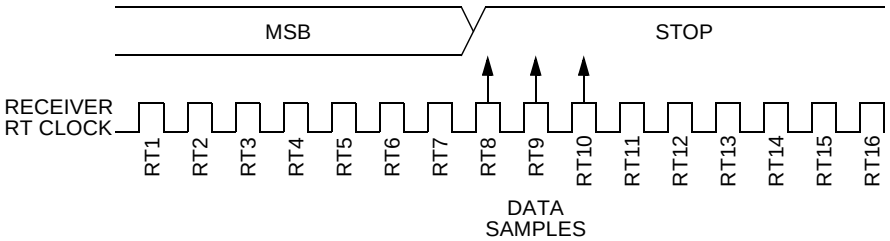


Figure 18-7. Slow Data

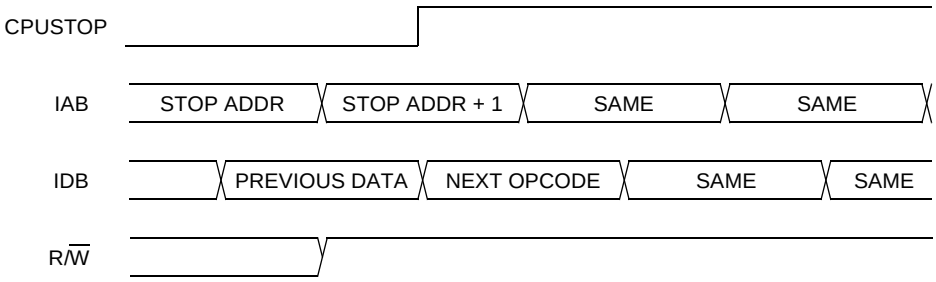
For an 8-bit character, data sampling of the stop bit takes the receiver 9 bit times × 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in Figure 18-7, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 9 bit times × 16 RT cycles + 3 RT cycles = 147 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit character with no errors is

$$\left|\frac{154 - 147}{154}\right| \times 100 = 4.54\%$$

For a 9-bit character, data sampling of the stop bit takes the receiver 10 bit times × 16 RT cycles + 10 RT cycles = 170 RT cycles.



Note : Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 19-18. Stop Mode Entry Timing

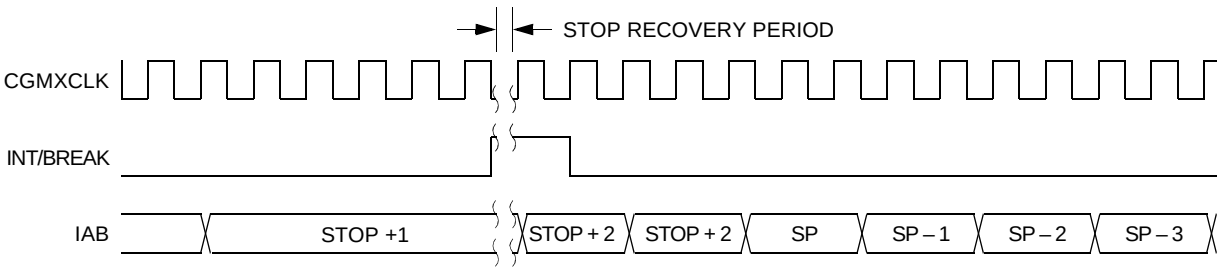


Figure 19-19. Stop Mode Recovery from Interrupt or Break

19.8 SIM Registers

The SIM has three memory-mapped registers. Table 19-4 shows the mapping of these registers.

Table 19-4. SIM Registers

Address	Register	Access Mode
$FE00	SBSR	User
$FE01	SRSR	User
$FE03	SBFCR	User

22.5.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

22.5.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

22.5.4 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in Output Compare. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

22.10.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Address: T1MODH, $0023 and T2MODH, $002E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented

Figure 22-7. TIM Counter Modulo Register High (TMODH)

Address: T1MODL, $0024 and T2MODL, $002F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented

Figure 22-8. TIM Counter Modulo Register Low (TMODL)

NOTE: *Reset the TIM counter before writing to the TIM counter modulo registers.*

23.8 3.0 V Control Timing

Table 23-7. 3.0 V Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of operation[2] Crystal option External clock option[3]	f_{osc}	32 dc[4]	100 16.4	kHz MHz
Internal operating frequency	f_{op}	—	4.1	MHz
Internal clock period ($1/f_{OP}$)	t_{cyc}	244	—	ns
$\overline{\text{RESET}}$ input pulse width low[5]	t_{IRL}	125	—	ns
$\overline{\text{IRQ}}$ interrupt pulse width low[6] (edge-triggered)	t_{ILIH}	125	—	ns
$\overline{\text{IRQ}}$ interrupt pulse period	t_{ILIL}	Note 8	—	t_{cyc}
16-bit timer[7] Input capture pulse width Input capture period	 t_{TH},t_{TL} t_{TLTL}	 Note 8	 — —	 ns t_{cyc}

Notes:

1. V_{SS} = 0 Vdc; timing shown with respect to 20% V_{DD} and 70% V_{SS} unless otherwise noted.
2. See Clock Generation Module Characteristics for more information.
3. No more than 10% duty cycle deviation from 50%
4. Some modules may require a minimum frequency greater than dc for proper operation. See appropriate table for this information.
5. Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.
6. Minimum pulse width is for guaranteed interrupt. It is possible for a smaller pulse width to be recognized.
7. Minimum pulse width is for guaranteed interrupt. It is possible for a smaller pulse width to be recognized.
8. The minimum period, t_{ILIL} or t_{TLTL}, should not be less than the number of cycles it takes to execute the interrupt service routine plus t_{CYC}.

23.13 5.0 V SPI Characteristics

Diagram Number[1]	Characteristic[2]	Symbol	Min	Max	Unit
	Operating frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 $f_{OP}/128$ DC	 $f_{OP}/2$ f_{OP}	 MHz MHz
1	Cycle time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2 1	 128 —	 t_{cyc} t_{cyc}
2	Enable lead time	$t_{Lead(S)}$	1	—	t_{cyc}
3	Enable lag time	$t_{Lag(S)}$	1	—	t_{cyc}
4	Clock (SPSCK) high time Master Slave	 $t_{SCKH(M)}$ $t_{SCKH(S)}$	 t_{cyc} –25 1/2 t_{cyc} –25	 64 t_{cyc} —	 ns ns
5	Clock (SPSCK) low time Master Slave	 $t_{SCKL(M)}$ $t_{SCKL(S)}$	 t_{cyc} –25 1/2 t_{cyc} –25	 64 t_{cyc} —	 ns ns
6	Data setup time (inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 30 30	 — —	 ns ns
7	Data hold time (inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 30 30	 — —	 ns ns
8	Access time, slave[3] CPHA = 0 CPHA = 1	 $t_{A(CP0)}$ $t_{A(CP1)}$	 0 0	 40 40	 ns ns
9	Disable time, slave[4]	$t_{DIS(S)}$	—	40	ns
10	Data valid time, after enable edge Master Slave[5]	 $t_{V(M)}$ $t_{V(S)}$	 — —	 50 50	 ns ns
11	Data hold time, outputs, after enable edge Master Slave	 $t_{HO(M)}$ $t_{HO(S)}$	 0 0	 — —	 ns ns

Notes:

1. Numbers refer to dimensions in Figure 23-16 and Figure 23-17.
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins.
3. Time to data active from high-impedance state
4. Hold time to high-impedance state
5. With 100 pF on all SPI pins

25.3 MC Order Numbers

Table 25-1. MC Order Numbers

	MC Order Number[1]	Operating Temperature Range (°C)
Production Parts	MC68HC908GR8CP	– 40 to + 85
	MC68HC908GR8CFA	– 40 to + 85
	MC68HC908GR8CDW	– 40 to + 85
	MC68HC908GR8VFA	– 40 to + 105
	MC68HC908GR8VP	– 40 to + 105
	MC68HC908GR8VDW	– 40 to + 105
	MC68HC908GR8MFA	– 40 to + 125
	MC68HC908GR8MP	– 40 to + 125
	MC68HC908GR8MDW	– 40 to + 125
	MC68HC908GR4CP	– 40 to + 85
	MC68HC908GR4CFA	– 40 to + 85
	MC68HC908GR4CDW	– 40 to + 85
	MC68HC908GR4VFA	– 40 to + 105
	MC68HC908GR4VP	– 40 to + 105
	MC68HC908GR4VDW	– 40 to + 105
	MC68HC908GR4MFA	– 40 to + 125
	MC68HC908GR4MP	– 40 to + 125
	MC68HC908GR4MDW	– 40 to + 125
Tape and Reel	MC908GR8CFAR2	– 40 to + 85
	MC908GR8CDWR2	– 40 to + 85
	MC908GR8VFAR2	– 40 to + 105
	MC908GR8VDWR2	– 40 to + 105
	MC908GR8MFAR2	– 40 to + 125
	MC908GR8MDWR2	– 40 to + 125
	MC908GR4CFAR2	– 40 to + 85
	MC908GR4CDWR2	– 40 to + 85
	MC908GR4VFAR2	– 40 to + 105
	MC908GR4VDWR2	– 40 to + 105
	MC908GR4MFAR2	– 40 to + 125
	MC908GR4MDWR2	– 40 to + 125

1. FA = quad flat pack
   P = plastic dual in line package
   DW = Small outline integrated circuit (SOIC) package

illegal address — An address not within the memory map

illegal opcode — A nonexistent opcode.

I — The interrupt mask bit in the condition code register of the CPU08. When I is set, all interrupts are disabled.

index register (H:X) — A 16-bit register in the CPU08. The upper byte of H:X is called H. The lower byte is called X. In the indexed addressing modes, the CPU uses the contents of H:X to determine the effective address of the operand. H:X can also serve as a temporary data storage location.

input/output (I/O) — Input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level on an external signal.

instructions — Operations that a CPU can perform. Instructions are expressed by programmers as assembly language mnemonics. A CPU interprets an opcode and its associated operand(s) and instruction.

interrupt — A temporary break in the sequential execution of a program to respond to signals from peripheral devices by executing a subroutine.

interrupt request — A signal from a peripheral to the CPU intended to cause the CPU to execute a subroutine.

I/O — See “input/output (I/0).”

IRQ — See "external interrupt module (IRQ)."

jitter — Short-term signal instability.

latch — A circuit that retains the voltage level (logic 1 or logic 0) written to it for as long as power is applied to the circuit.

latency — The time lag between instruction completion and data movement.

least significant bit (LSB) — The rightmost digit of a binary number.

logic 1 — A voltage level approximately equal to the input power voltage (V_{DD}).

logic 0 — A voltage level approximately equal to the ground voltage (V_{SS}).

low byte — The least significant eight bits of a word.

low voltage inhibit module (LVI) — A module in the M68HC08 Family that monitors power supply voltage.