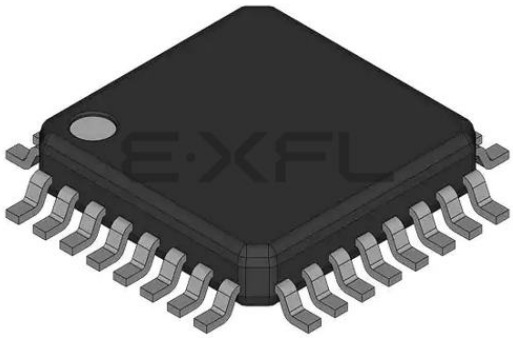

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	7.5KB (7.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchc908gr8mfae

Table of Contents

Section 24. Mechanical Specifications

Section 25. Ordering Information

Glossary

Revision History

- 7680 bytes of on-chip FLASH memory on the MC68HC908GR8 and 4096 bytes of on-chip FLASH memory on the MC68HC908GR4 with in-circuit programming capabilities of FLASH program memory
- 384 bytes of on-chip random-access memory (RAM)
- Serial peripheral interface module (SPI)
- Serial communications interface module (SCI)
- One 16-bit, 2-channel timer (TIM1) and one 16-bit, 1-channel timer (TIM2) interface modules with selectable input capture, output compare, and PWM capability on each channel
- 6-channel, 8-bit successive approximation analog-to-digital converter (ADC)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- Clock generator module with on-chip 32-kHz crystal compatible PLL (phase-lock loop)
- Up to 21 general-purpose input/output (I/O) pins, including:
  - 19 shared-function I/O pins
  - Up to two dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- High current 10-mA sink/10-mA source capability on all port pins
- Higher current 15-mA sink/source capability on PTC0–PTC1
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external 32-kHz crystal
- Oscillator stop mode enable bit (OSCSTOPENB) in the CONFIG register to allow user selection of having the oscillator enabled or disabled during stop mode

- Low-voltage inhibit (LVI) reset — A power supply voltage below the LVI_{tripf} voltage resets the MCU and loads the program counter with the contents of locations $FFFE and $FFFF.
- Break interrupt — A break interrupt loads the program counter with the contents of locations $FFFC and $FFFD.
- Timebase module (TBM) interrupt — A TBM interrupt loads the program counter with the contents of locations $FFDC and $FFDD when the timebase counter has rolled over. This allows the TBM to generate a periodic wakeup from stop mode.

Upon exit from stop mode, the system clocks begin running after an oscillator stabilization delay. A 12-bit stop recovery counter inhibits the system clocks for 4096 CGMXCLK cycles after the reset or external interrupt.

The short stop recovery bit, SSREC, in the configuration register controls the oscillator stabilization delay during stop recovery. Setting SSREC reduces stop recovery time from 4096 CGMXCLK cycles to 32 CGMXCLK cycles.

NOTE: *Use the full stop recovery time (SSREC = 0) in applications that use an external crystal.*

4.3.3.3 Low-Voltage Inhibit Reset

A low-voltage inhibit (LVI) reset is an internal reset caused by a drop in the power supply voltage to the LVI trip voltage, V_{TRIPF}.

An LVI reset:

- Holds the clocks to the CPU and modules inactive for an oscillator stabilization delay of 4096 CGMXCLK cycles after the power supply voltage rises to V_{TRIPF}
- Drives the $\overline{RST}$ pin low for as long as V_{DD} is below V_{TRIPF} and during the oscillator stabilization delay
- Releases the $\overline{RST}$ pin 32 CGMXCLK cycles after the oscillator stabilization delay
- Releases the CPU to begin the reset vector sequence 64 CGMXCLK cycles after the oscillator stabilization delay
- Sets the LVI bit in the SIM reset status register

4.3.3.4 Illegal Opcode Reset

An illegal opcode reset is an internal reset caused by an opcode that is not in the instruction set. An illegal opcode reset sets the ILOP bit in the SIM reset status register.

If the stop enable bit, STOP, in the mask option register is a logic 0, the STOP instruction causes an illegal opcode reset.

4.3.3.5 Illegal Address Reset

An illegal address reset is an internal reset caused by opcode fetch from an unmapped address. An illegal address reset sets the ILAD bit in the SIM reset status register.

A data fetch from an unmapped address does not generate a reset.

Section 5. Analog-to-Digital Converter (ADC)

5.1 Contents

5.2 Introduction

This section describes the 8-bit analog-to-digital converter (ADC).

For further information regarding analog-to-digital converters on Motorola microcontrollers, please consult the HC08 ADC Reference Manual, ADCRM/AD.

BW — Break Wait Bit

This read/write bit is set when a break interrupt causes an exit from wait mode. Clear BW by writing a logic 0 to it. Reset clears BW.

1 = Break interrupt during wait mode
0 = No break interrupt during wait mode

BW can be read within the break interrupt routine. The user can modify the return address on the stack by subtracting 1 from it. The following code is an example.

This code works if the H register was stacked in the break interrupt routine. Execute this code at the end of the break interrupt routine.

```
HIBYTE  EQU    5
LOBYTE  EQU    6
;       If not BW, do RTI
        BRCLR  BW,BSR, RETURN  ; See if wait mode or stop mode
                               ; was exited by break.
        TST    LOBYTE,SP       ; If RETURNLO is not 0,
        BNE    DOLO            ; then just decrement low byte.
        DEC    HIBYTE,SP       ; Else deal with high byte also.
DOLO    DEC    LOBYTE,SP       ; Point to WAIT/STOP opcode.
RETURN  PULH                   ; Restore H register.
        RTI
```

9.4.6 Reset Vector Fetch

A reset vector fetch occurs when the vector address appears on the data bus. A reset vector fetch clears the COP prescaler.

9.4.7 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register. See Configuration Register (CONFIG).

9.4.8 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register. See Configuration Register (CONFIG).

9.5 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 9-2. COP Control Register (COPCTL)

9.6 Interrupts

The COP does not generate CPU interrupt requests.

Table 15-1. Monitor Mode Signal Requirements and Options

$\overline{IRQ}$	RESET	$FFFE/$FFFF	PLL	PTB0	PTB1	External Clock(1)	CGMOUT	Bus Freq	COP	For Serial Communication			Comment
										PTA0	PTA1	Baud Rate(2) (3)	
X	GND	X	X	X	X	X	0	0	Disabled	X	X	0	No operation until reset goes high
V_{TST}	V_{DD} or V_{TST}	X	OFF	1	0	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PTB0 and PTB1 voltages only required if $\overline{IRQ} = V_{TST}$
										X	1	DNA	
V_{DD}	V_{DD}	$FFFF	OFF	X	X	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	External frequency always divided by 4
										X	1	DNA	
GND	V_{DD}	$FFFF	ON	X	X	32.768 kHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PLL enabled (BCS set) in monitor code
										X	1	DNA	
V_{DD} or GND	V_{TST}	$FFFF	OFF	X	X	X	—	—	Enabled	X	X	—	Enters user mode — will encounter an illegal address reset
V_{DD} or GND	V_{DD} or V_{TST}	Not $FFFF	OFF	X	X	X	—	—	Enabled	X	X	—	Enters user mode

Notes:

1. External clock is derived by a 32.768 kHz crystal or a 9.8304 MHz off-chip oscillator
2. PTA0 = 1 if serial communication; PTA0 = X if parallel communication
3. PTA1 = 0 → serial, PTA1 = 1 → parallel communication for security code entry
4. DNA = does not apply, X = don't care

If entering monitor mode with V_{TST} applied on $\overline{IRQ}$ (condition set 1), the CGMOUT frequency is equal to the CGMXCLK frequency and the OSC1 input directly generates internal bus clocks. In this case, the OSC1 signal must have a 50% duty cycle at maximum bus frequency.

If entering monitor mode without high voltage applied on $\overline{IRQ}$ (condition set 2 or 3, where applied voltage is either V_{DD} or V_{SS}), then all port B pin

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA)	Read:	0	0	0	0	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB)	Read:	0	0	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PTC)	Read:	0	0	0	0	0	0	PTC1	PTC0
		Write:								
		Reset:	Unaffected by reset							
$0003	Port D Data Register (PTD)	Read:	0	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
		Write:								
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA)	Read:	0	0	0	0	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB)	Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Data Direction Register C (DDRC)	Read:	0	0	0	0	0	0	DDRC1	DDRC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0007	Data Direction Register D (DDRD)	Read:	0	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-1. I/O Port Register Summary

16.5 Port C

Port C is a 2-bit, general-purpose bidirectional I/O port. Port C also has software configurable pullup devices if configured as an input port.

16.5.1 Port C Data Register

The port C data register (PTC) contains a data latch for each of the two port C pins.

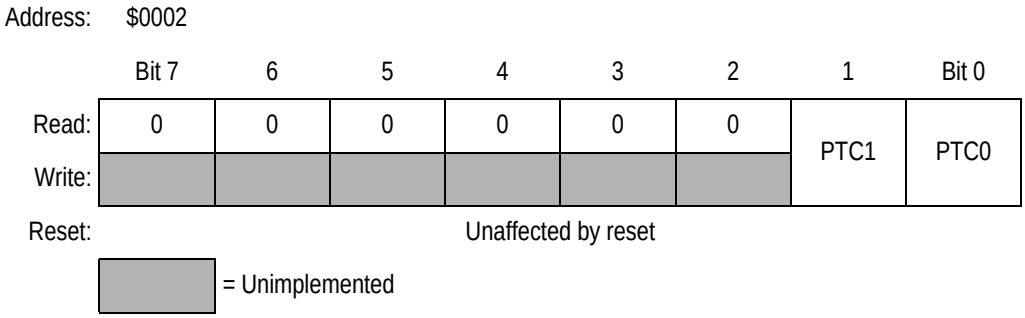

Figure 16-9. Port C Data Register (PTC)

PTC1–PTC0 — Port C Data Bits

These read/write bits are software-programmable. Data direction of each port C pin is under the control of the corresponding bit in data direction register C. Reset has no effect on port C data.

NOTE: PTC is not available in a 28-pin DIP and SOIC package

T1CH1 and T1CH0 — Timer 1 Channel I/O Bits

The PTD5/T1CH1–PTD4/T1CH0 pins are the TIM1 input capture/output compare pins. The edge/level select bits, ELSxB and ELSxA, determine whether the PTD5/T1CH1–PTD4/T1CH0 pins are timer channel I/O pins or general-purpose I/O pins. See Timer Interface Module (TIM).

SPSCK — SPI Serial Clock

The PTD3/SPSCK pin is the serial clock input of the SPI module. When the SPE bit is clear, the PTD3/SPSCK pin is available for general-purpose I/O.

MOSI — Master Out/Slave In

The PTD2/MOSI pin is the master out/slave in terminal of the SPI module. When the SPE bit is clear, the PTD2/MOSI pin is available for general-purpose I/O.

MISO — Master In/Slave Out

The PTD1/MISO pin is the master in/slave out terminal of the SPI module. When the SPI enable bit, SPE, is clear, the SPI module is disabled, and the PTD0/$\overline{SS}$ pin is available for general-purpose I/O.

Data direction register D (DDRD) does not affect the data direction of port D pins that are being used by the SPI module. However, the DDRD bits always determine whether reading port D returns the states of the latches or the states of the pins. See Table 16-5.

$\overline{SS}$ — Slave Select

The PTD0/$\overline{SS}$ pin is the slave select input of the SPI module. When the SPE bit is clear, or when the SPI master bit, SPMSTR, is set, the PTD0/$\overline{SS}$ pin is available for general-purpose I/O. When the SPI is enabled, the DDRB0 bit in data direction register B (DDRB) has no effect on the PTD0/$\overline{SS}$ pin.

16.6.3 Port D Input Pullup Enable Register

The port D input pullup enable register (PTDPUE) contains a software configurable pullup device for each of the seven port D pins. Each bit is individually configurable and requires that the data direction register, DDRD, bit be configured as an input. Each pullup is automatically and dynamically disabled when a port bit's DDRD is configured for output mode.

Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	PTDPUE6	PTDPUE5	PTDPUE4	PTDPUE3	PTDPUE2	PTDPUE1	PTDPUE0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 16-16. Port D Input Pullup Enable Register (PTDPUE)

PTDPUE6–PTDPUE0 — Port D Input Pullup Enable Bits

These writeable bits are software programmable to enable pullup devices on an input port bit.

1 = Corresponding port D pin configured to have internal pullup
0 = Corresponding port D pin has internal pullup disconnected

18.5.2.5 Inversion of Transmitted Output

The transmit inversion bit (TXINV) in SCI control register 1 (SCC1) reverses the polarity of transmitted data. All transmitted values, including idle, break, start, and stop bits, are inverted when TXINV is at logic 1. See SCI Control Register 1.

18.5.2.6 Transmitter Interrupts

These conditions can generate CPU interrupt requests from the SCI transmitter:

- SCI transmitter empty (SCTE) — The SCTE bit in SCS1 indicates that the SCDR has transferred a character to the transmit shift register. SCTE can generate a transmitter CPU interrupt request. Setting the SCI transmit interrupt enable bit, SCTIE, in SCC2 enables the SCTE bit to generate transmitter CPU interrupt requests.
- Transmission complete (TC) — The TC bit in SCS1 indicates that the transmit shift register and the SCDR are empty and that no break or idle character has been generated. The transmission complete interrupt enable bit, TCIE, in SCC2 enables the TC bit to generate transmitter CPU interrupt requests.

18.5.3 Receiver

Figure 18-5 shows the structure of the SCI receiver.

18.5.3.1 Character Length

The receiver can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCC1) determines character length. When receiving 9-bit data, bit R8 in SCI control register 2 (SCC2) is the ninth bit (bit 8). When receiving 8-bit data, bit R8 is a copy of the eighth bit (bit 7).

19.8.1 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from stop mode or wait mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note(1)	
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Note: 1. Writing a logic 0 clears SBSW.

Figure 19-20. SIM Break Status Register (SBSR)

SBSW — SIM Break Stop/Wait

This status bit is useful in applications requiring a return to wait or stop mode after exiting from a break interrupt. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Stop mode or wait mode was exited by break interrupt.

0 = Stop mode or wait mode was not exited by break interrupt.

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. The following code is an example of this. Writing 0 to the SBSW bit clears it.

```
This code works if the H register has been pushed onto the stack in the break
service routine software. This code should be executed at the end of the break
service routine software.

HIBYTE   EQU     5                   ;
LOBYTE   EQU     6                   ;
         If not SBSW, do RTI         ;
         BRCLR   SBSW,SBSR, RETURN   ;See if wait mode or stop mode was exited by
                                     ;break.
         TST     LOBYTE,SP           ;If RETURNLO is not zero,
         BNE     DOLO                ;then just decrement low byte.
```

Section 20. Serial Peripheral Interface (SPI)

20.1 Contents

20.2 Introduction

This section describes the serial peripheral interface (SPI) module, which allows full-duplex, synchronous, serial communications with peripheral devices.

The following paragraphs describe the operation of the SPI module.

20.5.1 Master Mode

The SPI operates in master mode when the SPI master bit, SPMSTR, is set.

NOTE: *Configure the SPI modules as master or slave before enabling them. Enable the master SPI before enabling the slave SPI. Disable the slave SPI before disabling the master SPI. See SPI Control Register.*

Only a master SPI module can initiate transmissions. Software begins the transmission from a master SPI module by writing to the transmit data register. If the shift register is empty, the byte immediately transfers to the shift register, setting the SPI transmitter empty bit, SPTE. The byte begins shifting out on the MOSI pin under the control of the serial clock. See Figure 20-3.

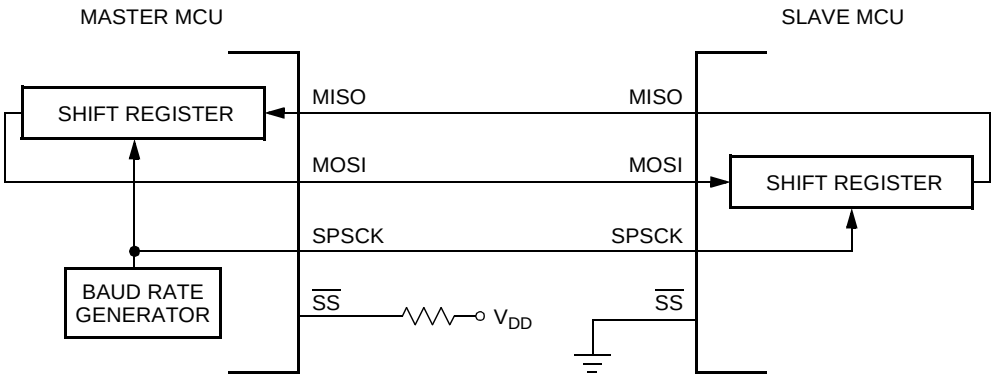

Figure 20-3. Full-Duplex Master-Slave Connections

SPR1 and SPR0 — SPI Baud Rate Select Bits

In master mode, these read/write bits select one of four baud rates as shown in Table 20-4. SPR1 and SPR0 have no effect in slave mode. Reset clears SPR1 and SPR0.

Table 20-4. SPI Master Baud Rate Selection

SPR1 and SPR0	Baud Rate Divisor (BD)
00	2
01	8
10	32
11	128

Use this formula to calculate the SPI baud rate:

$$\text{Baud rate} = \frac{\text{CGMOUT}}{2 \times \text{BD}}$$

where:

CGMOUT = base clock output of the clock generator module (CGM)
BD = baud rate divisor

Figure 22-2 summarizes the timer registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0020	Timer 1 Status and Control Register (T1SC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$0021	Timer 1 Counter Register High (T1CNTH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	Timer 1 Counter Register Low (T1CNTL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	Timer 1 Counter Modulo Register High (T1MODH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	Timer 1 Counter Modulo Register Low (T1MODL)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	Timer 1 Channel 0 Status and Control Register (T1SC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	Timer 1 Channel 0 Register High (T1CH0H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0027	Timer 1 Channel 0 Register Low (T1CH0L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0028	Timer 1 Channel 1 Status and Control Register (T1SC1)	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0029	Timer 1 Channel 1 Register High (T1CH1H)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$002A	Timer 1 Channel 1 Register Low (T1CH1L)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$002B	Timer 2 Status and Control Register (T2SC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$002C	Timer 2 Counter Register High (T2CNTH)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
			= Unimplemented							

Figure 22-2. TIM I/O Register Summary (Sheet 1 of 2)

23.5 5.0 V DC Electrical Characteristics

Table 23-4. 5.0V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.0 mA) all I/O pins (I_{Load} = –10.0 mA) all I/O pins (I_{Load} = –10.0 mA) pins PTC0–PTC1 only Maximum combined I_{OH} for port C, port E, port PTD0–PTD3 Maximum combined I_{OH} for port PTD4–PTD6, port A, port B Maximum total I_{OH} for all port pins	 V_{OH} V_{OH} V_{OH} I_{OH1} I_{OH2} I_{OHT}	 V_{DD} – 0.8 V_{DD} – 1.5 V_{DD} – 0.8 — — —	 — — — — — —	 — — — 50 50 100	 V V V mA mA mA
Output low voltage (I_{Load} = 1.6 mA) all I/O pins (I_{Load} = 10 mA) all I/O pins (I_{Load} = 15 mA) pins PTC0–PTC1 only Maximum combined I_{OL} for port C, port E, port PTD0–PTD3 Maximum combined I_{OL} for port PTD4–PTD6, port A, port B Maximum total I_{OL} for all port pins	 V_{OL} V_{OL} V_{OL} I_{OL1} I_{OL2} I_{OLT}	 — — — — — —	 — — — — — —	 0.4 1.5 1.0 50 50 100	 V V V mA mA mA
Input high voltage All ports, IRQs, RESET OSC1	V_{IH}	0.7 x V_{DD} 0.8 x V_{DD}	—	V_{DD}	V
Input low voltage All ports, IRQs, RESET, OSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
V_{DD} supply current Run[3] Wait[4]	I_{DD}	 — —	 15 4	 20 8	 mA mA
Stop[5] (<85 °C) Stop (>85 °C) Stop with TBM enabled[6] Stop with LVI and TBM enabled[6]	I_{DD}	— — — —	3 5 20 300	5 10 35 500	µA µA µA µA
I/O ports Hi-Z leakage current[7]	I_{IL}	—	—	±10	µA
Input current	I_{In}	—	—	1	µA