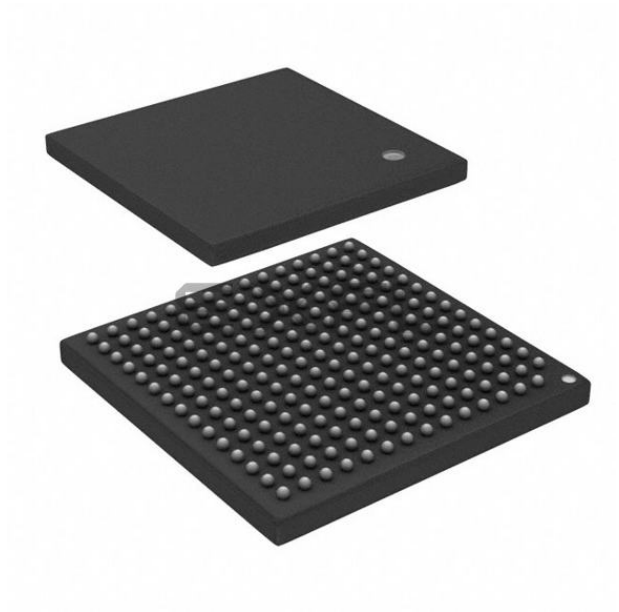
Renesas Electronics America Inc - R7FS7G27G2A01CBD#AC0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	172
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	224-LFBGA
Supplier Device Package	224-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27g2a01cbd-ac0

Table 1.3 System (2/2)

Feature	Functional description
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor reset 0 • Voltage monitor reset 1 • Voltage monitor reset 2 • Independent Watchdog Timer reset • Watchdog Timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM DED error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected in the software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer (WDT) on-chip oscillator • Clock out supports. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Low-power modes	Power consumption can be reduced in multiple ways, including by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low-power modes. See section 11, Low-Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Two MPUs and a CPU stack pointer monitor functions are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The WDT is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The IWDT consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Interrupt control

Feature	Functional description
Interrupt Controller Unit (ICU)	The ICU controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.

Table 1.5 Event link

Feature	Functional description
Event Link Controller (ELC)	The ELC uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.6 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A DTC module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMAC module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.7 External bus interface

Feature	Functional description
External buses	• CS area (EXBIU): Connected to the external devices (external memory interface) • SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.8 Timers

Feature	Functional description
General PWM Timer (GPT)	The GPT is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state.
Asynchronous General-Purpose Timer (AGT)	The AGT is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The RTC has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

1.5 Pin Functions

Table 1.16 Pin functions (1/5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect to the system power supply. Connect this pin to VSS through a 0.1-µF capacitor. Place the capacitor close to the pin.
	VCC_DCDC	Input	Switching regulator power supply pin.
	VLO	I/O	Switching regulator pin.
	VCL0 to VCL2	Input	Connect this pin to VSS through the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VCL_F	Input	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins.
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TDATA0 to TDATA3	Output	These pins indicate that output from the TDATA0 to TDATA3 pins is valid.
	SWDIO	I/O	Serial wire debug data input/output pin.
	SWCLK	Input	Serial wire clock pin.
	SWO	Output	Serial wire trace output pin.
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active LOW.
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active LOW.
	WR0, WR1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active LOW.
	BC0, BC1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active LOW.
	WAIT	Input	Input pin for wait request signals in access to the external space, active LOW.
	CS0 to CS7	Output	Select signals for CS areas, active LOW.
	A00 to A23	Output	Address bus.
	D00 to D15	I/O	Data bus.

Table 1.16 Pin functions (3/5)

Function	Signal	I/O	Description
SSI	SSISCK0	I/O	SSI serial bit clock pin.
	SSISCK1		
	SSIWS0	I/O	Word select pins.
	SSIWS1		
	SSITXD0	Output	Serial data output pins.
	SSIRXD0	Input	Serial data input pins.
	SSIDATA1	I/O	Serial data input/output pins.
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock).
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master.
	MISOA, MISOB	I/O	Input or output pins for data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection.
QSPI	QSPCLK	Output	QSPI clock output pin.
	QSSL	Output	QSPI slave output pin.
	QIO0 to QIO3	I/O	Data0 to Data3.
CAN	CRX0, CRX1	Input	Receive data.
	CTX0, CTX1	Output	Transmit data.
USBFS	VCC_USB	Input	Power supply pins.
	VSS_USB	Input	Ground pins.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. Connect this pin to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip.
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip.
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode.
USBHS	VCC_USBHS	Input	Power supply pin.
	VSS1_USBHS	Input	Ground pin.
	VSS2_USBHS	Input	Ground pin.
	AVCC_USBHS	Input	Analog power supply pin for the USBHS.
	AVSS_USBHS	Input	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin.
	PVSS_USBHS	Input	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin.
	USBHS_RREF	I/O	USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor (±1%).
	USBHS_DP	I/O	USB bus D+ data pin.
	USBHS_DM	I/O	USB bus D- data pin.
	USBHS_EXICEN	Output	Connect this pin to the OTG power supply IC.
	USBHS_ID	Input	Connect this pin to the OTG power supply IC.
	USBHS_VBUSEN	Output	VBUS power enable signal for USB.
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for USB.
	USBHS_VBUS	Input	USB cable connection monitor input pin.

Table 1.16 Pin functions (5/5)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the analog. Connect this pin to VCC.
	AVSS0	Input	Analog ground pin. Connect this pin to VSS.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to VCC when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12.
	VREFH	Input	Reference voltage input pin for the ADC12 (unit 1) and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if the ADC12 (unit 1) or DAC12 is not in use.
	VREFL	Input	Reference ground pin for the ADC12 and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin.
ADC12	AN000 to AN006, AN016 to AN021	Input	Input pins for the analog signals to be processed by the ADC12.
	AN100 to AN106, AN116 to AN120	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active LOW.
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	Differential input pins.
DAC12	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin.
	IVREF0 to IVREF3	Input	Reference voltage input pin for comparator.
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator.
CTSU	TS00 to TS17	Input	Capacitive touch detection pins (touch pins).
	TSCAP	–	Secondary power supply pin for the touch driver.
KINT	KR00 to KR07	Input	A key interrupt (KINT) can be generated by inputting a falling edge to the key interrupt input pins.
I/O ports	P000 to P007	Input	General-purpose input pin.
	P008 to P011, P014, P015	I/O	General-purpose input/output pins.
	P100 to P115	I/O	General-purpose input/output pins.
	P200	Input	General-purpose iInput pin.
	P201 to P207, P212, P213	I/O	General-purpose input/output pins.
	P300 to P315	I/O	General-purpose input/output pins.
	P400 to P415	I/O	General-purpose input/output pins.
	P500 to P515	I/O	General-purpose input/output pins.
	P600 to P615	I/O	General-purpose input/output pins.
	P700 to P713	I/O	General-purpose input/output pins.
	P800 to P813	I/O	General-purpose input/output pins.
	P900 to P915	I/O	General-purpose input/output pins.
	PA00 to PA15	I/O	General-purpose input/output pins.
	PB00 to PB07	I/O	General-purpose input/output pins.
GLCDC	LCD_DATA00 to LCD_DATA23	Output	Data output pin for panel.
	LCD_TCON0 to LCD_TCON3	Output	Output pins for panel timing adjustment.
	LCD_CLK	Output	Panel clock output pin.
	LCD_EXTCLK	Input	Panel clock source input pin.
PDC	PIXCLK	Input	Image transfer clock pin.
	VSYNC	Input	Vertical synchronization signal pin.
	HSYNC	Input	Horizontal synchronization signal pin.
	PIXD0 to PIXD7	Input	8-bit image data pins.
	PCKO	Output	Output pin for dot clock.

1.7 Pin Lists

Table 1.17 Pin list (1/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces									Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
N13	N13	1	N13	1	1	-	P400	-	-	-	-	GTIOC6A_A	-	-	SCK4_B	SCK7_A	SCL0_A	-	AUDIO_CLK	ET1_TX_CLK	-	-	-	ADTRG1_B	-	-	IRQ0	-
P15	R15	2	L11	2	2	-	P401	-	-	-	GETRGA_B	GTIOC6B_A	-	CTX0_B	CTS4_RTS4_B/SS4_B	TXD7_A/MOSI7_A/SDA7_A	SDA0_A	-	-	ET0_MDC	ET0_MDC	-	-	-	-	-	IRQ5-DS	-
N14	P14	3	M13	3	3	-	P402	-	-	AGTIO0_B/AGTIO1_B	-	-	RTCIC0	CRX0_B	-	RXD7_A/MISO7_A/SCL7_A	-	-	-	ET0_MDIO	ET0_MDIO	-	-	-	-	-	IRQ4-DS	-
N15	M12	4	K11	4	4	-	P403	-	-	AGTIO0_C/AGTIO1_C	-	GTIOC3A_B	RTCIC1	-	-	CTS7_RTS7_A/SS7_A	-	-	SSISCK0_A	ET1_MDC	ET1_MDC	-	-	-	-	-	-	PIXD7
K10	M13	5	L12	5	5	-	P404	-	-	-	-	GTIOC3B_B	RTCIC2	-	-	-	-	-	SSIWS0_A	ET1_MDIO	ET1_MDIO	-	-	-	-	-	-	PIXD6
M13	P15	6	L13	6	6	-	P405	-	-	-	-	GTIOC1A_B	-	-	-	-	-	-	SSITXD0_A	ET1_TX_EN	RMII1_TXD_EN	-	-	-	-	-	-	PIXD5
J9	N14	7	J10	7	7	-	P406	-	-	-	-	GTIOC1B_B	-	-	-	-	-	-	SSIRXD0_A	ET1_RX_ER	RMII1_TXD1	-	-	-	-	-	-	PIXD4
M14	N15	8	H10	8	-	-	P700	-	-	-	-	GTIOC5A_B	-	-	-	-	-	-	-	ET1_ETXD1	RMII1_TXD0	-	-	-	-	-	-	PIXD3
M15	M14	9	K12	9	-	-	P701	-	-	-	-	GTIOC5B_B	-	-	-	-	-	-	-	ET1_ETXD0	REF50CK1	-	-	-	-	-	-	PIXD2
K11	L12	10	K13	10	-	-	P702	-	-	-	-	GTIOC6A_B	-	-	-	-	-	-	-	ET1_ERXD1	RMII1_RXD0	-	-	-	-	-	-	PIXD1
J8	M15	11	J11	11	-	-	P703	-	-	-	-	GTIOC6B_B	-	-	-	-	-	-	-	ET1_ERXD0	RMII1_RXD1	-	-	-	-	-	-	PIXD0
J10	L13	12	H11	12	-	-	P704	-	-	-	-	-	-	-	-	-	-	-	-	ET1_RX_CLK	RMII1_RX_ER	-	-	-	-	-	-	HSYNC
L13	K12	13	G11	13	-	-	P705	-	-	-	-	-	-	-	-	-	-	-	-	ET1_CRS	RMII1_CRS_DV	-	-	-	-	-	-	PIXCLK
L14	L14	14	-	-	-	-	P706	-	-	-	-	-	-	-	-	RXD3_B/MISO3_B/SCL3_B	-	-	-	-	-	USBHS_OVRCURB	-	-	-	-	IRQ7	-
L15	L15	15	-	-	-	-	P707	-	-	-	-	-	-	-	-	TXD3_B/MOSI3_B/SDA3_B	-	-	-	-	-	USBHS_OVRCURA	-	-	-	-	IRQ8	-

Table 1.17 Pin list (7/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
A3	A3	85	D5	69	47	-	P303	A08	A08	-	-	GTIOC7B_A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
A2	B3	86	A2	70	48	-	P302	A07	A07	-	GTOUUP_A	GTIOC4A_A	-	-	TXD2_A/MOSI2_A/SDA2_A	-	-	SSLB3_B	-	-	-	-	-	-	-	-	IRQ5	LCD_DATA14_A
B3	A2	87	C3	71	49	-	P301	A06	A06	-	GTOULO_A	GTIOC4B_A	-	-	RXD2_A/MISO2_A/SCL2_A	-	-	SSLB2_B	-	-	-	-	-	-	-	-	IRQ6	LCD_DATA13_A
F5	C4	88	B2	72	50	TCK/SWCLK	P300	-	-	-	-	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-	-
B2	C3	89	A1	73	51	TMS/SWDIO	P108	-	-	-	-	GTIOC0B_A	-	-	-	CTS9_RTS9_B/SS9_B	-	SSLB0_B	-	-	-	-	-	-	-	-	-	-
B1	A1	90	D4	74	52	CLKOUT_B/TDO/SWO	P109	-	-	-	GTOVUP_A	GTIOC1A_A	-	CTX1_A	-	TXD9_B/MISO9_B/SDA9_B	-	MOSIB_B	-	-	-	-	-	-	-	-	-	-
C2	D3	91	B1	75	53	TDI	P110	-	-	-	GTOVLO_A	GTIOC1B_A	-	CRX1_A	CTS2_RTS2_B/SS2_B	RXD9_B/MISO9_B/SCL9_B	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	IRQ3	-
C1	D4	92	C2	76	54	-	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2_B	SCK9_B	-	RSPCKB_B	-	-	-	-	-	-	-	-	IRQ4	LCD_DATA12_A
C3	B2	93	D3	77	55	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2_B/MOSI2_B/SDA2_B	-	-	-	SSISCK0_B		-	-	-	-	-	-	-	LCD_DATA11_A
D3	B1	94	C1	78	56	-	P113	A03	A03	-	-	-	-	-	RXD2_B/MISO2_B/SCL2_B	-	-	-	SSIWS0_B		-	-	-	-	-	-	-	LCD_DATA10_A
E4	C2	95	E4	79	57	-	P114	A02	A02	-	-	-	-	-	-	-	-	-	SSIRXD0_B		-	-	-	-	-	-	-	LCD_DATA09_A
E3	C1	96	E3	80	58	-	P115	A01	A01	-	-	-	-	-	-	-	-	-	SSITXD0_B		-	-	-	-	-	-	-	LCD_DATA08_A
D1	E3	97	D2	81	-	VCC		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	E4	98	D1	82	-	VSS		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F4	D2	99	F4	83	59	-	P608	A00/BC0	A00/DQM1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A

Table 1.17 Pin list (9/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
J5	-	-	-	-	-		PA03	-	-	-	-	-	-	-	-	RXD7_B/MISO7_B/SCL7_B	-	-	-	-	-	-	-	-	-	-	IRQ9	-
H6	-	-	-	-	-		PA02	-	-	-	-	-	-	-	-	TXD7_B/MOSI7_B/SDA7_B	-	-	-	-	-	-	-	-	-	-	IRQ10	-
J6	H2	113	-	-	-		PA01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_B
J7	H4	114	-	-	-		PA00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_B
K5	J4	115	-	-	-		P607	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_B
K6	J1	116	-	-	-		P606	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_B
K1	J2	117	H2	93	-		P605	D11	DQ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K2	J3	118	G4	94	-		P604	D12	DQ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	K3	119	H3	95	-		P603	D13	DQ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L1	K1	120	J1	96	65		P602	EBCLK	SDCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_A
L2	K2	121	J2	97	66	-	P601	WR/WR0	DQM0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_A
L3	L1	122	H4	98	67	-	P600	RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA02_A
M2	K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M1	L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K4	L2	125	J3	101	68	-	P107	D07	DQ07	-	-	GTIOC8A_A	-	-	CTS8_RTS8_A/SS8_A	-	-	-	-	-	-	-	-	-	-	-	KR07	LCD_DATA01_A
L4	M1	126	K3	102	69	-	P106	D06	DQ06	-	-	GTIOC8B_A	-	-	SCK8_A	-	-	SSLA3_A	-	-	-	-	-	-	-	-	KR06	LCD_DATA00_A
M3	L3	127	J4	103	70	-	P105	D05	DQ05	-	GTETRGA_C	-	-	-	TXD8_A/MOSI8_A/SDA8_A	-	-	SSLA2_A	-	-	-	-	-	-	-	-	IRQ0/KR05	LCD_TCON3_A
N3	M2	128	L3	104	71	-	P104	D04	DQ04	-	GTETRGB_B	-	-	-	RXD8_A/MISO8_A/SCL8_A	-	-	SSLA1_A	-	-	-	-	-	-	-	-	IRQ1/KR04	LCD_TCON2_A

Derating is the systematic reduction of load for improved reliability.

Table 2.2 Recommended operating conditions

Item	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
Switching regulator power supply voltage	VCC_DCDC	When switching regulator is used	-	VCC	-	V
		When switching regulator is not used	-	0	-	V
VBATT power supply voltage	VBATT		2.0		3.6	V
Analog power supply voltages	AVCC0		-	VCC	-	V
	AVSS0		-	0	-	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) –40 to +105°C

Item	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1/2)

Item			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI	V_{IH}	VCC × 0.8	-	VCC + 0.3	V
			V_{IL}	–0.3	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15	V_{IH}	VCC × 0.7	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.3	
		ETHERC	V_{IH}	2.3	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	-	VCC + 0.3	
			V_{IL}	–0.3	-	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	-	5.8	
			V_{IL}	–0.3	-	0.8	

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}

Item			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008 to P011, P201,P212	-	I_{OH}	-	--	–2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015, P213, P400, P401, P511, P512	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P402 to P404	Low drive*1	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins)	Low drive*1	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	–20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	–2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	–16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P008 to P011, P201,P212	-	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015, P213, P400, P401, P511, P512	-	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P402 to P404	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins)	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	–40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	–4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	–8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	–32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value total pins)	Maximum of all output pins		$\Sigma I_{OH\ (max)}$	-	-	–80	mA
			$\Sigma I_{OL\ (max)}$	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

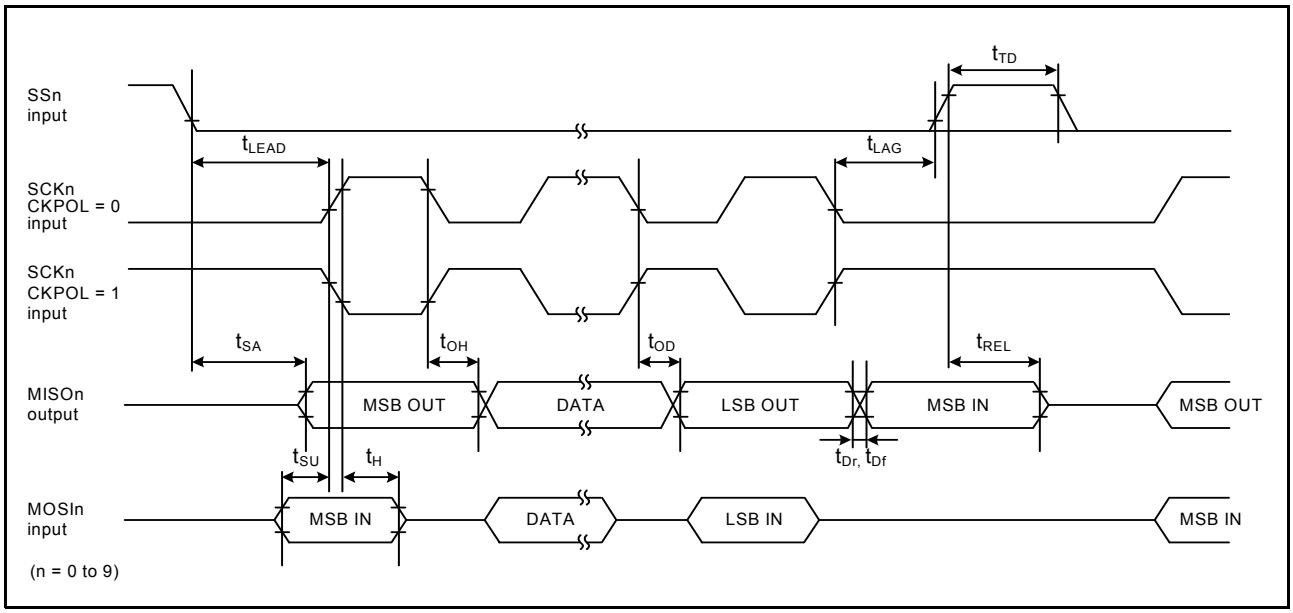

Figure 2.40 SCI simple SPI mode timing for slave when CKPH = 1

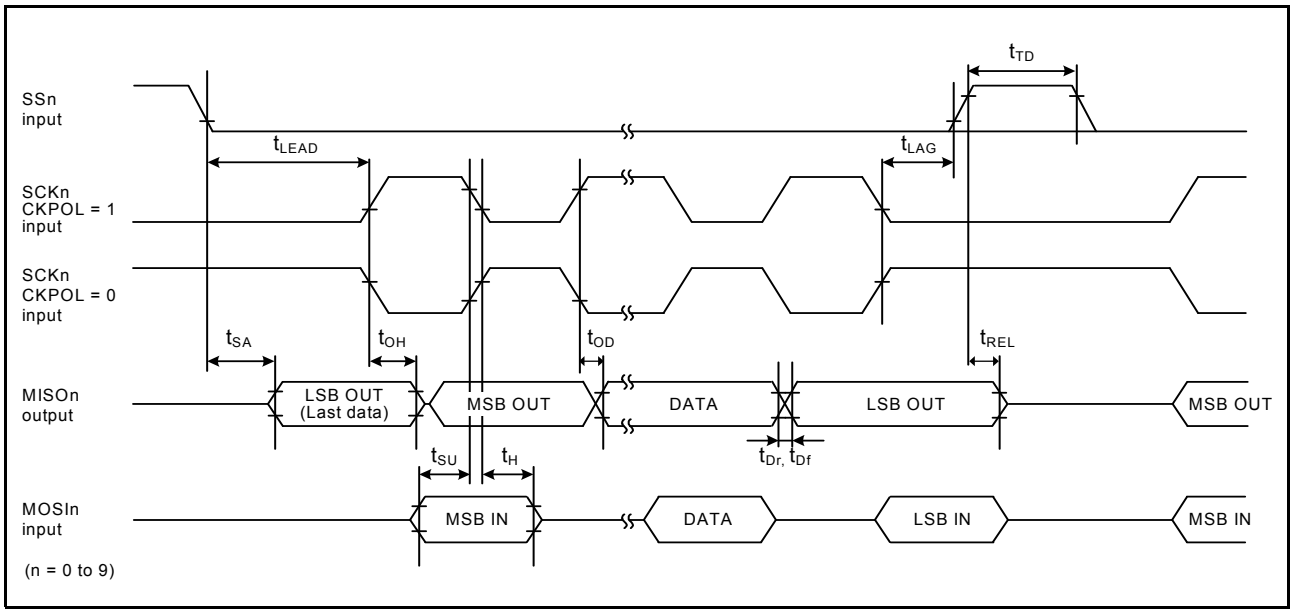

Figure 2.41 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1/2)

Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.42
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Table 2.24 SCI timing (3) (2/2)
Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	-	300	ns	Figure 2.42
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Note: SCL1_A output is not supported in these specifications.
t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKA cycle.
Note 1. Cb indicates the total capacity of the bus line.

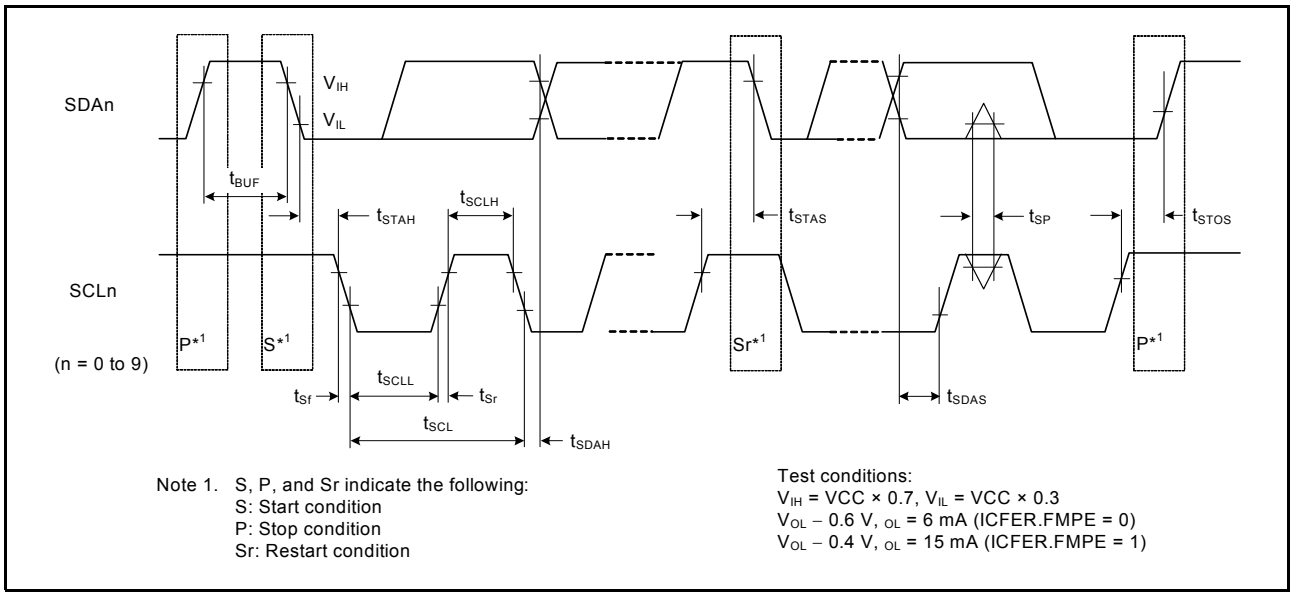

Figure 2.42 SCI simple IIC mode timing

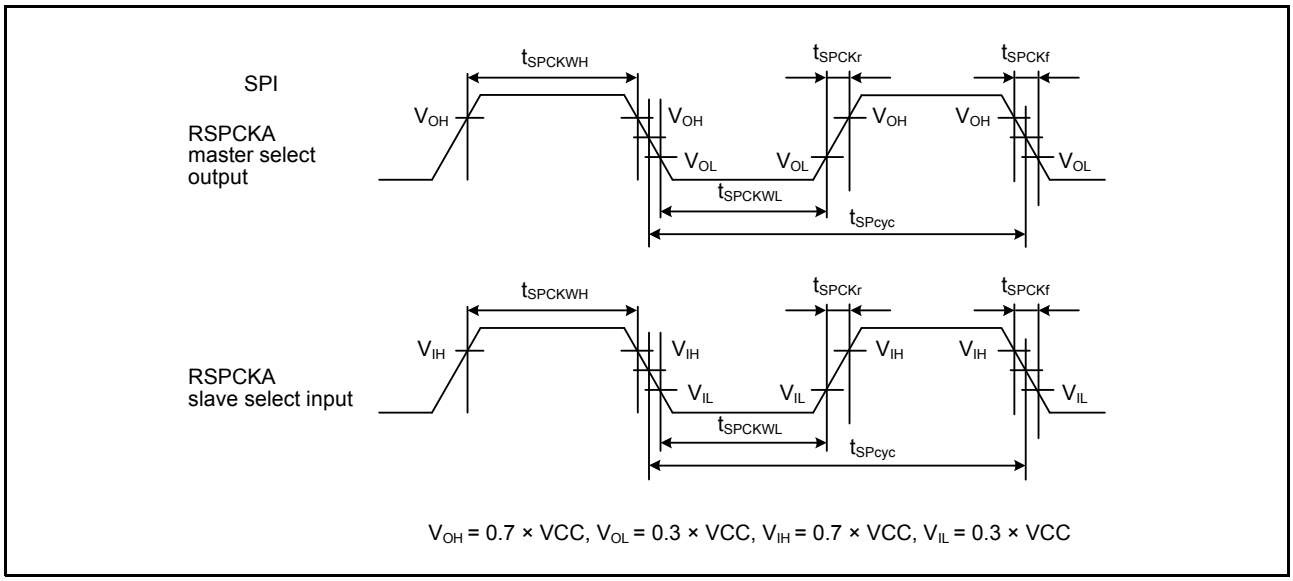

Figure 2.43 SPI clock timing

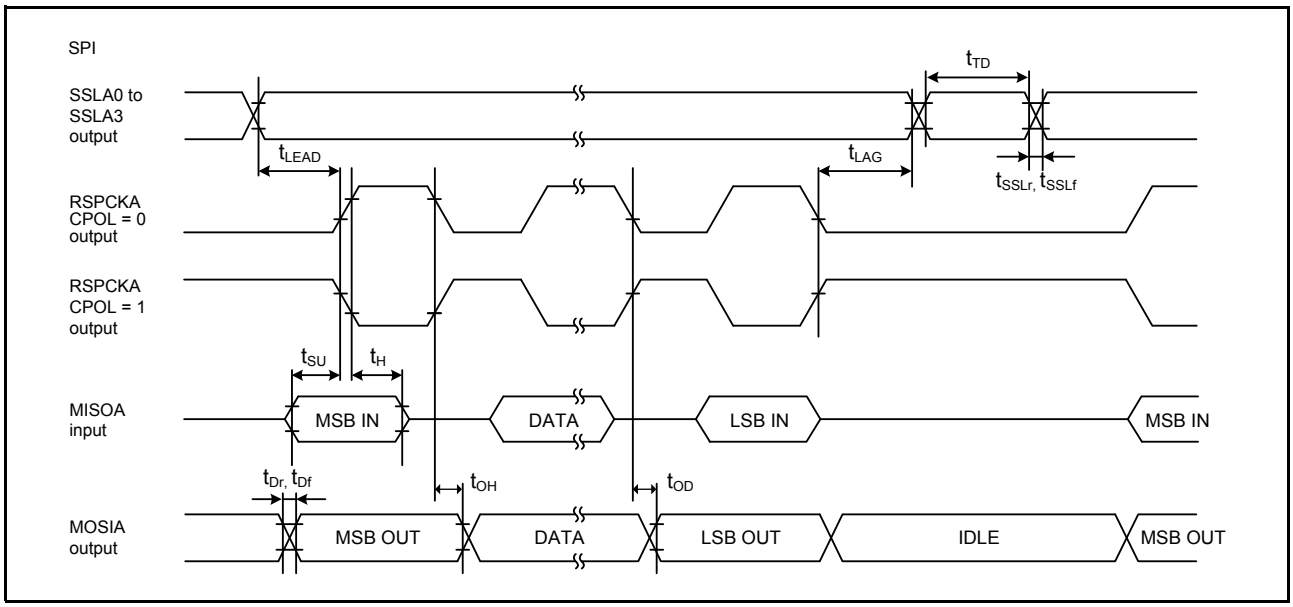

Figure 2.44 SPI timing for master when CPHA = 0

Table 2.28 IIC timing (2)

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3(6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

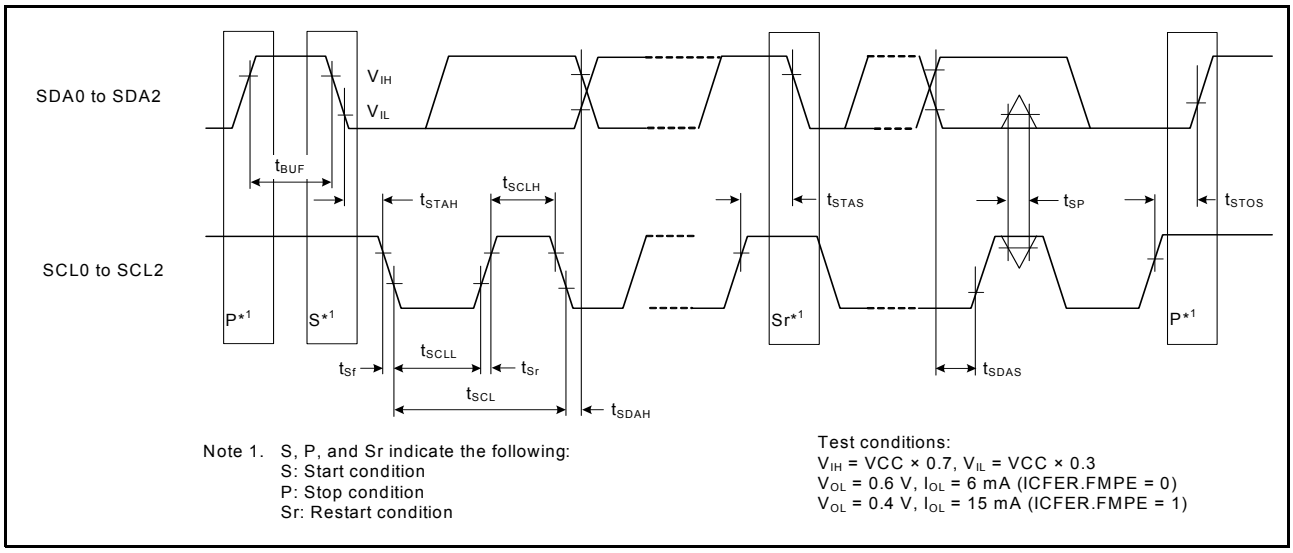

Figure 2.52 I²C bus interface input/output timing

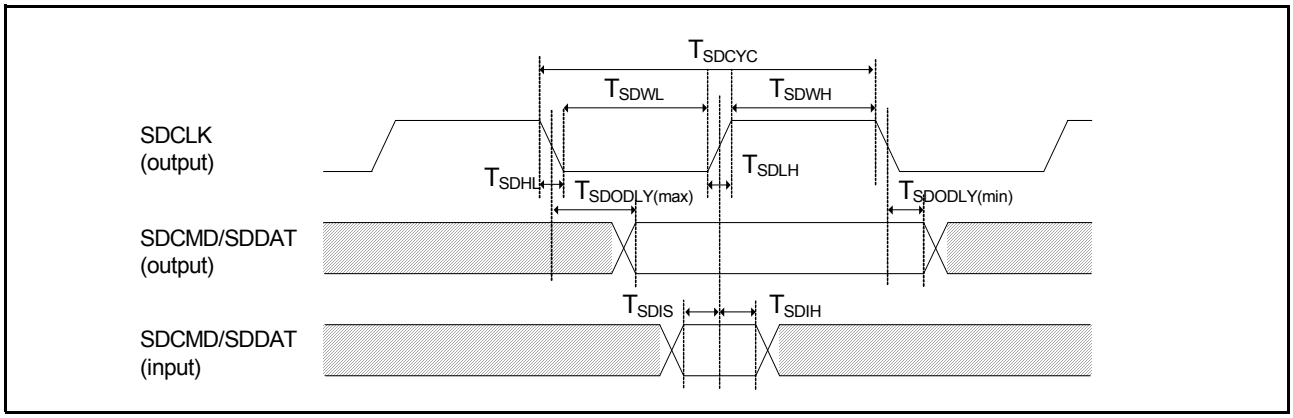

Figure 2.57 SD/MMC Host Interface signal timing

2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO, ET1_MDC, and ET1_MDIO
For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	-	ns	Figure 2.58 to Figure 2.61
	REF50CK frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay	T_{co}	2.5	12.0	ns	
	RMII_xxxx*2 setup time	T_{su}	3	-	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	-	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.4	4	ns	
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.62
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	-	ns	-
	ET_TX_EN output delay	t_{TENd}	1	20	ns	Figure 2.63
	ET_ETXD0 to ET_ETXD3 output delay	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	-	ns	
	ET_CRS hold time	t_{CRSh}	10	-	ns	
	ET_COL setup time	t_{COLs}	10	-	ns	Figure 2.64
	ET_COL hold time	t_{COLh}	10	-	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	-	ns	-
	ET_RX_DV setup time	t_{RDVs}	10	-	ns	Figure 2.65
	ET_RX_DV hold time	t_{RDVh}	10	-	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	-	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	-	ns	
	ET_RX_ER setup time	t_{RERs}	10	-	ns	Figure 2.66
	ET_RX_ER hold time	t_{RESh}	10	-	ns	
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.67

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.

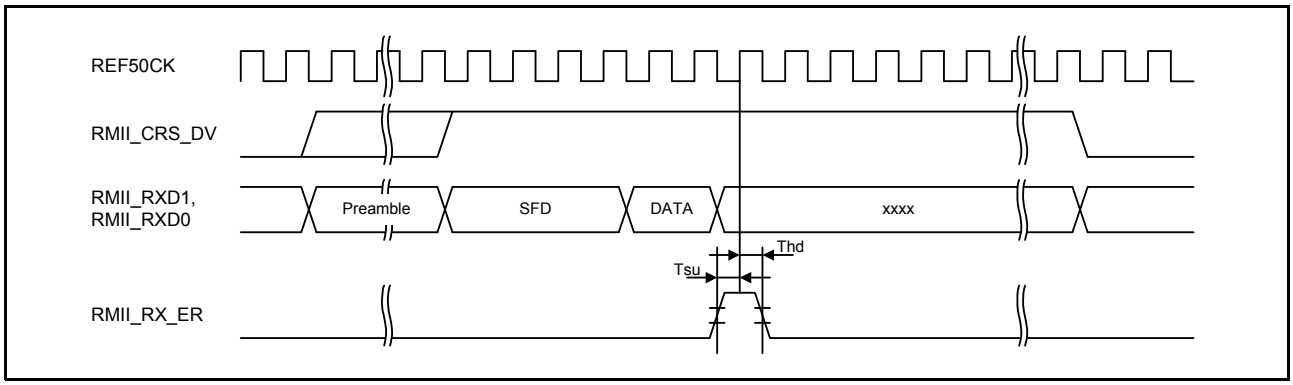

Figure 2.61 RMII reception timing when an error occurs

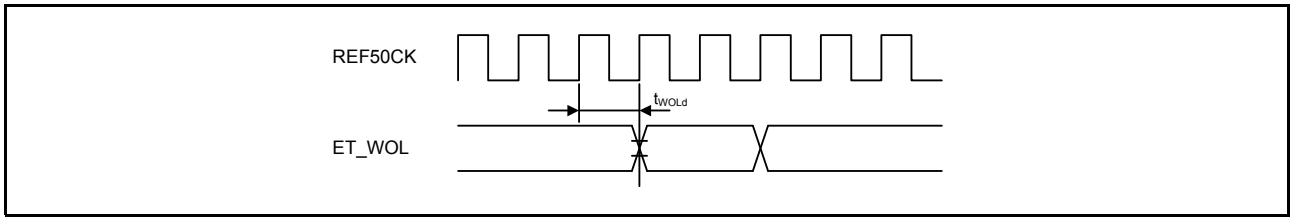

Figure 2.62 WOL output timing for RMII

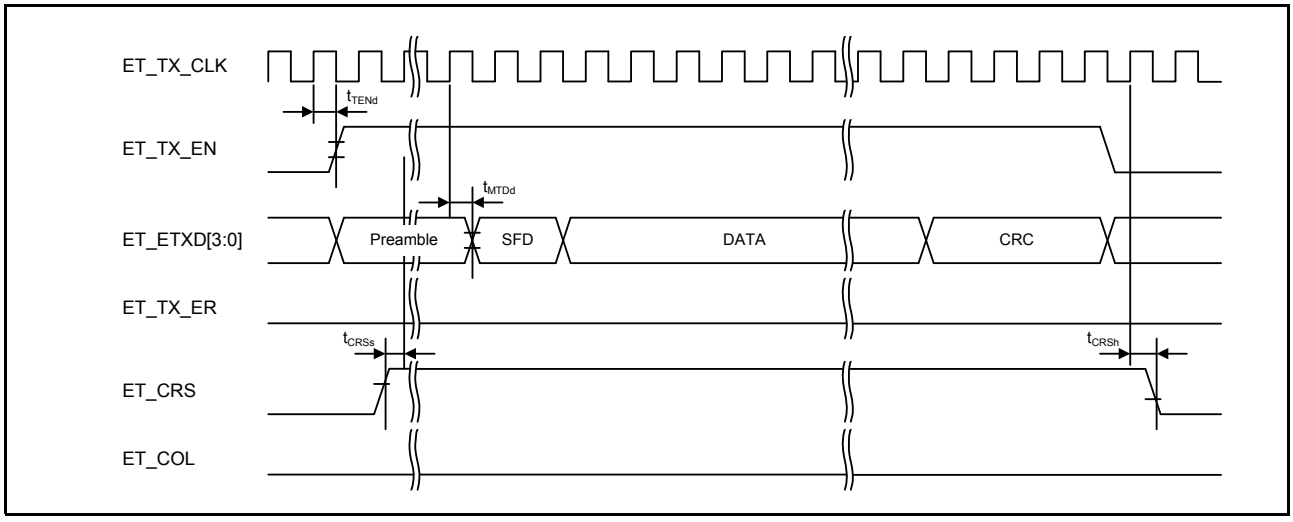

Figure 2.63 MII transmission timing in normal operation

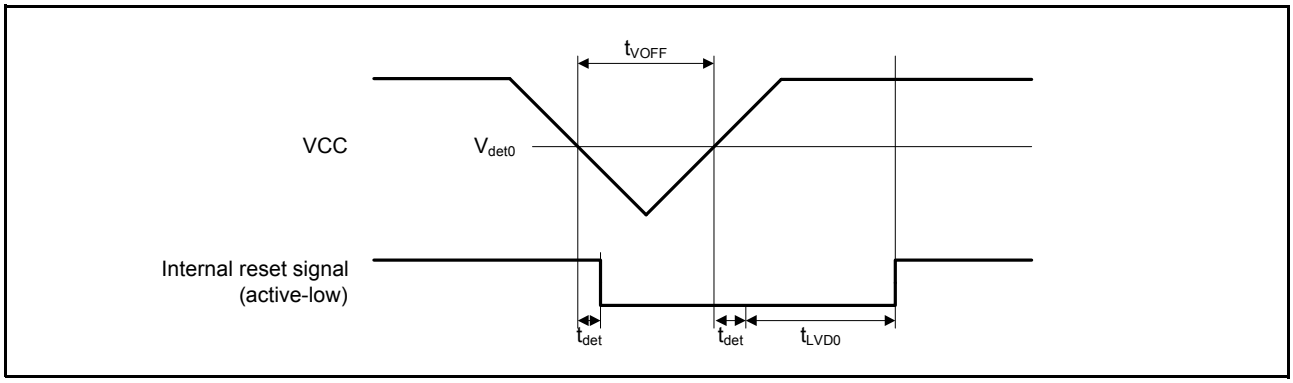

Figure 2.90 Voltage detection circuit timing (V_{det0})

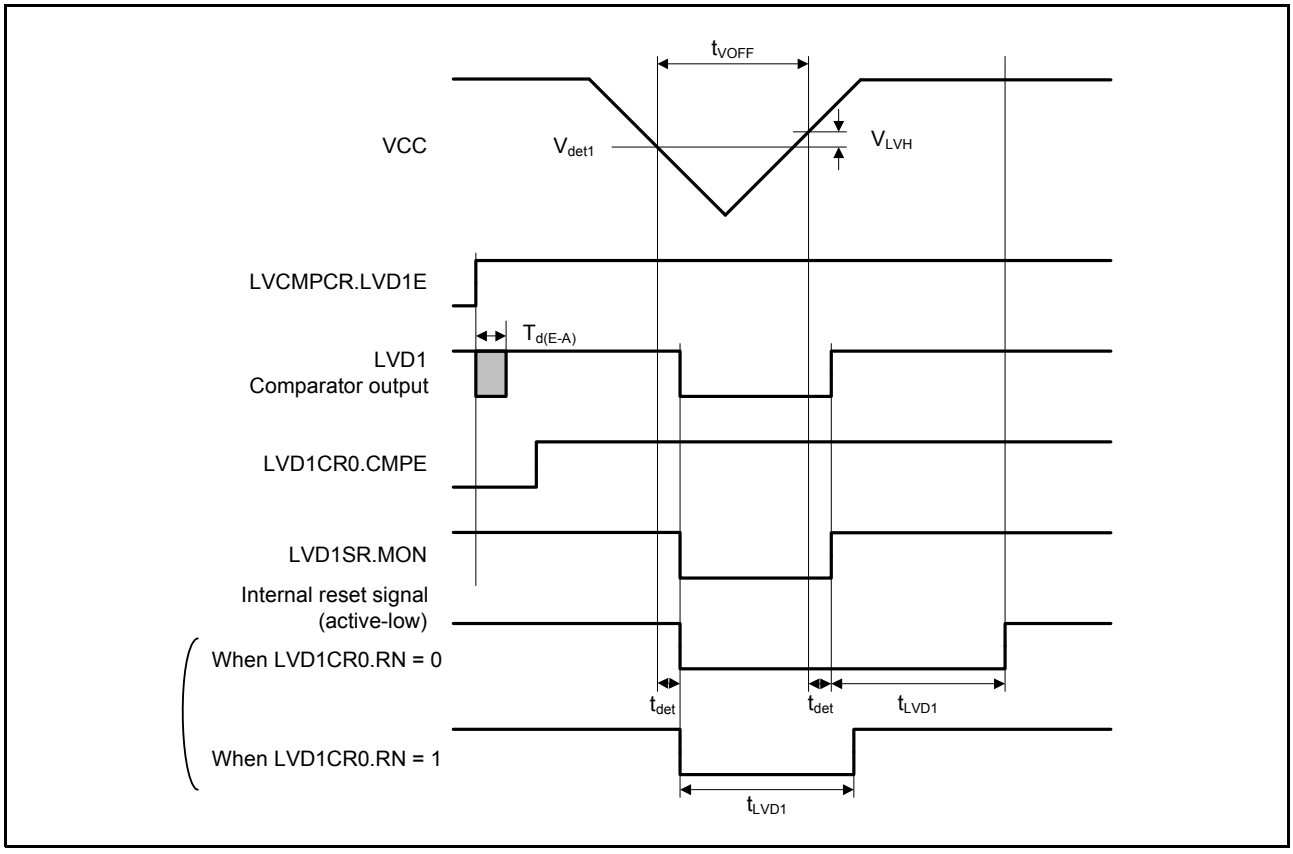

Figure 2.91 Voltage detection circuit timing (V_{det1})

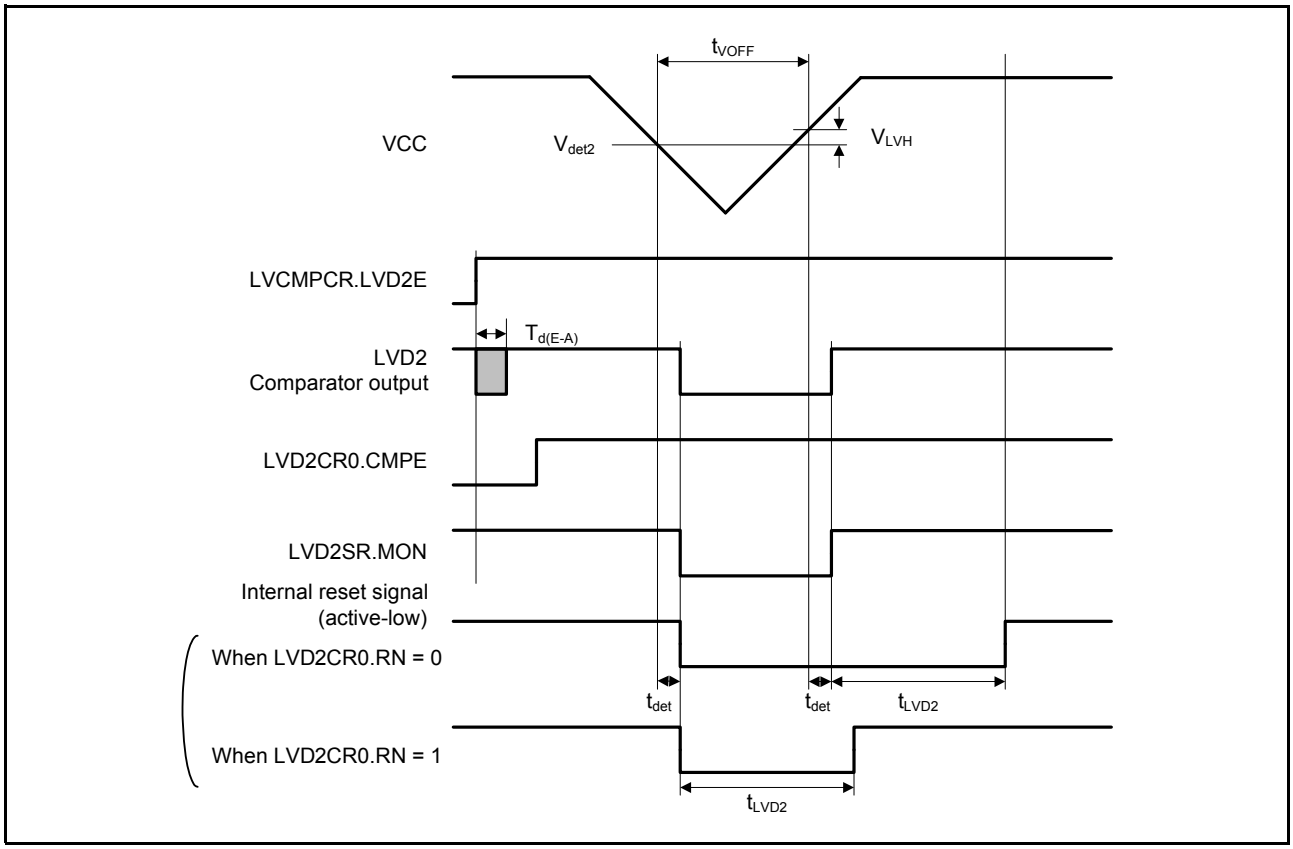

Figure 2.92 Voltage detection circuit timing (V_{det2})

2.10 VBATT Characteristics

Table 2.47 Battery backup function characteristics
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 2.0 to 3.6 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.93
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	-	-	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

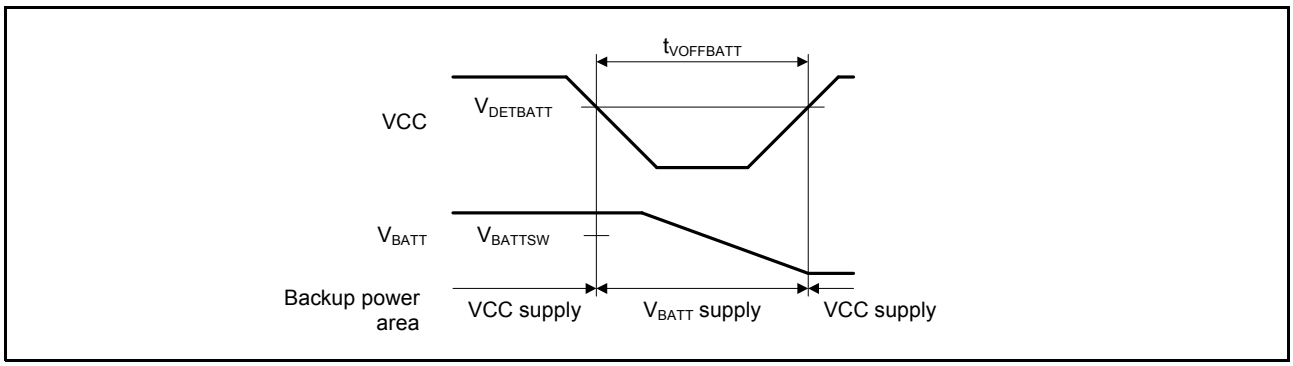

Figure 2.93 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.48 CTSU characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{oH}	-	-	-40	mA	When the mutual capacitance method is applied

2.12 Comparator Characteristics

Table 2.49 ACMPHS characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV

Note 1. This value is the internal propagation delay.

2.13 PGA Characteristics

Table 2.50 PGA characteristics in single mode (1/2)

Item	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V

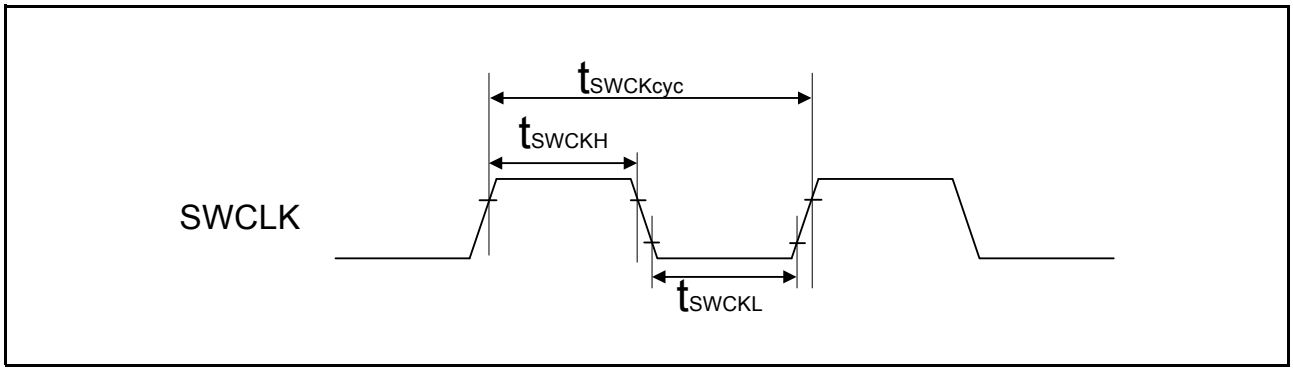

Figure 2.100 SWD SWCLK timing

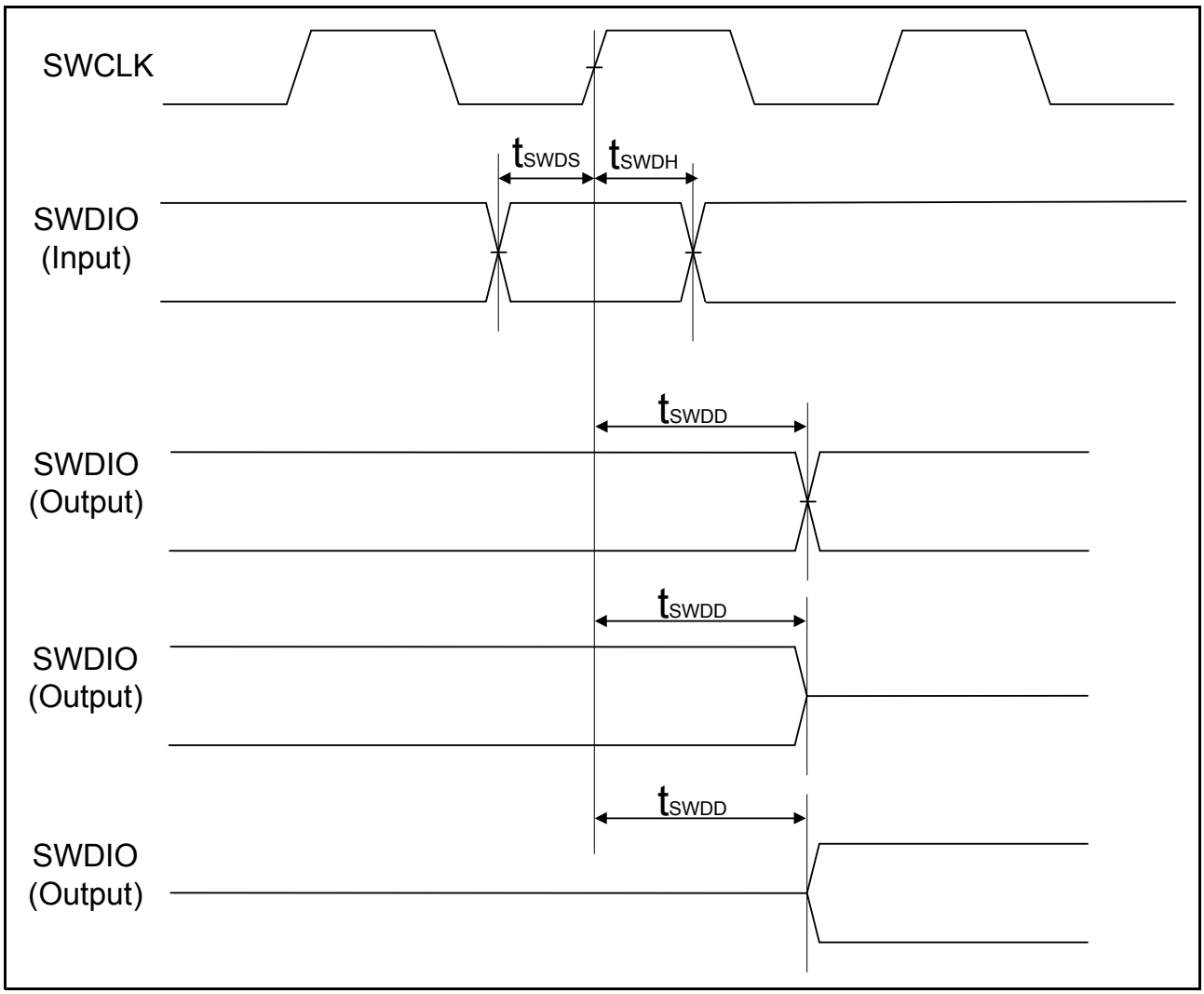

Figure 2.101 SWD input/output timing