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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	126
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 21x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27g2a01cbg-ac0

Table 1.9 Communication interfaces (2/2)

Feature	Functional description
Ethernet MAC with IEEE 1588 PTP (ETHERC)	Two-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. Each ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: • Synchronization Frame Processing units (SYNFP0 and SYNFP1) • A Packet Relation Controller unit (PRC-TC) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface provide the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-, 4-, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.10 Analog

Feature	Functional description
12-Bit A/D Converter (ADC12)	Up to two successive approximation 12-Bit A/D Converters are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 12 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 46, 12-Bit A/D Converter (ADC12) in User's Manual.
12-Bit D/A Converter (DAC12)	The DAC12 D/A converts data and includes an output amplifier. See section 47, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature sensor (TSN)	The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 48, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	Analog comparators can be used to compare a test voltage with a reference voltage and to provide a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 49, High-Speed Analog Comparator (ACMPHS) in User's Manual.

Table 1.11 Human machine interfaces (1/2)

Feature	Functional description
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.

1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

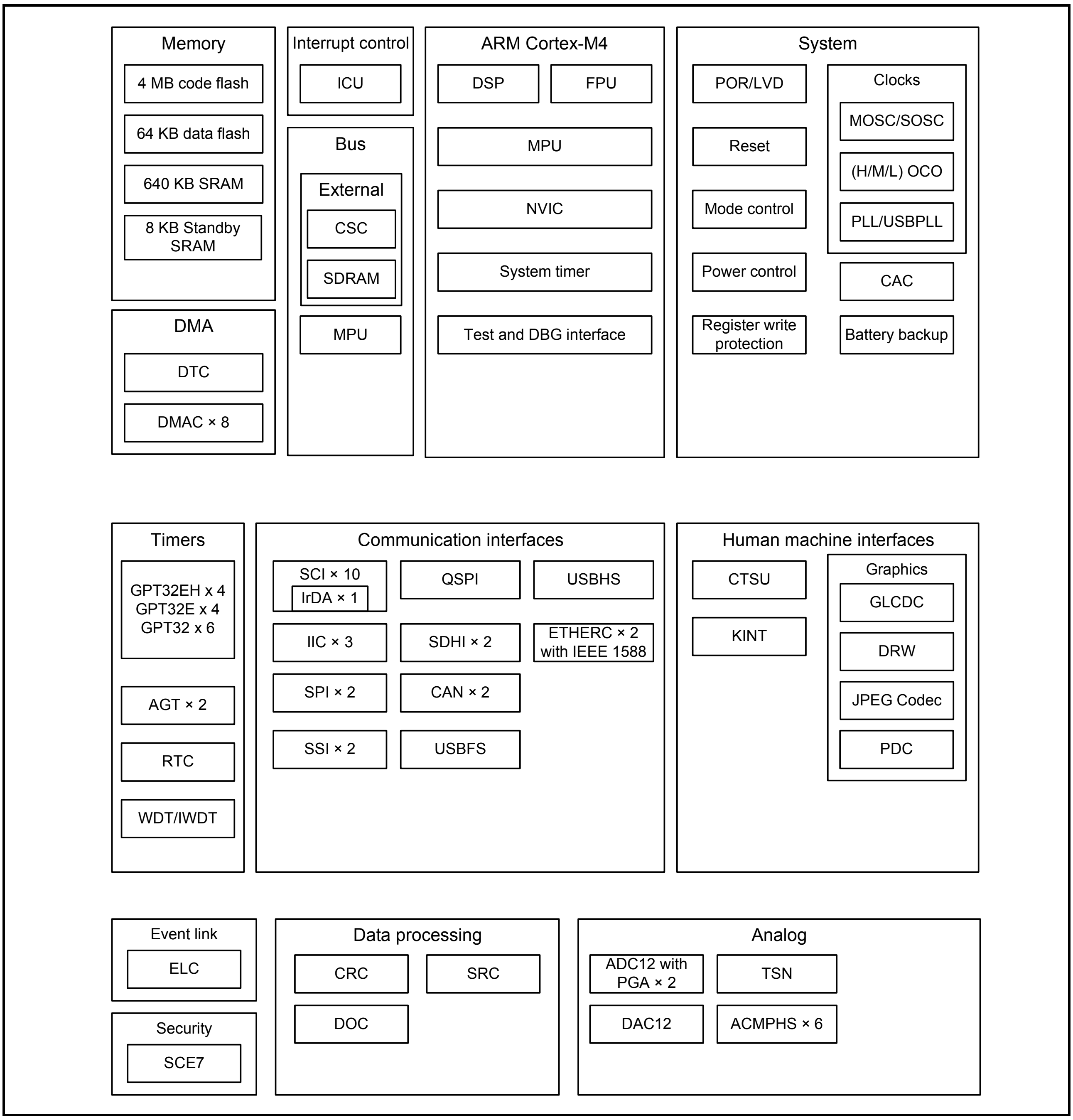


Figure 1.1 Block diagram

1.4 Function Comparison

Table 1.15 Functional comparison

Function			Part numbers					
			R7FS7G27H2A01CBD/ R7FS7G27G2A01CBD	R7FS7G27H2A01CBG/ R7FS7G27G2A01CBG	R7FS7G27H3A01CFC/ R7FS7G27G3A01CFC	R7FS7G27H2A01CLK/ R7FS7G27G2A01CLK	R7FS7G27H3A01CFB/ R7FS7G27G3A01CFB	R7FS7G27G3A01CFP
Pin count			224	176	176	145	144	100
Package			BGA	BGA	LQFP	LGA	LQFP	LQFP
Code flash memory			4/3 MB					3 MB
Data flash memory			64 KB					
SRAM			640 KB					
		Parity	608 KB					
		DED	32 KB					
Standby SRAM			8 KB					
System		CPU clock	240 MHz					
		Backup registers	512 bytes					
Interrupt control		ICU	Yes					
Event link		ELC	Yes					
DMA		DTC	Yes					
		DMAC	8					
BUS		External bus	16-bit bus					8-bit bus
		SDRAM	Yes					No
Timers		GPT32EH	4	4	4	4	4	4
		GPT32E	4	4	4	4	4	3
		GPT32	6	6	6	6	6	5
		AGT	2	2	2	2	2	2
		RTC	Yes					
		WDT/IWDT	Yes					
Communication		SCI	10					
		IIC	3					2
		SPI	2					
		SSI	2					1
		QSPI	1					Dual-SPI 1
		SDHI	2					
		CAN	2					
		USBFS	Yes					
		USBHS	Yes			No		
		ETHERC	2	RMII 2	RMII 2	RMII 2/MII 1		RMII 1
Analog		ADC12	25	21	21	19	19	16
		DAC12	2					
		ACMPHS	6					
		TSN	Yes					
HMI		CTSU	18	12	12	18		12
		KINT	8					
	Graphics	GLCDC	RGB888					RGB565
		DRW	Yes					
		JPEG	Yes					
		PDC	Yes					No
Data processing		CRC	Yes					
		DOC	Yes					
		SRC	Yes					
Security			SCE7					

Table 1.16 Pin functions (4/5)

Function	Signal	I/O	Description
ETHERC	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timing in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	Indicate carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode.
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode.
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode.
	RMII0_RX_ER, RMII1_RX_ER	Input	Indicate an error occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable signals.
	ET0_RX_DV, ET1_RX_DV	Input	Indicate valid receive data on ET_ERXD3 to ET_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Input	General-purpose external output pins.
	ET0_LINKSTA, ET1_LINKSTA	Output	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	output	4 bits of MII transmit data.
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data.
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable signals. Function as signals indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timing from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timing to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer through ET_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management data with PHY-LSI.
SDHI	SD0CLK, SD1CLK	Output	SD clock output pin.
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pin.
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins.
	SD0CD, SD1CD	Input	SD card detection pin.
	SD0WP, SD1WP	Input	SD write-protect signal.

1.7 Pin Lists

Table 1.17 Pin list (1/12)

Pin number						Power, System, Clock, Debug,		Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100		I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
N13	N13	1	N13	1	1	-	P400	-	-	-	-	GTIOC6A_A	-	-	SCK4_B	SCK7_A	SCL0_A	-	AUDIO_CLK	ET1_TX_CLK	-	-	-	ADTRG1_B	-	-	IRQ0	-
P15	R15	2	L11	2	2	-	P401	-	-	-	GTETRGA_B	GTIOC6B_A	-	CTX0_B	CTS4_RTS4_B/SS4_B	TXD7_A/MOSI7_A/SDA7_A	SDA0_A	-	-	ET0_MDC	ET0_MDC	-	-	-	-	-	IRQ5-DS	-
N14	P14	3	M13	3	3	-	P402	-	-	AGTIO0_B/AGTIO1_B	-	-	RTCIC0	CRX0_B	-	RXD7_A/MISO7_A/SCL7_A	-	-	-	ET0_MDIO	ET0_MDIO	-	-	-	-	-	IRQ4-DS	-
N15	M12	4	K11	4	4	-	P403	-	-	AGTIO0_C/AGTIO1_C	-	GTIOC3A_B	RTCIC1	-	-	CTS7_RTS7_A/SS7_A	-	-	SSISCK0_A	ET1_MDC	ET1_MDC	-	-	-	-	-	-	PIXD7
K10	M13	5	L12	5	5	-	P404	-	-	-	-	GTIOC3B_B	RTCIC2	-	-	-	-	-	SSIWS0_A	ET1_MDIO	ET1_MDIO	-	-	-	-	-	-	PIXD6
M13	P15	6	L13	6	6	-	P405	-	-	-	-	GTIOC1A_B	-	-	-	-	-	-	SSITXD0_A	ET1_TX_EN	RMII1_TXD_EN	-	-	-	-	-	-	PIXD5
J9	N14	7	J10	7	7	-	P406	-	-	-	-	GTIOC1B_B	-	-	-	-	-	-	SSIRXD0_A	ET1_RX_ER	RMII1_TXD1	-	-	-	-	-	-	PIXD4
M14	N15	8	H10	8	-	-	P700	-	-	-	-	GTIOC5A_B	-	-	-	-	-	-	-	ET1_ETXD1	RMII1_TXD0	-	-	-	-	-	-	PIXD3
M15	M14	9	K12	9	-	-	P701	-	-	-	-	GTIOC5B_B	-	-	-	-	-	-	-	ET1_ETXD0	REF50CK1	-	-	-	-	-	-	PIXD2
K11	L12	10	K13	10	-	-	P702	-	-	-	-	GTIOC6A_B	-	-	-	-	-	-	-	ET1_ERXD1	RMII1_RXD0	-	-	-	-	-	-	PIXD1
J8	M15	11	J11	11	-	-	P703	-	-	-	-	GTIOC6B_B	-	-	-	-	-	-	-	ET1_ERXD0	RMII1_RXD1	-	-	-	-	-	-	PIXD0
J10	L13	12	H11	12	-	-	P704	-	-	-	-	-	-	-	-	-	-	-	-	ET1_RX_CLK	RMII1_RX_ER	-	-	-	-	-	-	HSYNC
L13	K12	13	G11	13	-	-	P705	-	-	-	-	-	-	-	-	-	-	-	-	ET1_CRS	RMII1_CRS_DV	-	-	-	-	-	-	PIXCLK
L14	L14	14	-	-	-	-	P706	-	-	-	-	-	-	-	-	RXD3_B/MISO3_B/SCL3_B	-	-	-	-	-	USBHS_OVRCURB	-	-	-	-	IRQ7	-
L15	L15	15	-	-	-	-	P707	-	-	-	-	-	-	-	-	TXD3_B/MOSI3_B/SDA3_B	-	-	-	-	-	USBHS_OVRCURA	-	-	-	-	IRQ8	-

Table 1.17 Pin list (11/12)

Pin number								Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug,	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
P5	N5	143	K5	116	79	-	P503	-	-	-	GTETRGC_B	GTIOC12B	-	USB_EXICEN_B	CTS6_RTS6_B/SS6_B	SCK5_A	-	QIO1	-	-	-	-	SD1DAT1	AN117	-	-		-
R5	P5	144	L5	117	80	-	P504	-	-	-	GTETRGD_B	GTIOC13A	-	USB_ID_B	SCK6_B	CTS5_RTS5_A/SS5_A		QIO2	-	-	-	-	SD1DAT2	AN018	-	-		-
M5	P6	145	K6	118	-	-	P505	-	-	-	-	GTIOC13B	-	-	RXD6_B/MISO6_B/SCL6_B	-	-	QIO3	-	-	-	-	SD1DAT3	AN118	-	-	IRQ14	-
M6	R5	146	L6	119	-	-	P506	-	-	-	-	-	-	-	TXD6_B/MOSI6_B/SDA6_B	-	-	-	-	-	-	-	SD1CD	AN019	-	-	IRQ15	-
N6	N6	147	-	-	-	-	P507	-	-	-	-	-	-	-		CTS5_RTS5_B/SS5_B	-	-	-	-	-	-	SD1WP	AN119	-	-	-	-
M7	-	-	-	-	-	-	P508	-	-	-	-	-	-	-		SCK5_B	-	-	-	-	-	-	-	AN020	-	-	-	-
P6	-	-	-	-	-	-	P509	-	-	-	-	-	-	-		TXD5_B/MOSI5_B/SDA5_B	-	-	-	-	-	-	-	AN120	-	-	-	-
N7	-	-	-	-	-	-	P510	-	-	-	-	-	-	-	-	RXD5_B/MISO5_B/SCL5_B	-	-	-	-	-	-	-	AN021	-	-	-	-
R6	R6	148	N4	120	81	VCL2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R7	N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	P7	151	M6	123	84	-	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	IRQ13	-
M9	R7	152	N6	124	85	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-	-
N8	P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P8	N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. When the following ports are configured for high driving ability, they shift to middle driving ability during Deep Software Standby mode: P203 to P207, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01.
Note 4. Except for P000 to P007, P200, which are input ports.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1	V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*2	V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
		V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
		V_{OL}	-	-	0.4		I_{OL} = 1.0 mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins)*3	V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
		V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\lvert I_{in}\rvert$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P007, P200		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\lvert I_{TSI}\rvert$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB (except for ports P000 to P007)	I_p	–300	-	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015,P400, P415, P401, P511, P512	C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	Other input pins		-	-	8		

Note 1. SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B, SCL2, SDA2 (total 8 pins).
Note 2. SCL0_A, SDA0_A (total 2 pins).
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. Even when high driving ability is selected, I_{OH} and I_{OL} shift to middle driving ability during Deep Software Standby mode.

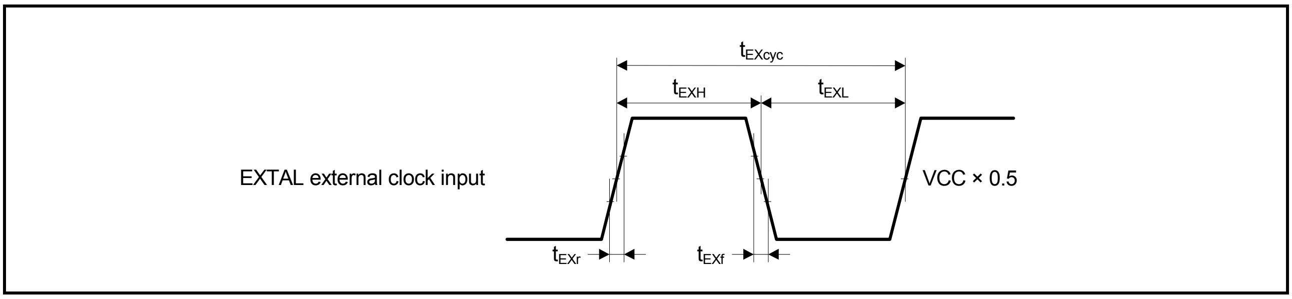


Figure 2.4 EXTAL external clock input timing

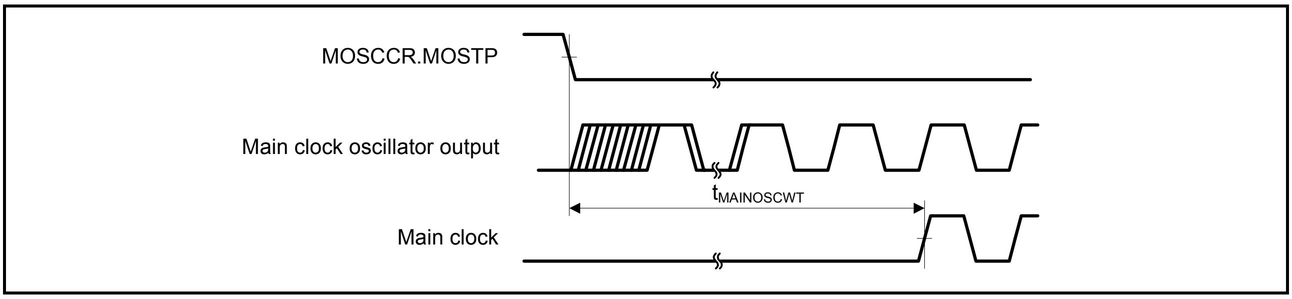


Figure 2.5 Main clock oscillation start timing

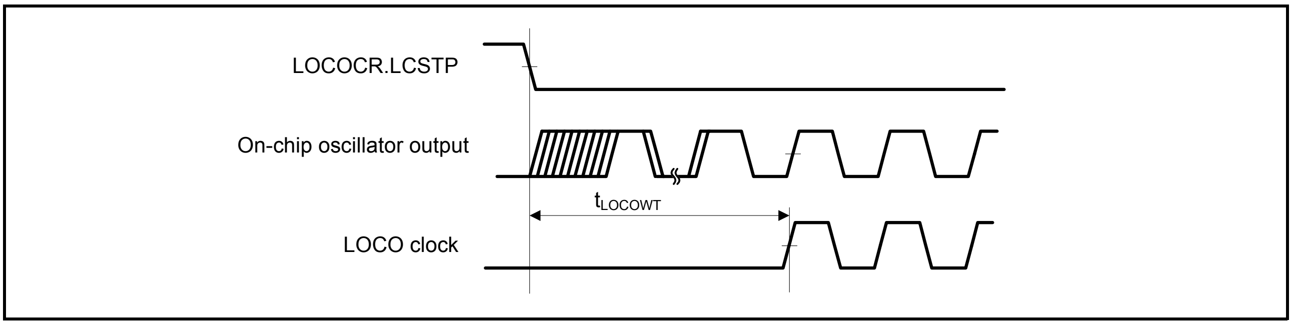


Figure 2.6 LOCO clock oscillation start timing

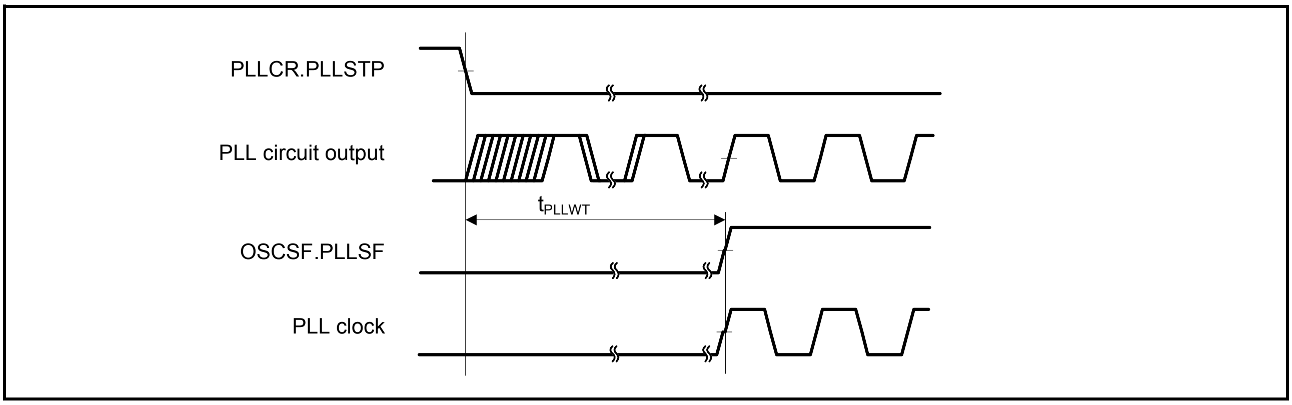


Figure 2.7 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

equation:

t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, 86 µs is added as the power supply recovery time.

Note 10. This defines the duration of Normal mode after a transition from Snooze to Normal mode.
The following cases are valid uses of the main clock oscillator:
- The crystal resonator is connected to main clock oscillator
- The external clock is input to main clock oscillator.
The following cases are excluded:
- The main clock resonator is not connected to the system clock source
- Transition is made from Software Standby to Normal mode.

Note 11. The same value as set in MOSCWTCR.MSTS[3:0]. Duration of Normal mode must be longer than the main clock oscillator wait time.
MOSCWTCR: Main Clock Oscillator Wait Control Register
$t_{cycmosc}$: Main clock oscillator frequency cycle.

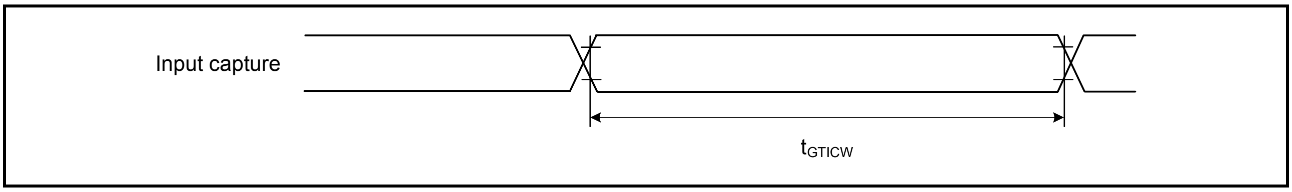


Figure 2.28 GPT32 input capture timing

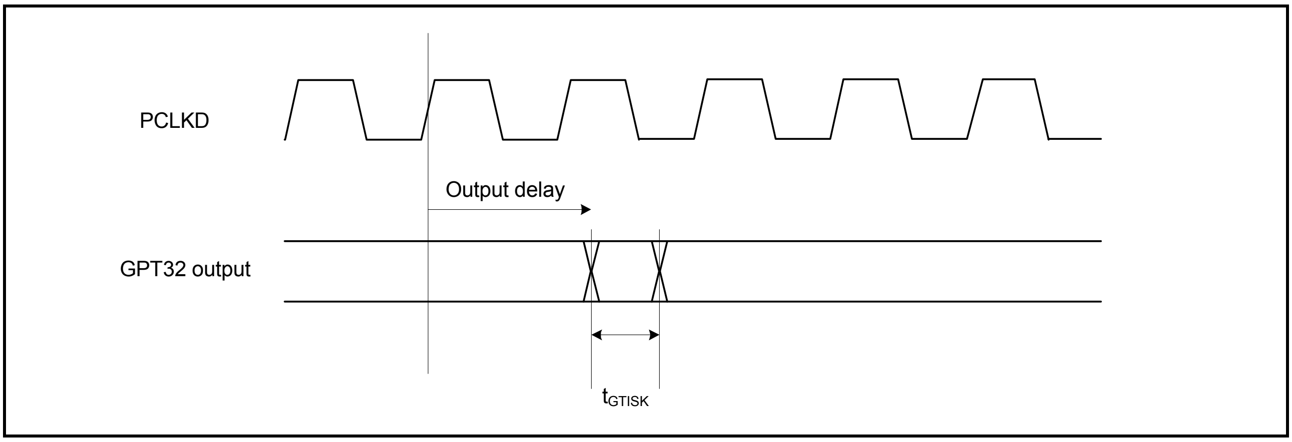


Figure 2.29 GPT32 output delay skew

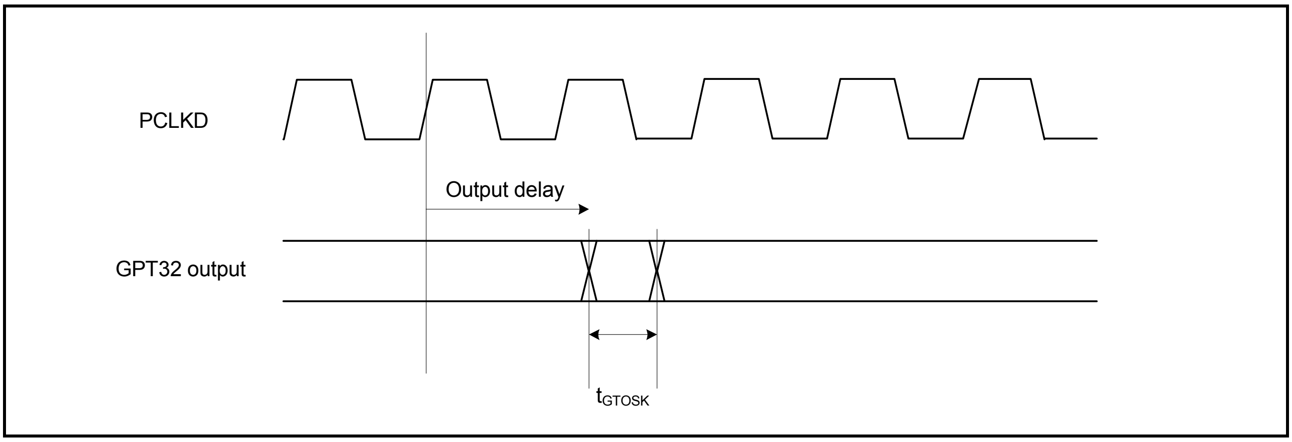


Figure 2.30 GPT32 output delay skew for OPS

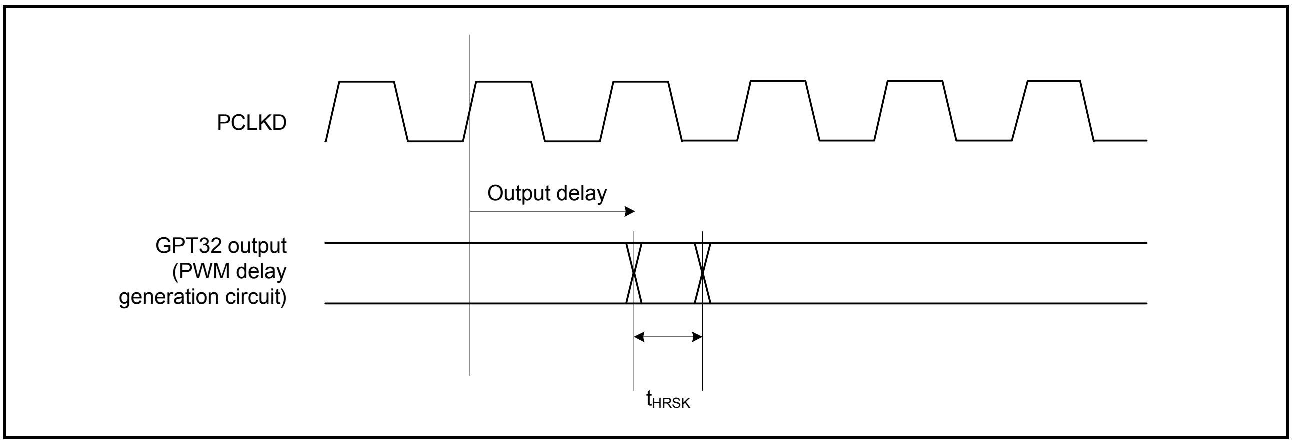


Figure 2.31 GPT32 (PWM Delay Generation Circuit) output delay skew

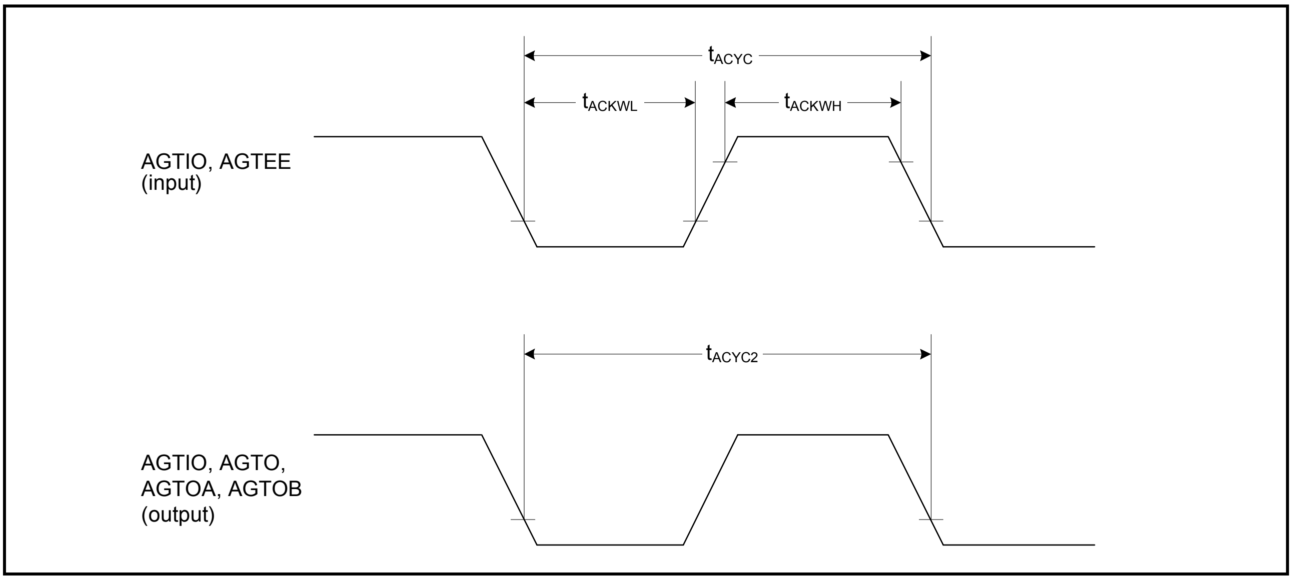


Figure 2.32 AGT input/output timing

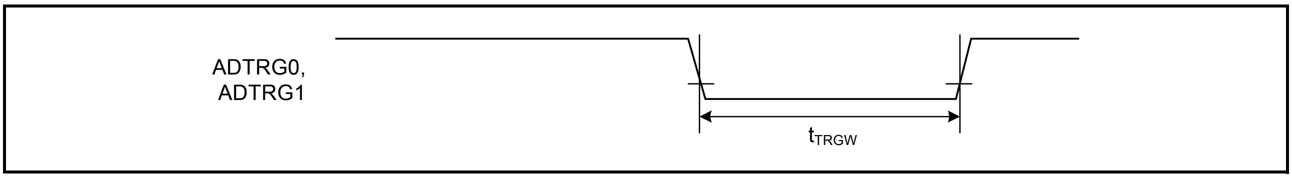


Figure 2.33 ADC12 trigger input timing

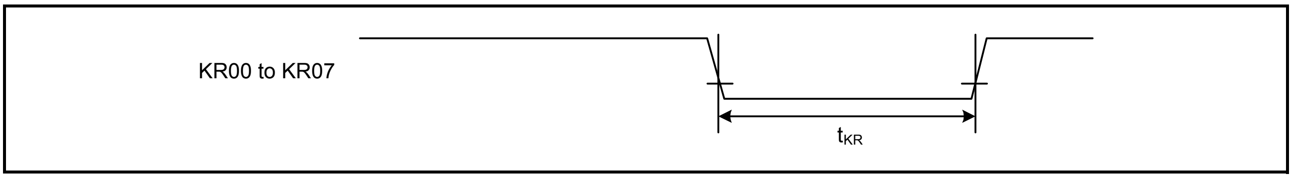


Figure 2.34 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

Item			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq tcac^{*2}$	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac^{*2}$		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9 (except for SCK4_B, SCK7_A), SCK4_B, SCK7_A.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.35
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 2.36
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

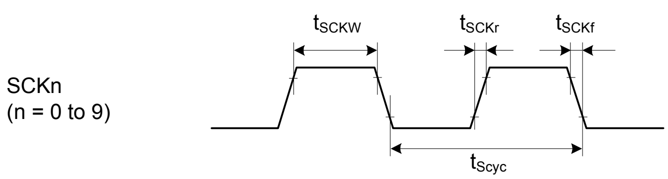


Figure 2.35 SCK clock input/output timing

Table 2.27 IIC timing (1) (2/2)

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

Item		Symbol	Min*1, *2	Max	Unit	Test conditions
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.

Table 2.28 IIC timing (2)

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3(6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

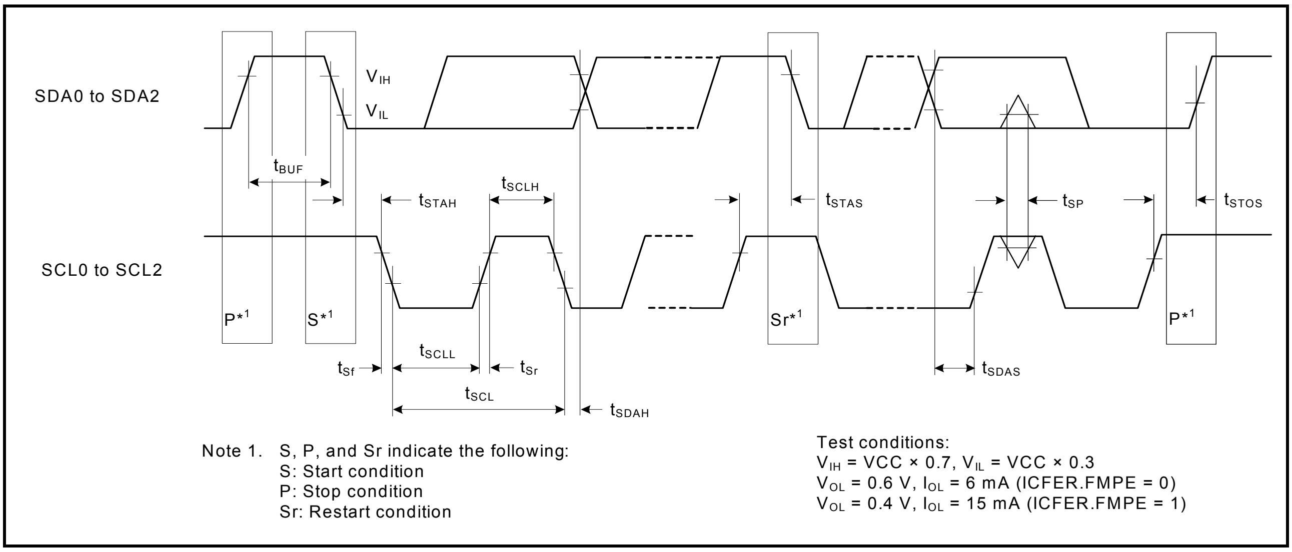


Figure 2.52 I^2C bus interface input/output timing

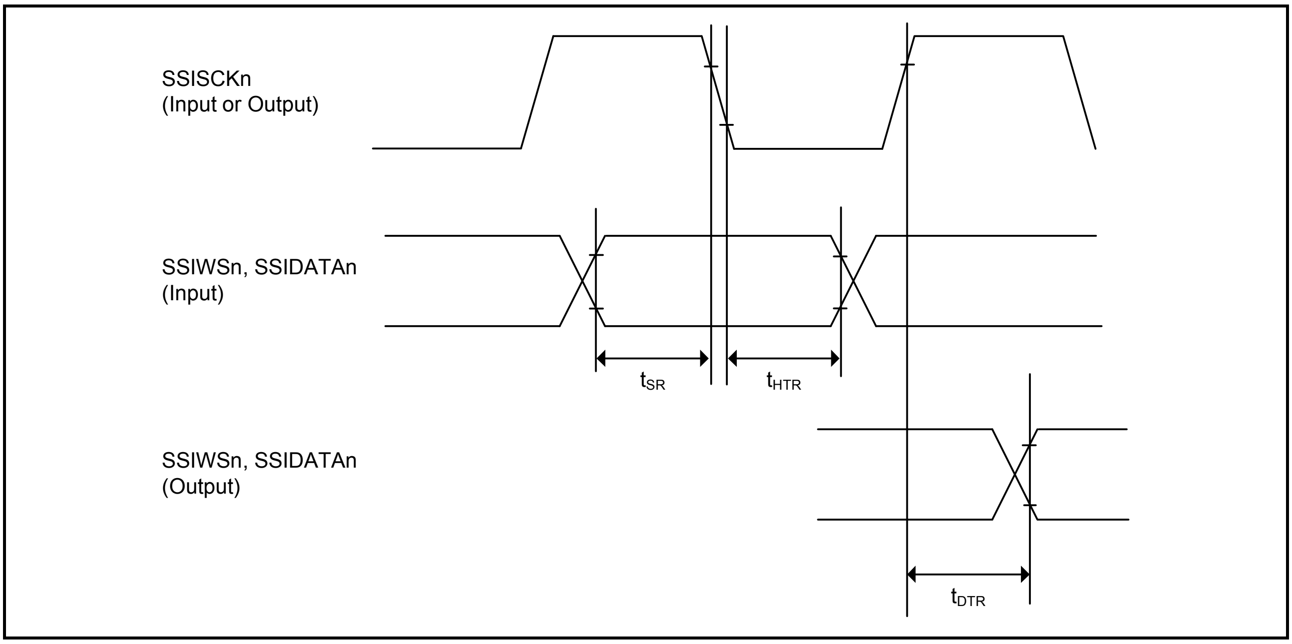


Figure 2.55 SSI data transmit and receive timing when SSICR.SCKP = 1

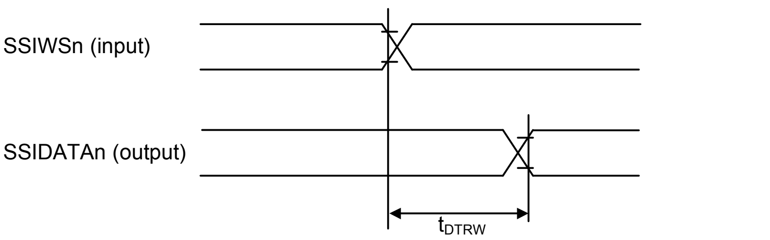


Figure 2.56 SSI data output delay after SSIWSn change

2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Item	Symbol	Min	Max	Unit	Test conditions
SDCLK clock cycle	T_{SDCYC}	20	-	ns	Figure 2.57
SDCLK clock high pulse width	T_{SDWH}	6.5	-	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	-	ns	
SDCLK clock rise time	T_{SDLH}	-	3	ns	
SDCLK clock fall time	T_{SDHL}	-	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	–6	5	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4	-	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	2	-	ns	

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.83
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

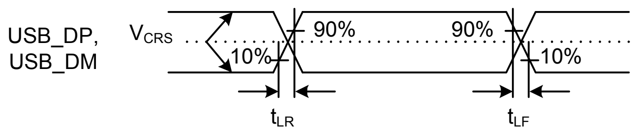


Figure 2.83 USB_DP and USB_DM output timing in low-speed mode

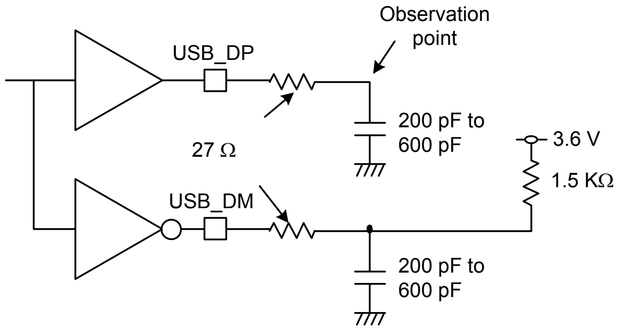


Figure 2.84 Test circuit in low-speed mode

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (1/2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-

2.6 DAC12 Characteristics

Table 2.43 D/A conversion characteristics

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
DNL		±1.0	±2.0	LSB	Resistive load 2 MΩ
Output impedance	-	7.5	-	kΩ	-
Conversion time	-	-	3.0	μs	Capacitive load 20 pF
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	μs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH – 0.2	V	-

2.7 TSN Characteristics

Table 2.44 TSN characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.1	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	μs	-
Sampling time	-	4.15	-	-	μs	-

2.8 OSC Stop Detect Characteristics

Table 2.45 Oscillation stop detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.88

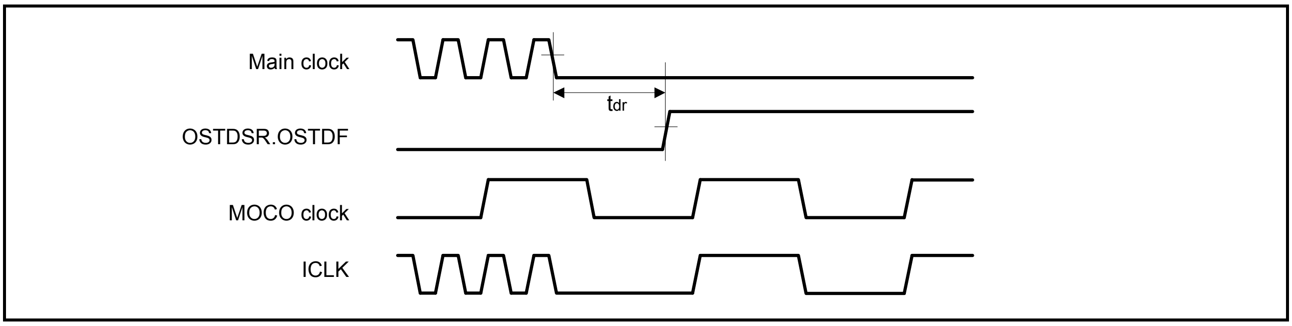


Figure 2.88 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.46 Power-on reset circuit and voltage detection circuit characteristics

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	Module-stop function disabled*1	V_{POR}	2.5	2.6	2.7	V	Figure 2.89
		Module-stop function enabled*2		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.90
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.91
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.92
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	-	4.6	-	ms	Figure 2.89
	LVD0 reset time		t_{LVD0}	-	0.70	-		Figure 2.90
	LVD1 reset time		t_{LVD1}	-	0.57	-		Figure 2.91
	LVD2 reset time		t_{LVD2}	-	0.57	-		Figure 2.92
Minimum VCC down time			t_{VOFF}	200	-	-	μs	Figure 2.89, Figure 2.90
Response delay			t_{det}	-	-	200	μs	Figure 2.89 to Figure 2.92
LVD operation stabilization time (after LVD is enabled)			$T_{d(E-A)}$	-	-	10	μs	Figure 2.91, Figure 2.92
Hysteresis width (LVD1 and LVD2)			V_{LVH}	-	80	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.

Note 2. The low-power function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 3. The low-power function is enabled and DEEPCUT[1:0] = 11b.

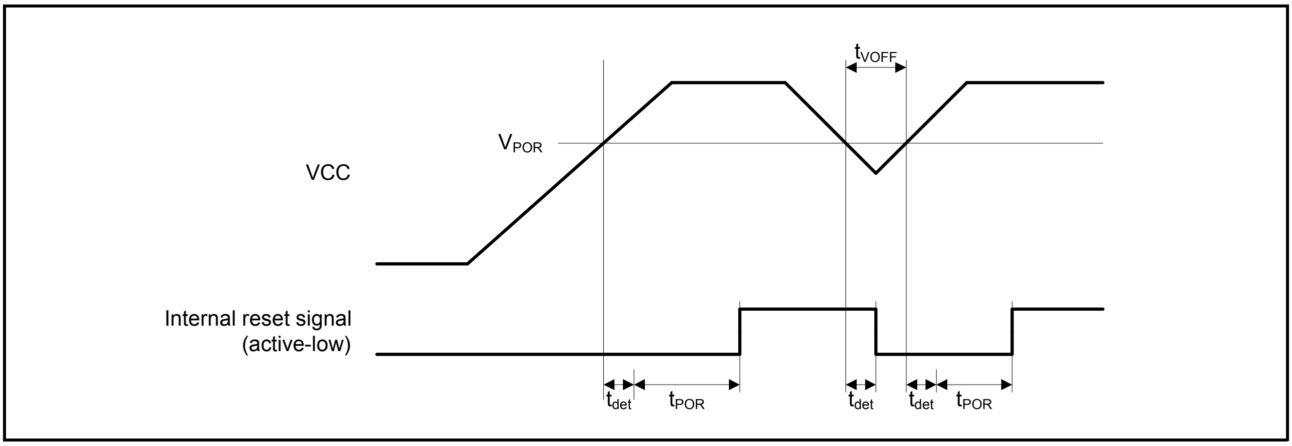


Figure 2.89 Power-on reset timing

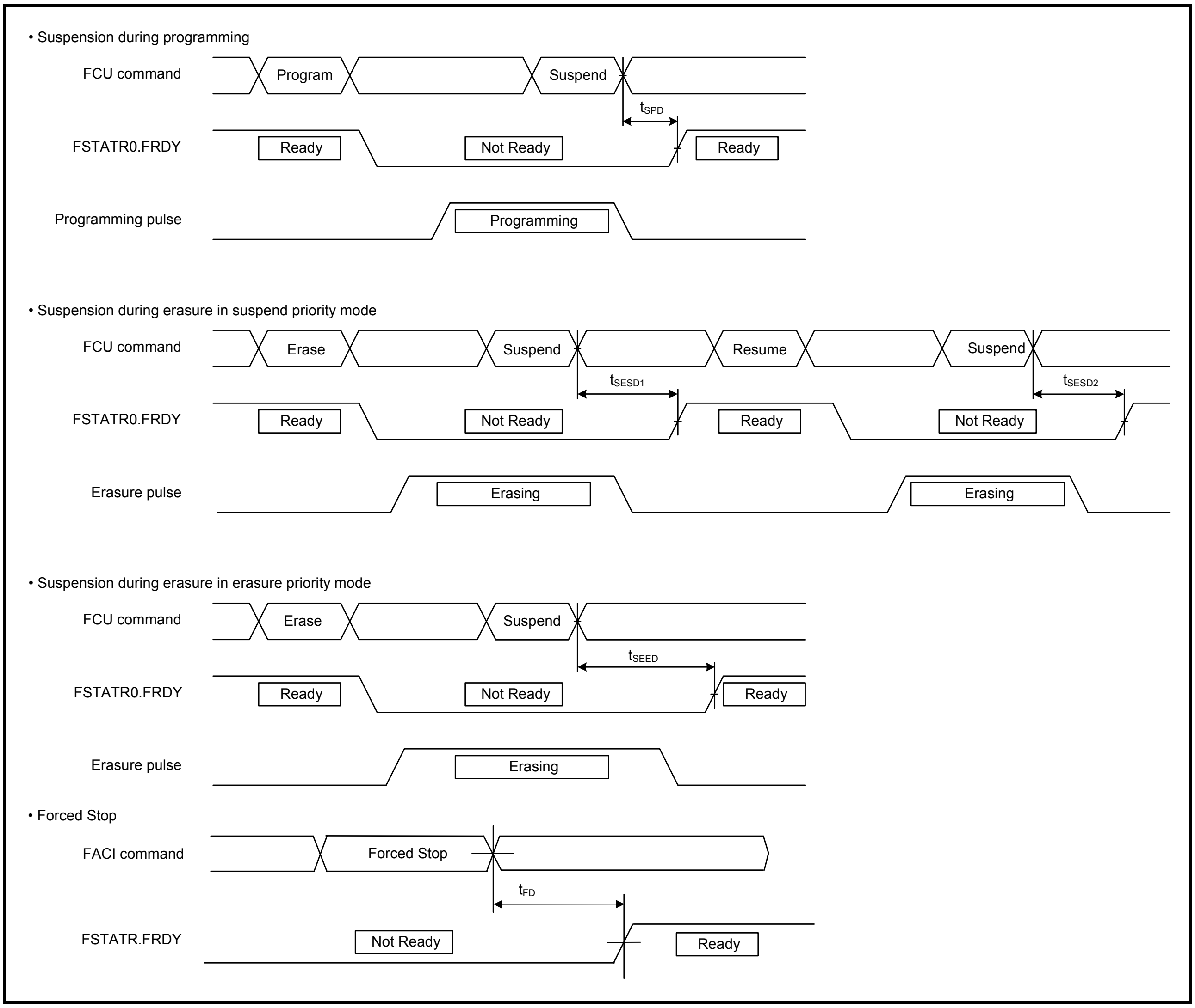


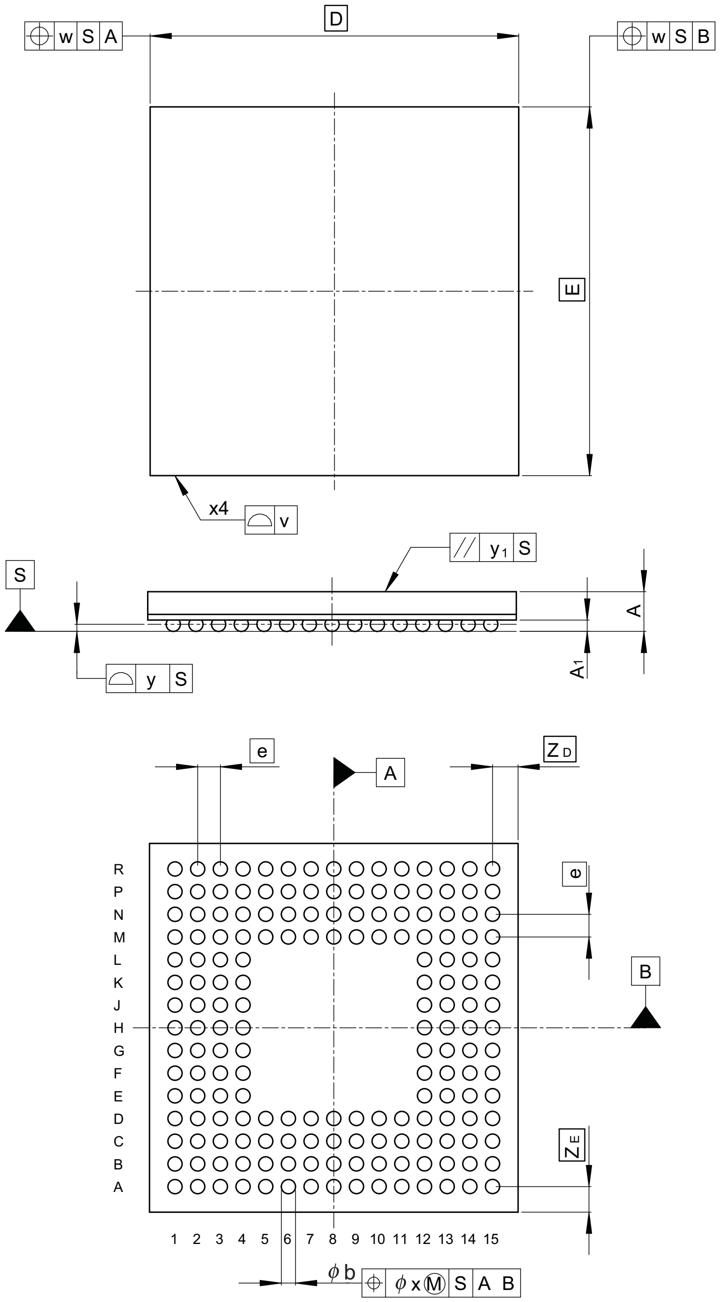
Figure 2.94 Suspension and forced stop timing for flash memory programming and erasure

2.14.2 Data Flash Memory Characteristics

Table 2.53 Data flash memory characteristics (1/2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms
Erasure time	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	μs
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	-	-	125000*2	-	-	-
Suspend delay during programming		t_{DSPD}	-	-	264	-	-	120	μs
First suspend delay during erasure in suspend priority mode		t_{DSESD1}	-	-	216	-	-	120	μs
Second suspend delay during erasure in suspend priority mode		t_{DSESD2}	-	-	300	-	-	300	μs
Suspend delay during erasing in erasure priority mode		t_{DSEED}	-	-	300	-	-	300	μs

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 1.2 176-pin BGA