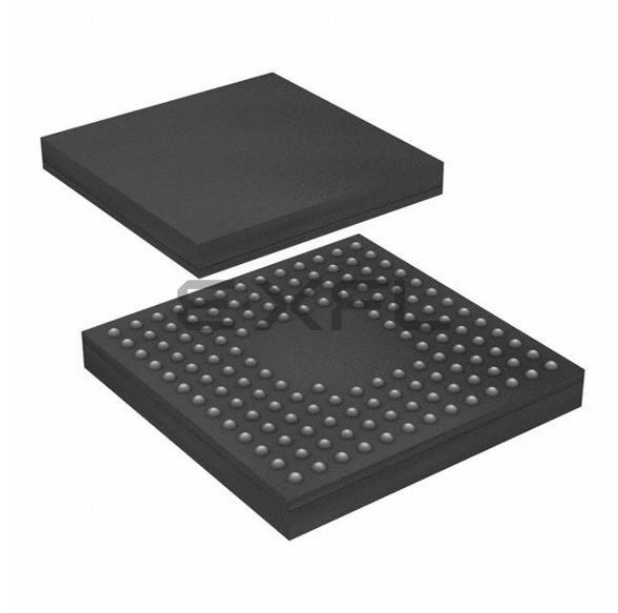
Renesas Electronics America Inc - R7FS7G27G2A01CLK#AC0 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27g2a01clk-ac0

1. Overview

The S7G2 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 240 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 4 MB of code flash memory. See section 54, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 54, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or double-bit error detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 52, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 53, Standby SRAM in User's Manual.

Table 1.3 System (1/2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.4 Interrupt control

Feature	Functional description
Interrupt Controller Unit (ICU)	The ICU controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.

Table 1.5 Event link

Feature	Functional description
Event Link Controller (ELC)	The ELC uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.6 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A DTC module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMAC module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.7 External bus interface

Feature	Functional description
External buses	• CS area (EXBIU): Connected to the external devices (external memory interface) • SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.8 Timers

Feature	Functional description
General PWM Timer (GPT)	The GPT is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state.
Asynchronous General-Purpose Timer (AGT)	The AGT is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The RTC has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

Table 1.9 Communication interfaces (1/2)

Feature	Functional description
Serial Communications Interface (SCI)	The SCI is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual.
I^2C Bus Interface (IIC)	The three-channel IIC conforms with and provides a subset of the NXP I^2C bus (Inter-Integrated Circuit bus) interface functions. See section 36, I^2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface (SSI)	The SSI peripheral provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSI supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface (SSI) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Controller Area Network (CAN) Module	The CAN module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed Module (USBFS)	Full-Speed USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual.
USB 2.0 High-Speed Module (USBHS)	High-Speed USB controller that can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual.

Table 1.9 Communication interfaces (2/2)

Feature	Functional description
Ethernet MAC with IEEE 1588 PTP (ETHERC)	Two-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. Each ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: • Synchronization Frame Processing units (SYNFP0 and SYNFP1) • A Packet Relation Controller unit (PRC-TC) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface provide the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-, 4-, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.10 Analog

Feature	Functional description
12-Bit A/D Converter (ADC12)	Up to two successive approximation 12-Bit A/D Converters are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 12 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 46, 12-Bit A/D Converter (ADC12) in User's Manual.
12-Bit D/A Converter (DAC12)	The DAC12 D/A converts data and includes an output amplifier. See section 47, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature sensor (TSN)	The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 48, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	Analog comparators can be used to compare a test voltage with a reference voltage and to provide a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 49, High-Speed Analog Comparator (ACMPHS) in User's Manual.

Table 1.11 Human machine interfaces (1/2)

Feature	Functional description
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.

1.3 Part Numbering

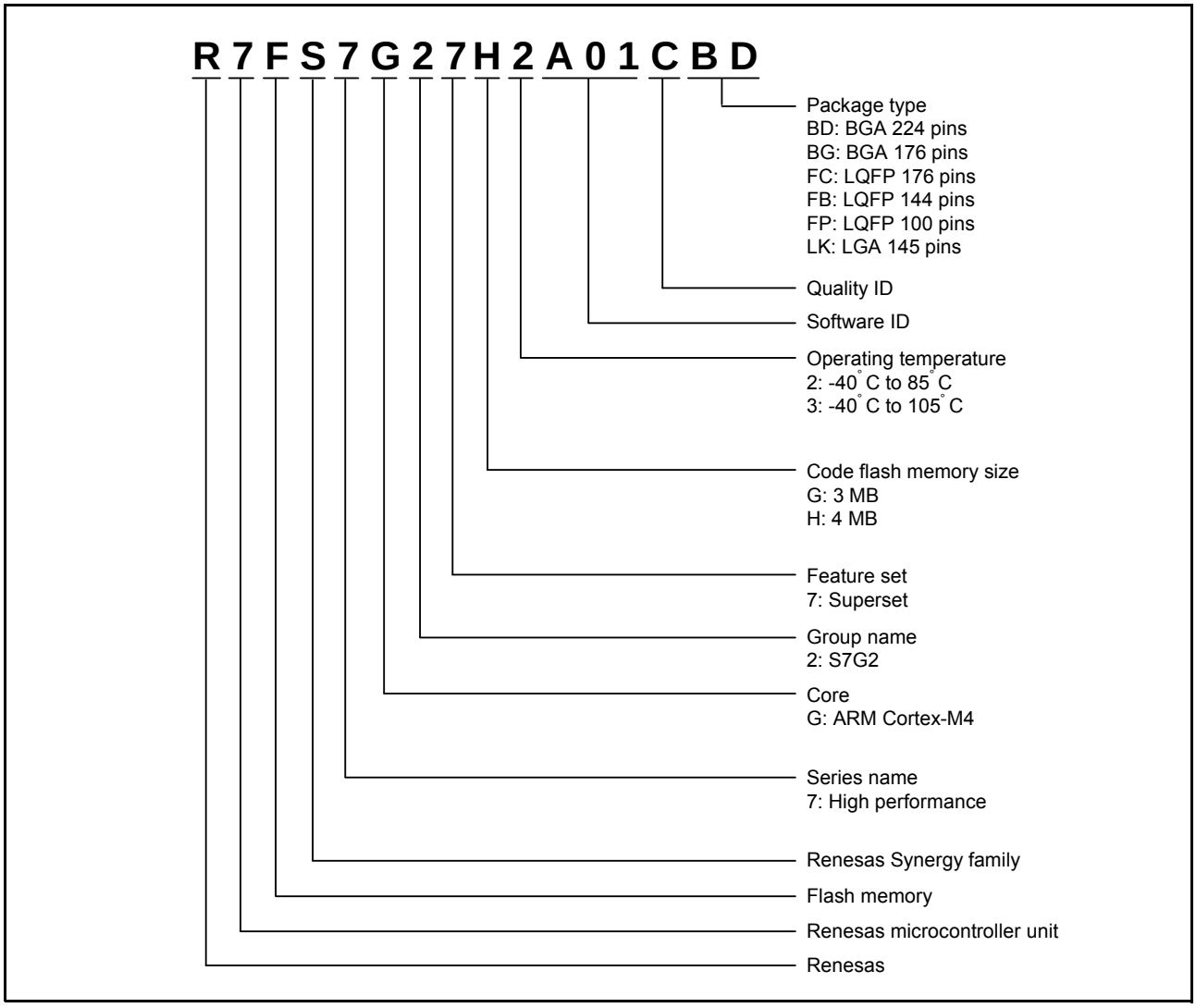


Figure 1.2 Part numbering scheme

R7FS7G2xxxA01CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	VCL1	VSS	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	VLO	VLO	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	VCC_ DCDC	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	VCL2	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL_F	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.6 Pin assignment for 145-pin LGA (top view)

Table 1.17 Pin list (12/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
N10	-	-	-	-	-	-	P011	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN104	-	-	IRQ15-DS	-
M10	M8	159	-	-	-	-	P010	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN103	-	-	IRQ14-DS	-
R10	M9	160	M9	131	-	-	P009	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN004	-	-	IRQ13-DS	-
N11	P10	161	N9	132	92	-	P008	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-	IRQ12-DS	-
L9	M6	162	K7	133	93	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS100	-	-	-	-
P10	N10	163	L9	134	94	-	P006	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-	IRQ11-DS	-
R11	R10	164	K8	135	95	-	P005	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-	IRQ10-DS	-
M11	P11	165	K9	136	96	-	P004	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-	IRQ9-DS	-
L10	M5	166	K10	137	97	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVSS000	-	-	-	-
N12	R11	167	M10	138	98	-	P002	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-	IRQ8-DS	-
P11	N11	168	N10	139	99	-	P001	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-	IRQ7-DS	-
R12	R12	169	L10	140	100	-	P000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-	IRQ6-DS	-
L11	M10	170	N11	141	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L12	M11	171	N12	142	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M12	P12	172	-	-	-	-	P806	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXTCLK_B
R13	R13	173	-	-	-	-	P805	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA17_B
P12	-	-	-	-	-	-	P807	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P13	N12	174	-	-	-	-	P513	-	-	-	-	-	-	-	-	-	-	-	-	ET1_ETXD3	-	-	-	-	-	-	-	LCD_DATA16_B
K9	-	-	-	-	-	-	P515	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R14	R14	175	M11	143	-	-	P512	-	-	-	-	GTIOC0A_B	-	CTX1_B	TXD4_B/MOSI4_B/SDA4_B	-	SCL2	-	-	ET1_ETXD2	-	-	-	-	-	-	IRQ14	VSYNC
P14	-	-	-	-	-	-	P514	-	-	-	GTETRGB_C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		-
R15	P13	176	M12	144	-	-	P511	-	-	-	-	GTIOC0B_B	-	CRX1_B	RXD4_B/MISO4_B/SCL4_B	-	SDA2	-	-	ET1_TX_ER	-	-	-	-	-	-	IRQ15	PCKO

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the IIC, SPI, and SSI functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1/2)

Item				Symbol	LDO mode			DCDC mode			Unit	Test conditions
					Min	Typ	Max	Min	Typ	Max		
Supply current*1	High-speed mode	Maximum*2		I_{CC}	-	-	330	-	-	140	mA	ICLK = 240 MHz PCLKA = 120 MHz*6 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*4			-	45	-	-	24	-		
		Normal mode*3	All peripheral clocks enabled, code executing from flash		-	75	-	-	38	-		
			All peripheral clocks disabled, code executing from flash		-	32	-	-	18	-		
		Sleep mode*4			-	25	150	-	15	75		
		Increase during BGO operation	Data flash P/E		-	7	-	-	7	-		
			Code flash P/E		-	10	-	-	10	-		
	Low-speed mode*4				-	4.4	-	-	3	-		ICLK = 1 MHz
	Subosc-speed mode*4				-	3	-	-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	2.4	110	-	1.2	55		-
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	37	255	-	37	255	µA	VBAT ≠ VCC*7
					-	37	285	-	37	285		VBAT = VCC
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		VBAT ≠ VCC*7
					-	25	80	-	25	80		VBAT = VCC
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		VBAT ≠ VCC*7
					-	16	65	-	16	65		VBAT = VCC
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	9	-	-	9	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-	-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	3.0	-	-	3.0	-		-
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		-	0.9	-	-	0.9	-		V_{BATT} = 2.0 V, VCC = 0 V
					-	1.6	-	-	1.6	-		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.7	-	-	1.7	-		V_{BATT} = 2.0 V, VCC = 0 V
					-	3.3	-	-	3.3	-		V_{BATT} = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	-	1	3	mA	-
	ACMPHS (1unit)					100	150		100	150	µA	AVCC ≥ 2.7 V
	Temperature sensor				-	0.1	0.2	-	0.1	0.2	mA	-
	During D/A conversion (per unit)	Without AMP output			-	0.1	0.2	-	0.1	0.2	mA	-
		With AMP output			-	0.5	0.8	-	0.5	0.8	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)				-	2	6	-	2	6	µA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	-	70	120	µA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.4	-	0.07	0.4	µA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.2	-	0.07	0.2	µA	-

equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 00h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 00h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, 86 µs is added as the power supply recovery time.

Note 10. This defines the duration of Normal mode after a transition from Snooze to Normal mode.
The following cases are valid uses of the main clock oscillator:
- The crystal resonator is connected to main clock oscillator
- The external clock is input to main clock oscillator.
The following cases are excluded:
- The main clock resonator is not connected to the system clock source
- Transition is made from Software Standby to Normal mode.

Note 11. The same value as set in MOSCWTCR.MSTS[3:0]. Duration of Normal mode must be longer than the main clock oscillator wait time.
MOSCWTCR: Main Clock Oscillator Wait Control Register
$t_{cycmosc}$: Main clock oscillator frequency cycle.

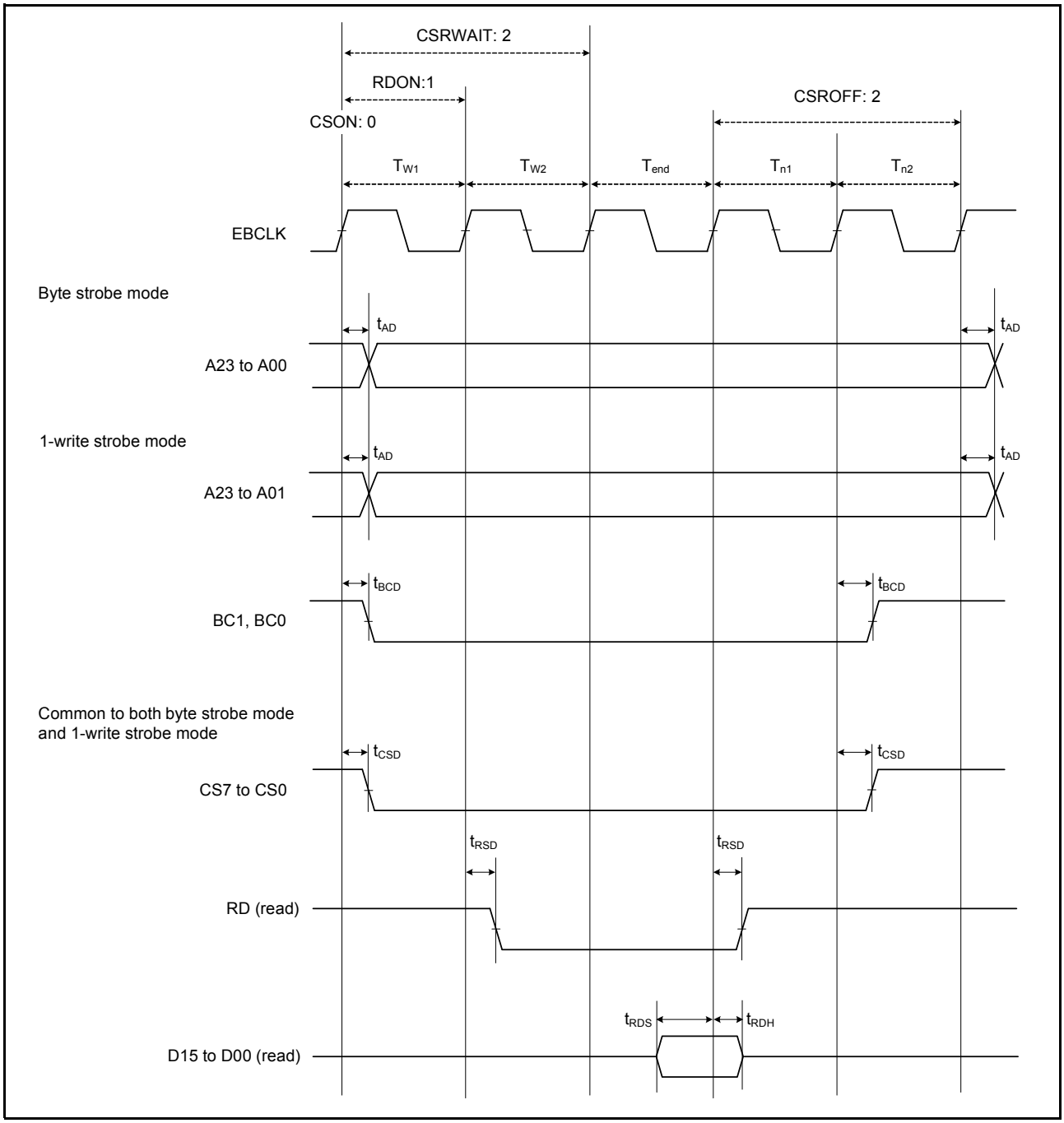


Figure 2.14 External bus timing for normal read cycle with bus clock synchronized

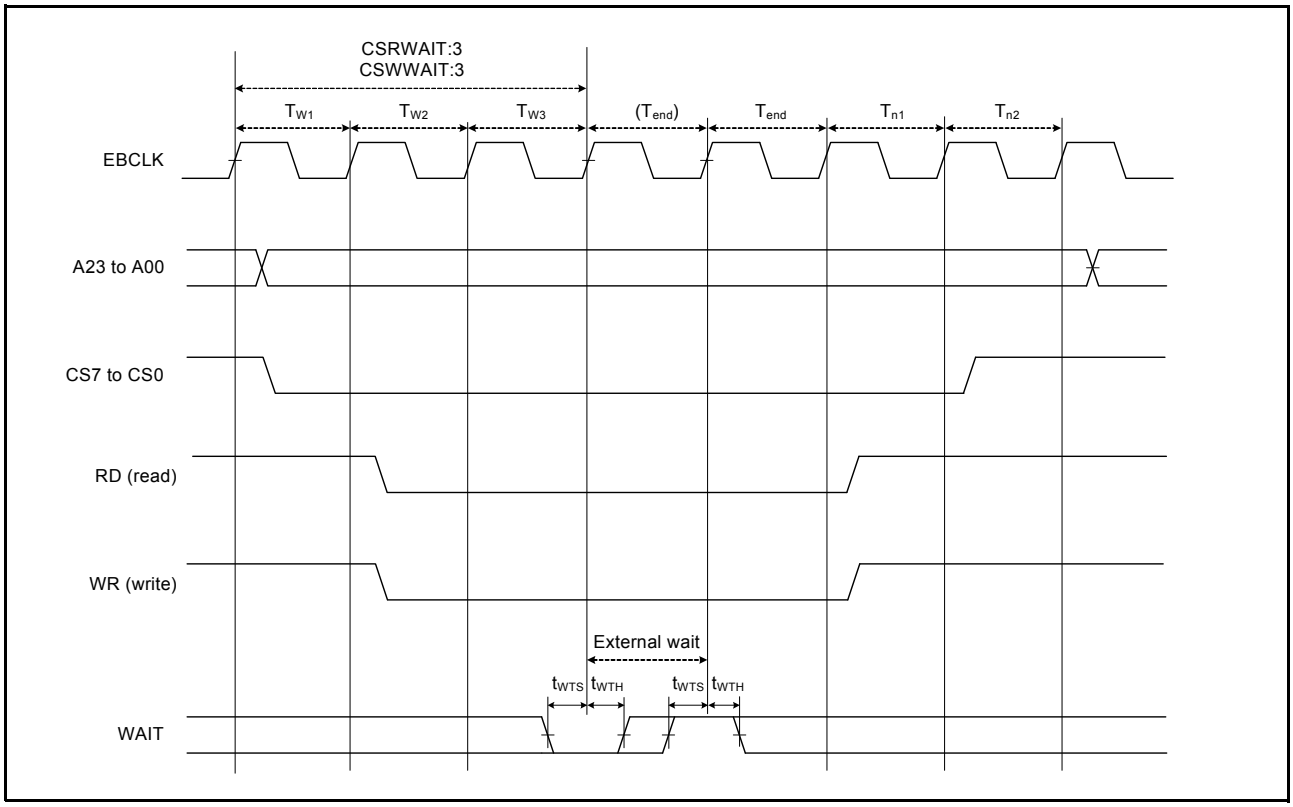


Figure 2.18 External bus timing for external wait control

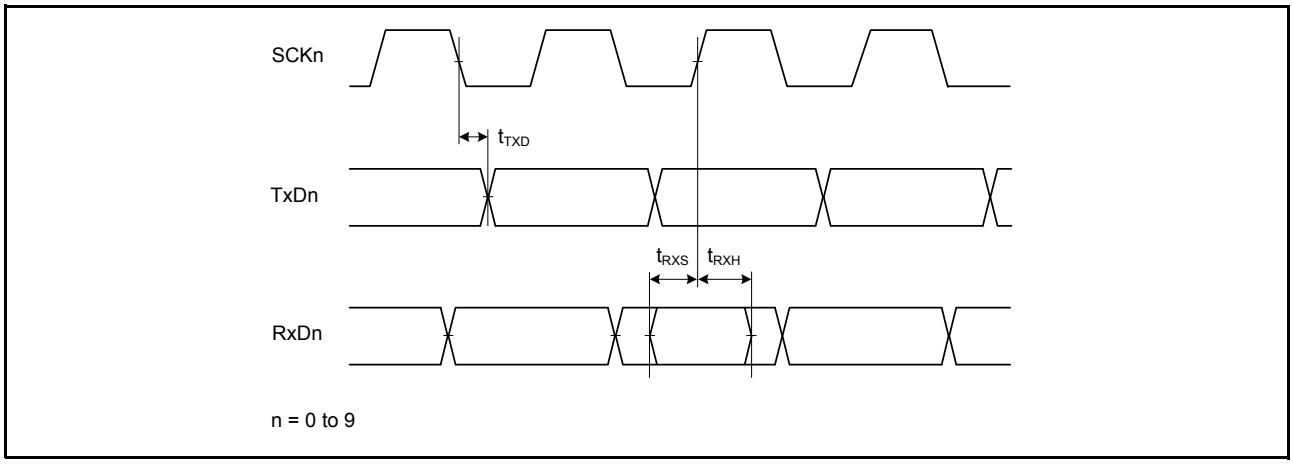


Figure 2.36 SCI input/output timing in clock synchronous mode

Table 2.23 SCI timing (2)

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9 (except for SCK4_B, SCK7_A).
For the SCK4_B and SCK7_A pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.
For the MISO1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 2.37
	SCK clock cycle input (slave)	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	t_{SU}	33.3	-	ns	Figure 2.38 to Figure 2.41
	Data input hold time	t_{H}	33.3	-	ns	
	SS input setup time	t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	t_{OD}	-	33.3	ns	
	Data output hold time	t_{OH}	–10	-	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	-	16.6	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	Slave access time	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 2.41
	Slave output release time	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

Note: MISO1_A is not supported in these specifications.

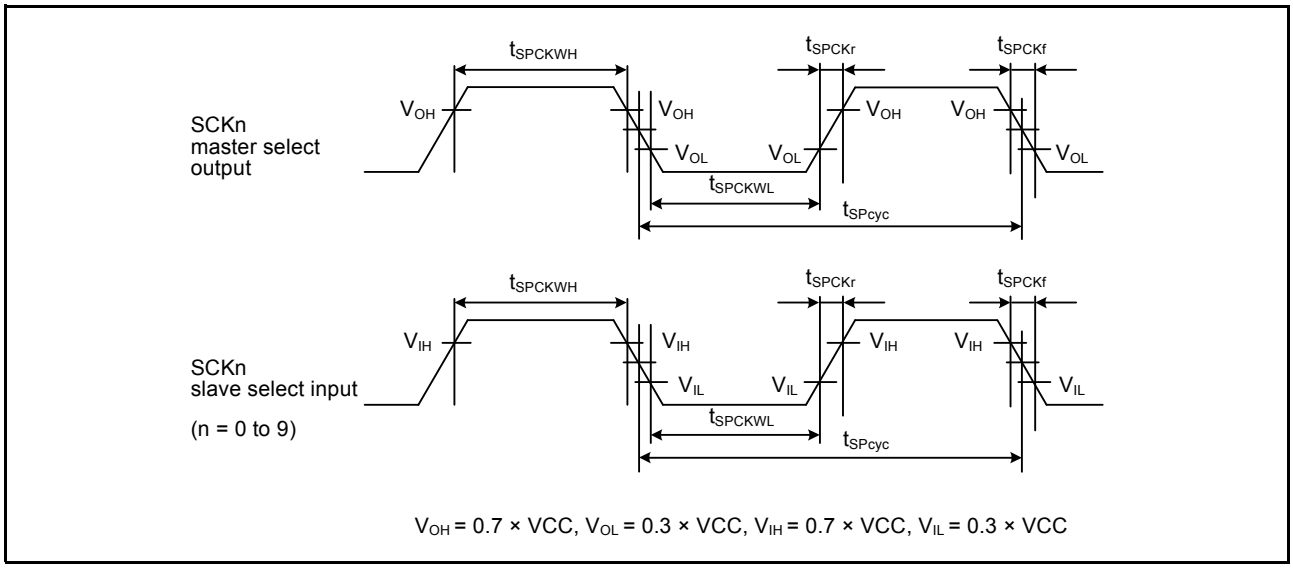


Figure 2.37 SCI simple SPI mode clock timing

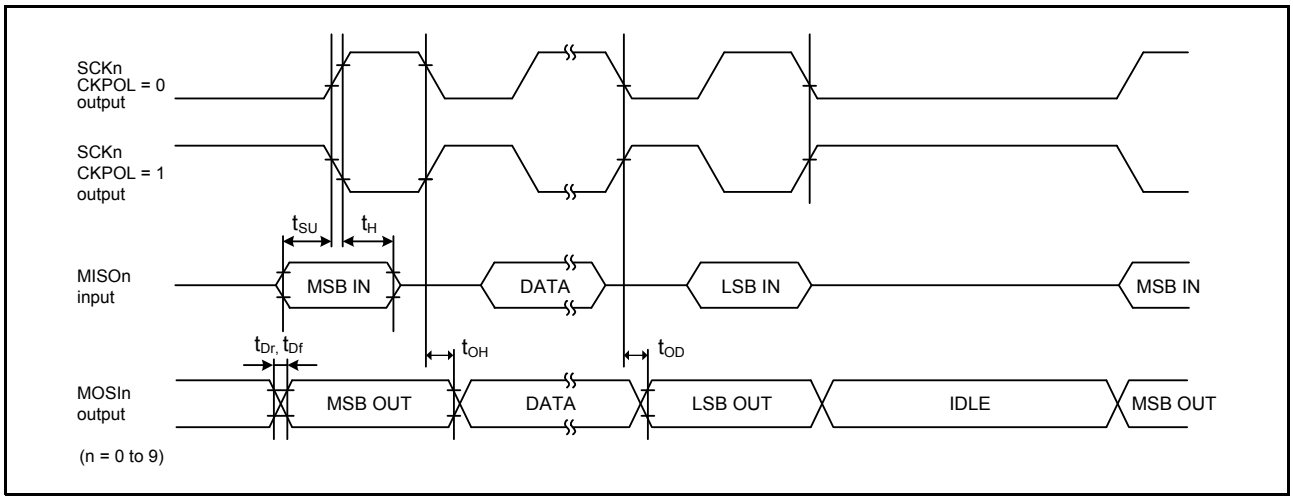


Figure 2.38 SCI simple SPI mode timing for master when CKPH = 1

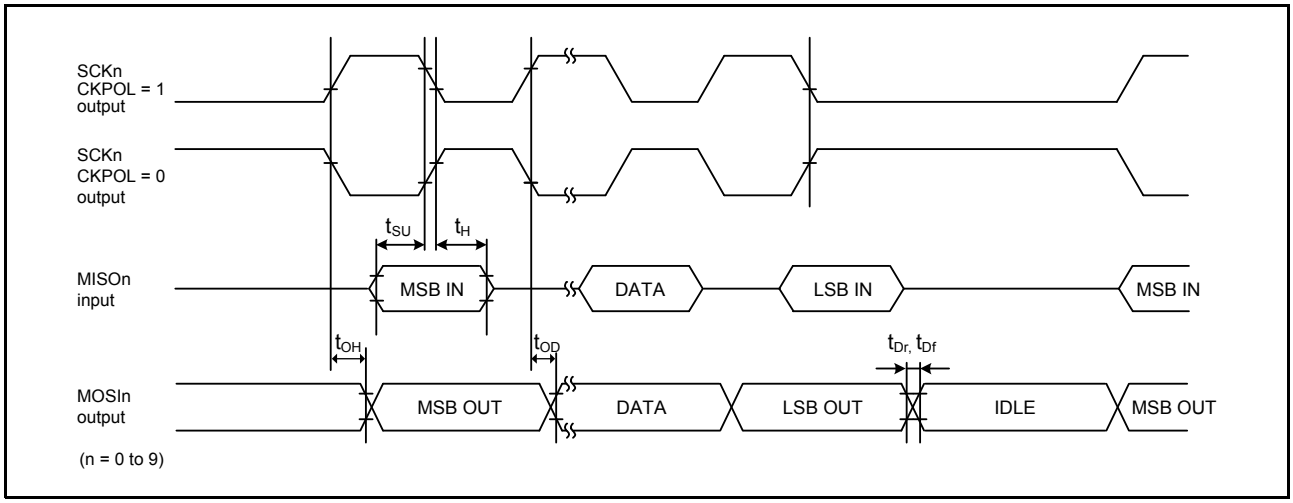


Figure 2.39 SCI simple SPI mode timing for master when CKPH = 0

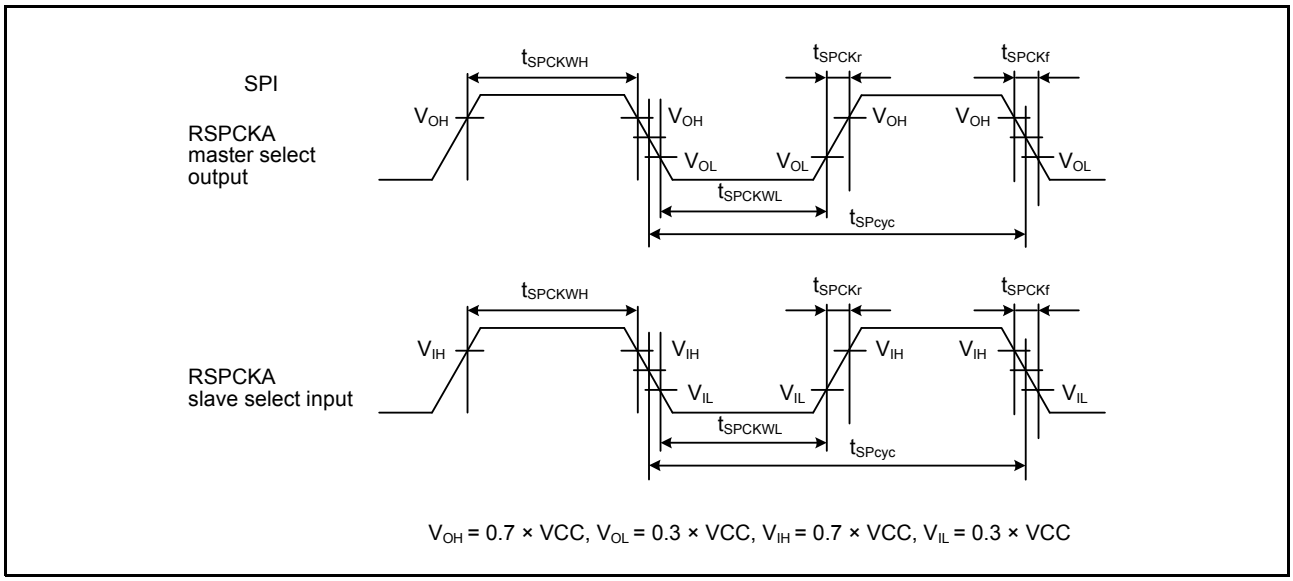


Figure 2.43 SPI clock timing

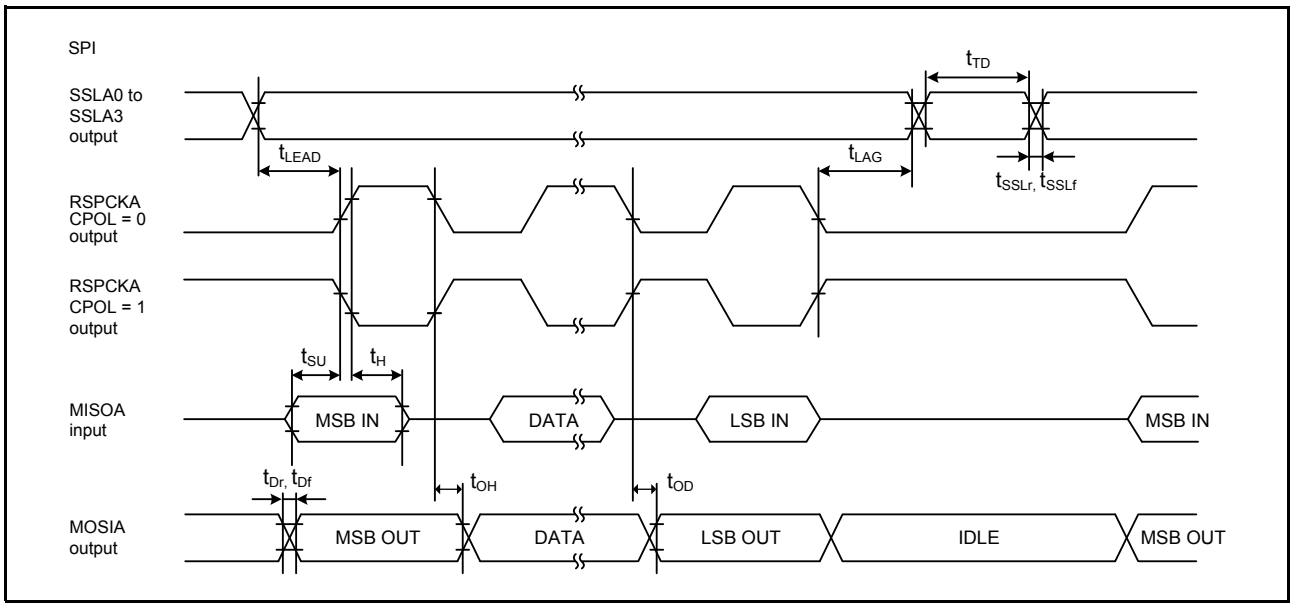


Figure 2.44 SPI timing for master when CPHA = 0

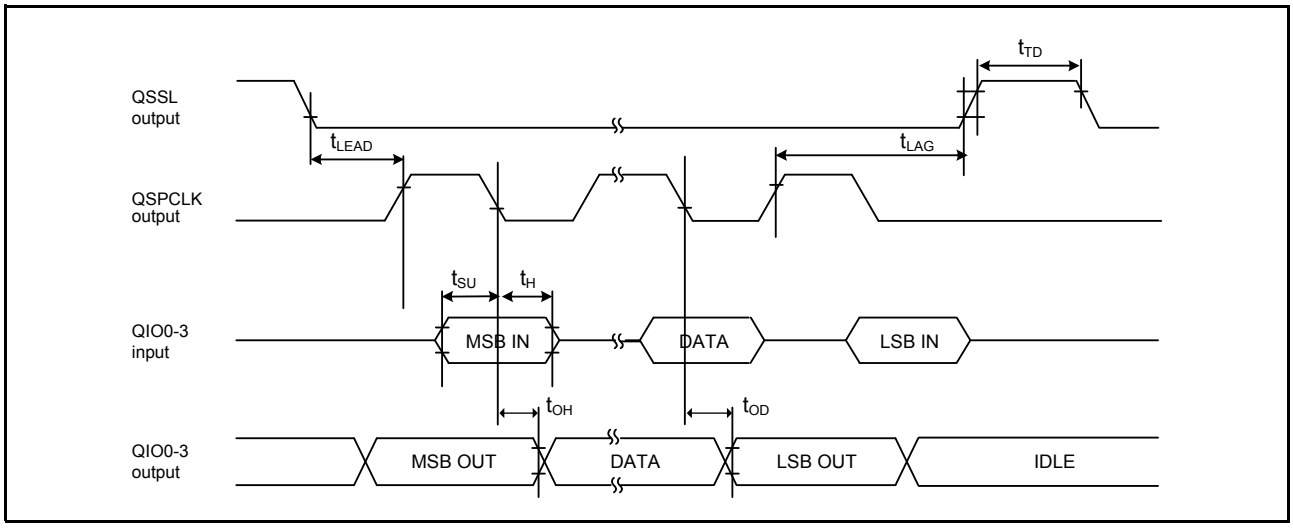


Figure 2.51 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1/2)

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

Item		Symbol	Min*1, *2	Max	Unit	Test conditions
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

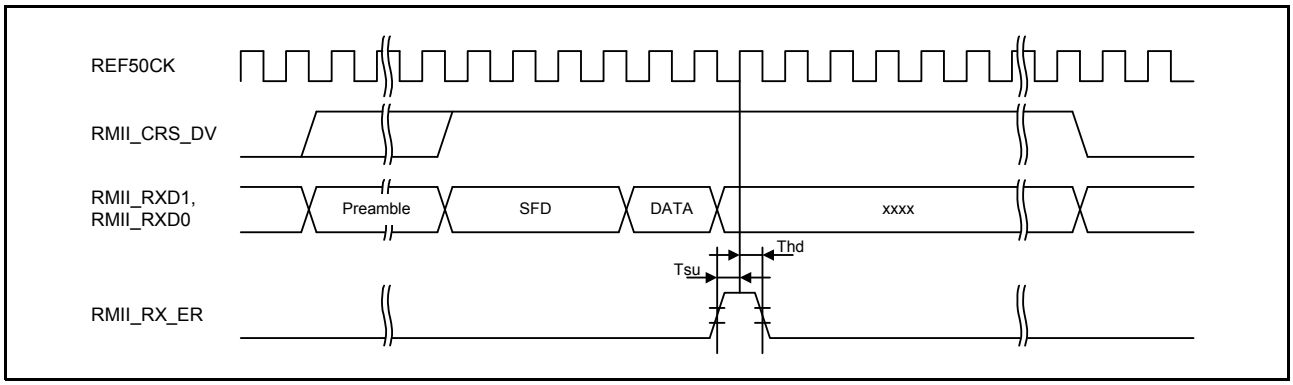


Figure 2.61 RMII reception timing when an error occurs

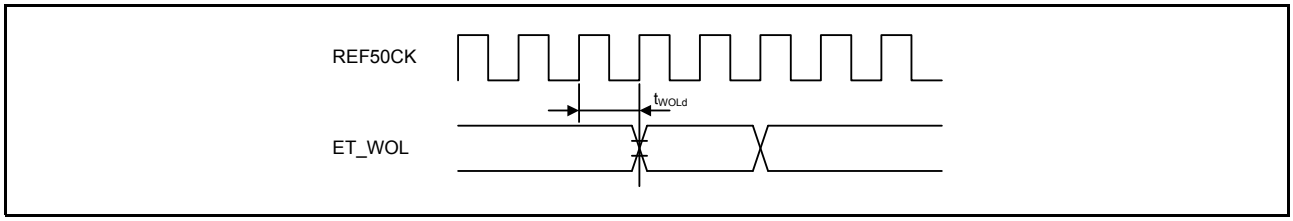


Figure 2.62 WOL output timing for RMII

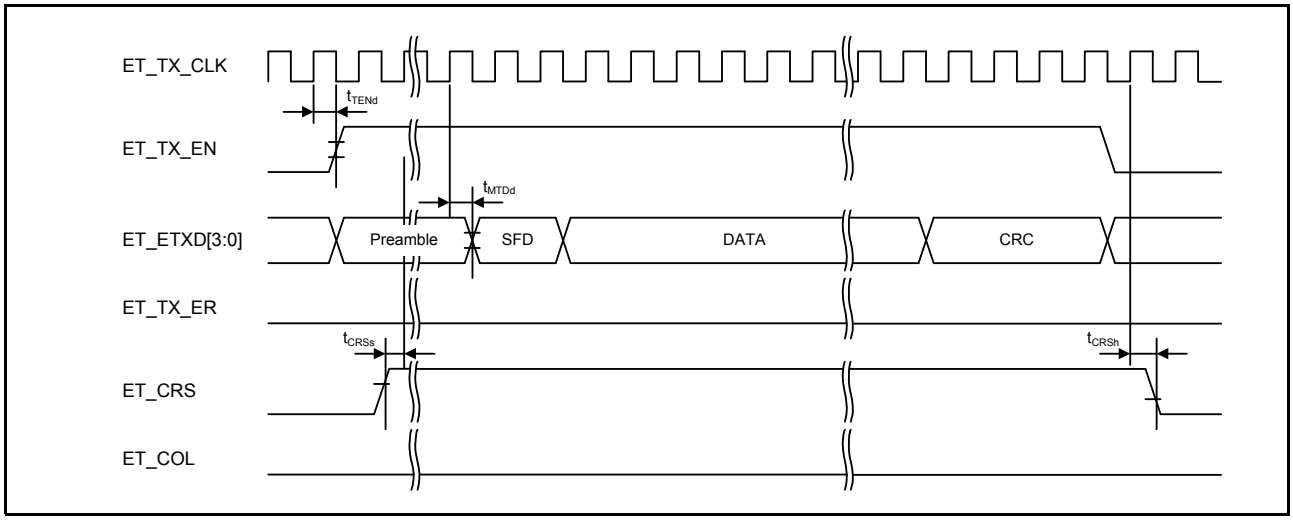


Figure 2.63 MII transmission timing in normal operation

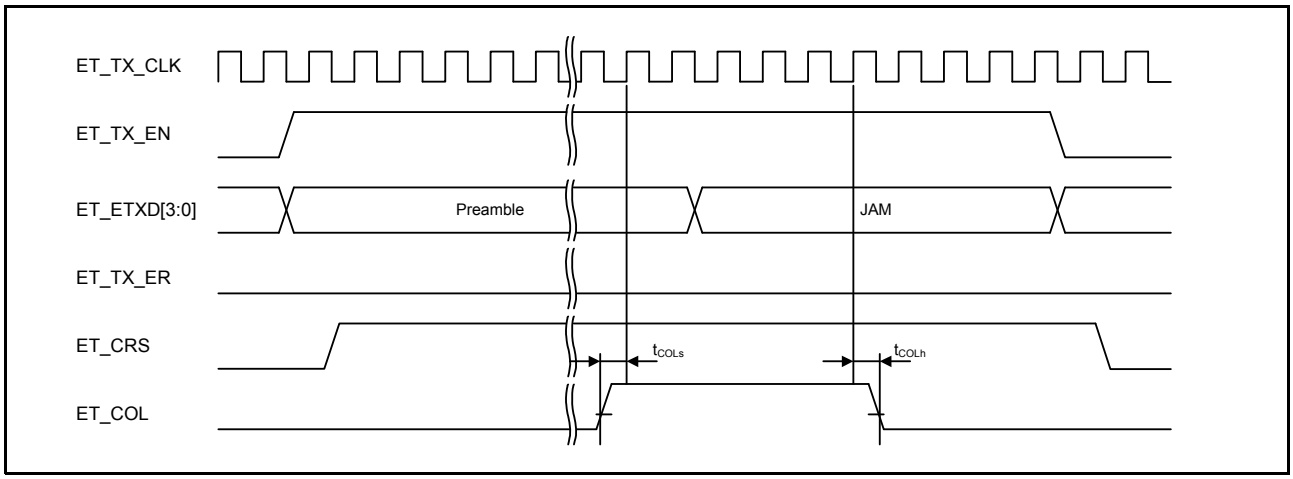


Figure 2.64 MII transmission timing when a conflict occurs

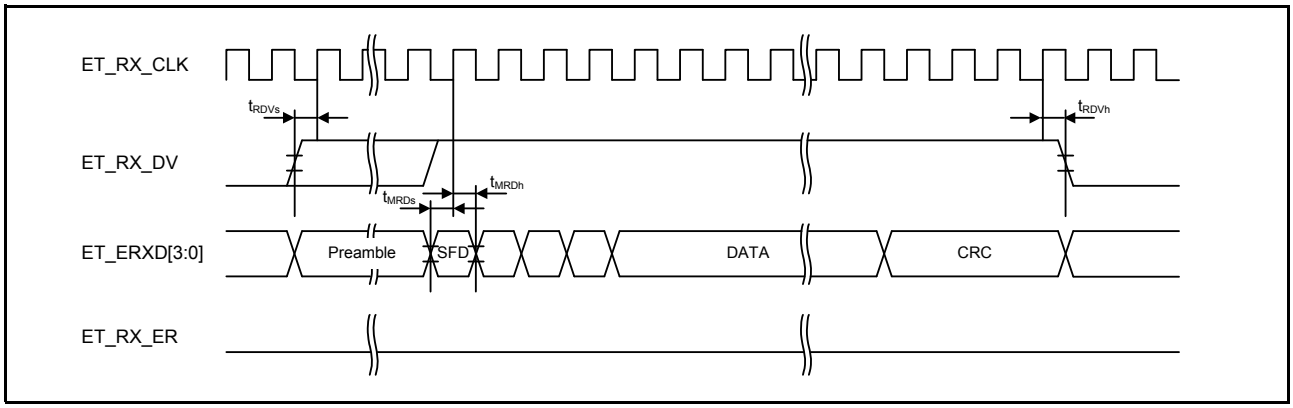


Figure 2.65 MII reception timing in normal operation

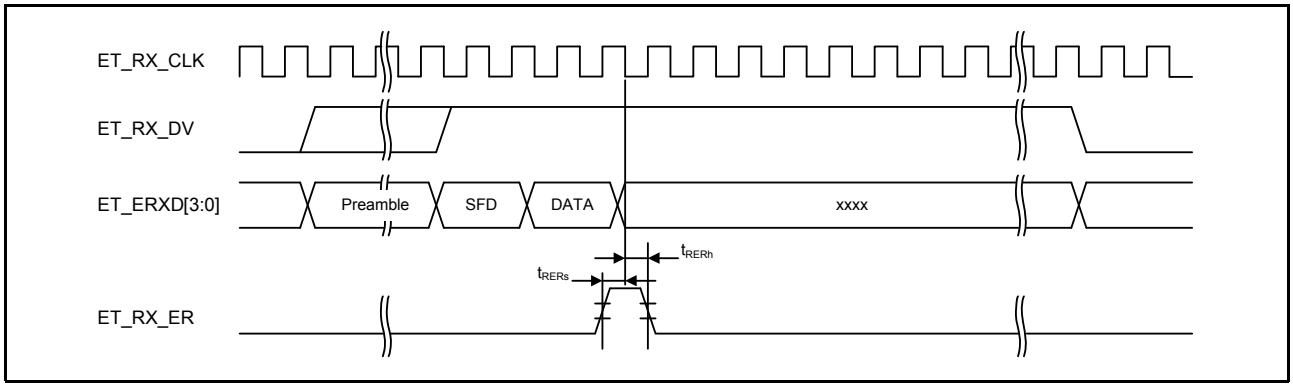


Figure 2.66 MII reception timing when an error occurs

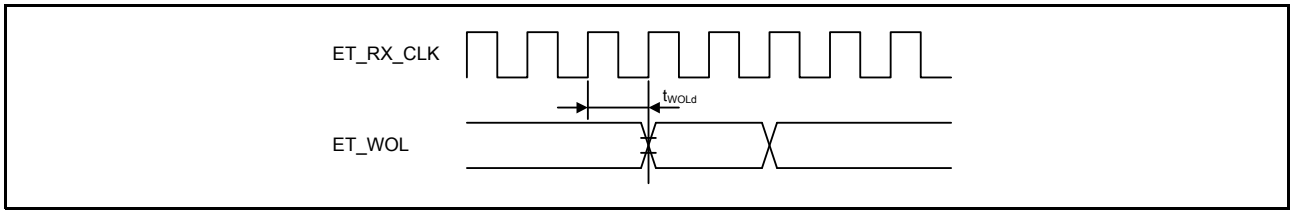


Figure 2.67 WOL output timing for MII

2.6 DAC12 Characteristics

Table 2.43 D/A conversion characteristics

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
DNL		±1.0	±2.0	LSB	Resistive load 2 MΩ
Output impedance	-	7.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Capacitive load 20 pF
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH – 0.2	V	-

2.7 TSN Characteristics

Table 2.44 TSN characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.1	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.45 Oscillation stop detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.88

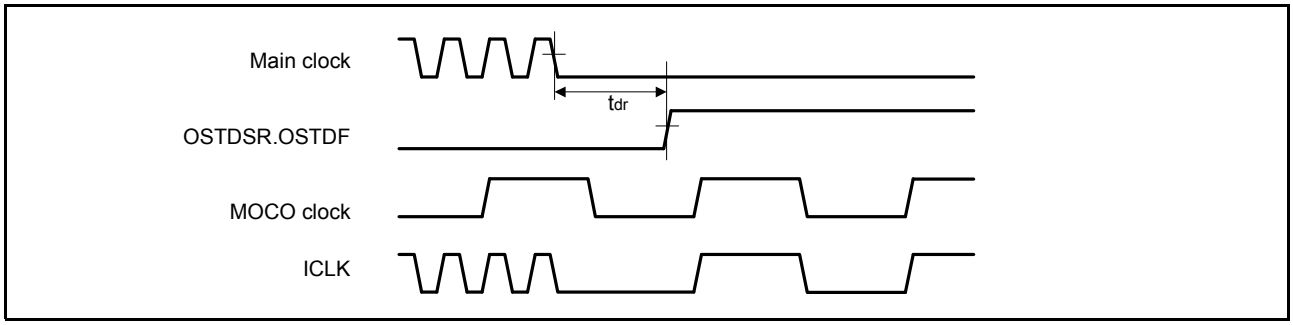


Figure 2.88 Oscillation stop detection timing

Table 2.50 PGA characteristics in single mode (2/2)

Item	Symbol	Min	Typ	Max	Unit
Gain error	Gerr0 (G = 2.000)	–1.0	-	1.0	%
	Gerr1 (G = 2.500)	–1.0	-	1.0	%
	Gerr2 (G = 2.667)	–1.0	-	1.0	%
	Gerr3 (G = 2.857)	–1.0	-	1.0	%
	Gerr4 (G = 3.077)	–1.0	-	1.0	%
	Gerr5 (G = 3.333)	–1.5	-	1.5	%
	Gerr6 (G = 3.636)	–1.5	-	1.5	%
	Gerr7 (G = 4.000)	–1.5	-	1.5	%
	Gerr8 (G = 4.444)	–2.0	-	2.0	%
	Gerr9 (G = 5.000)	–2.0	-	2.0	%
	Gerr10 (G = 5.714)	–2.0	-	2.0	%
	Gerr11 (G = 6.667)	–2.0	-	2.0	%
	Gerr12 (G = 8.000)	–2.0	-	2.0	%
	Gerr13 (G = 10.000)	–2.0	-	2.0	%
	Gerr14 (G = 13.333)	–2.0	-	2.0	%
Offset error	Voff	–8	-	8	mV

Table 2.51 PGA characteristics in differential mode

Item		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	–0.3	-	0.3	V
Differential input voltage range (G = 1.500)		AIN-PGAVSS	–0.5	-	0.5	V
Input voltage range (G = 2.333)			–0.4	-	0.4	V
Input voltage range (G = 4.000)			–0.2	-	0.2	V
Input voltage range (G = 5.667)			–0.15	-	0.15	V
Gain error	G = 1.500	Gerr	–2.5	-	2.5	%
	G = 2.333		–2	-	2	
	G = 4.000		–1	-	1	
	G = 5.667		–1	-	1	

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.52 Code flash memory characteristics (1/2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time N_{PEC} ≤ 100 times	256-byte	t_{P256}	-	0.9	13.2	-	0.4	6	ms
	8-KB	t_{P8K}	-	29	176	-	13	80	ms
	32-KB	t_{P32K}	-	116	704	-	52	320	ms
Programming time N_{PEC} > 100 times	256-byte	t_{P256}	-	1.1	15.8	-	0.5	7.2	ms
	8-KB	t_{P8K}	-	35	212	-	16	96	ms
	32-KB	t_{P32K}	-	140	848	-	64	384	ms
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	-	71	216	-	39	120	ms
	32-KB	t_{E32K}	-	254	864	-	141	480	ms

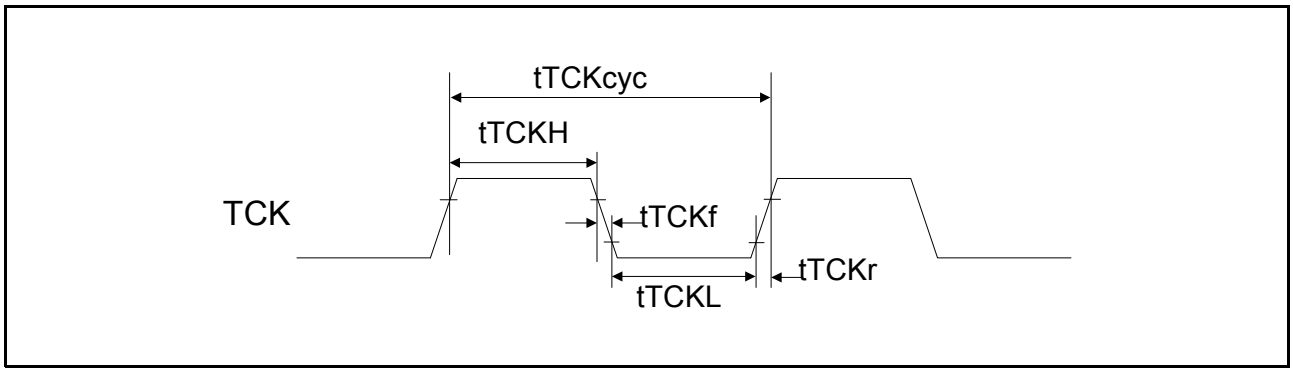


Figure 2.98 JTAG TCK timing

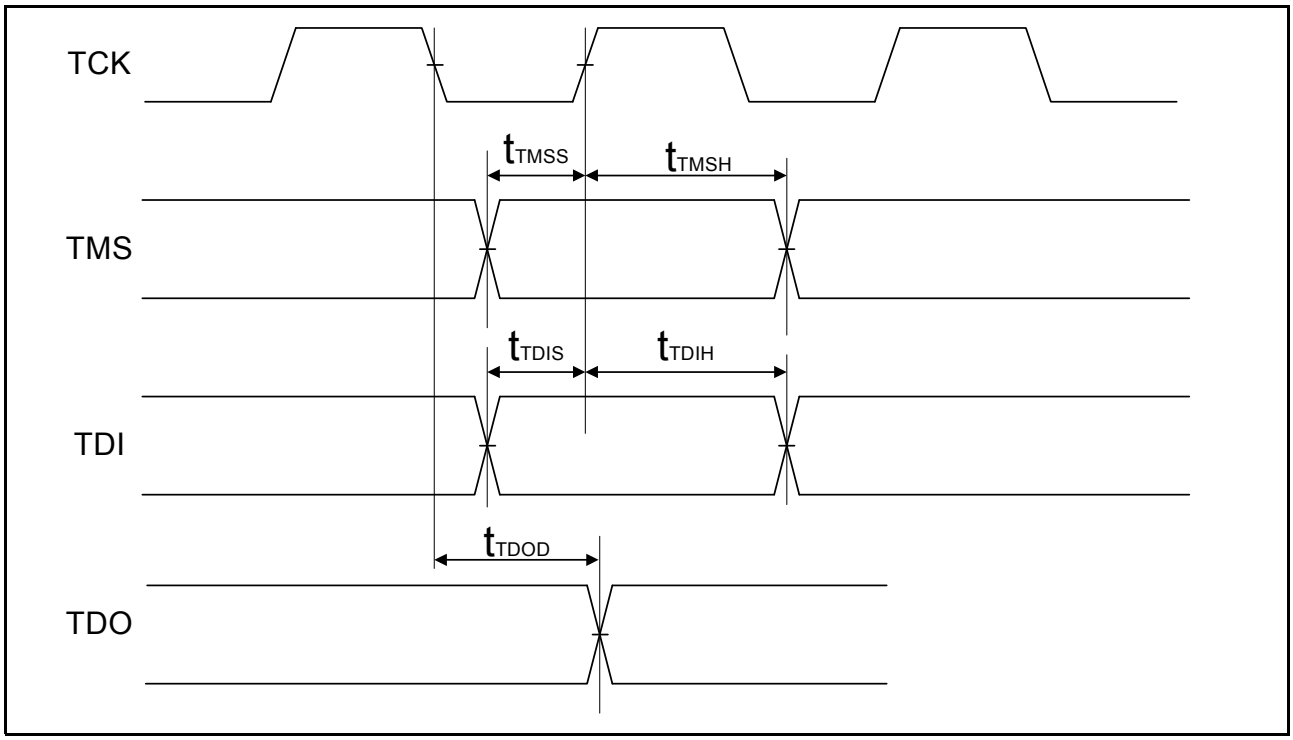


Figure 2.99 JTAG input/output timing

2.17 Serial Wire Debug (SWD)

Table 2.56 SWD

Item	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.100
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.101
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	