Renesas Electronics America Inc - R7FS7G27G3A01CFB#AA0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27g3a01cfb-aa0

1. Overview

The S7G2 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 240 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 4 MB of code flash memory. See section 54, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 54, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or double-bit error detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 52, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 53, Standby SRAM in User's Manual.

Table 1.3 System (1/2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.9 Communication interfaces (1/2)

Feature	Functional description
Serial Communications Interface (SCI)	The SCI is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual.
IrDA Interface (IrDA)	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual.
I^2C Bus Interface (IIC)	The three-channel IIC conforms with and provides a subset of the NXP I^2C bus (Inter-Integrated Circuit bus) interface functions. See section 36, I^2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface (SSI)	The SSI peripheral provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSI supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface (SSI) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual.
Controller Area Network (CAN) Module	The CAN module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed Module (USBFS)	Full-Speed USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual.
USB 2.0 High-Speed Module (USBHS)	High-Speed USB controller that can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual.

Table 1.16 Pin functions (4/5)

Function	Signal	I/O	Description
ETHERC	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timing in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	Indicate carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode.
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode.
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode.
	RMII0_RX_ER, RMII1_RX_ER	Input	Indicate an error occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable signals.
	ET0_RX_DV, ET1_RX_DV	Input	Indicate valid receive data on ET_ERXD3 to ET_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Input	General-purpose external output pins.
	ET0_LINKSTA, ET1_LINKSTA	Output	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	output	4 bits of MII transmit data.
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data.
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable signals. Function as signals indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timing from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timing to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer through ET_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management data with PHY-LSI.
SDHI	SD0CLK, SD1CLK	Output	SD clock output pin.
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pin.
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins.
	SD0CD, SD1CD	Input	SD card detection pin.
	SD0WP, SD1WP	Input	SD write-protect signal.

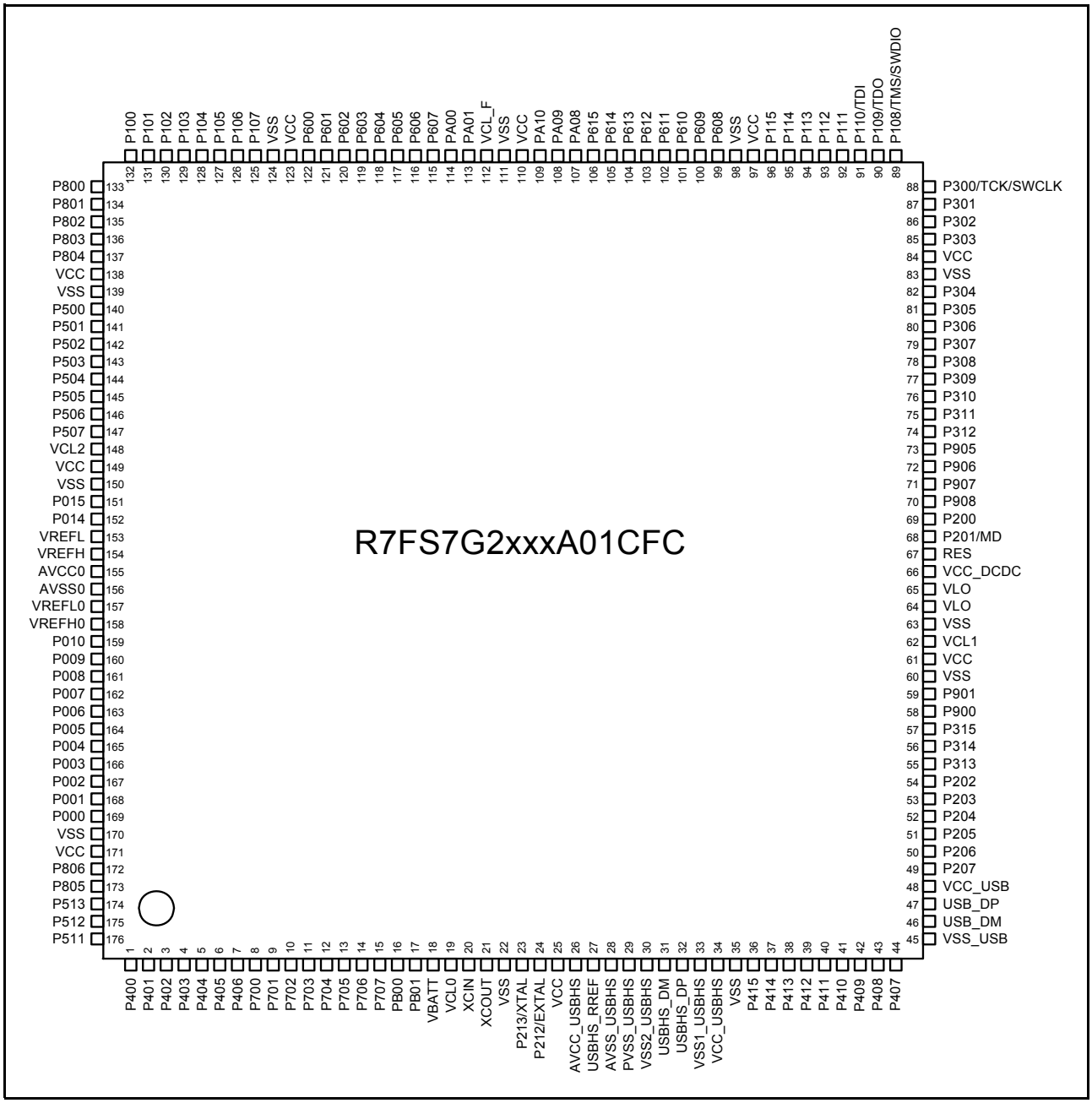


Figure 1.5 Pin assignment for 176-pin LQFP (top view)

R7FS7G2xxxA01CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	VCL1	VSS	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	VLO	VLO	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	VCC_ DCDC	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	VCL2	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL_F	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.6 Pin assignment for 145-pin LGA (top view)

Table 1.17 Pin list (4/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
D14	C15	40	D11	32	21	-	P411	-	-	AGTOA1	GTOVUP_B	GTIOC9A_A	-	-	TXD0_B/MOSI0_B/SDA0_B	CTS3_RTS3_A/SS3_A	-	MOSIA_B	-	ET0_ERXD1	RMII0_RXD0	-	SD0DAT0	-	-	TS07	IRQ4	-
C15	C14	41	C12	33	22	-	P410	-	-	AGTOB1	GTOVLO_B	GTIOC9B_A	-	-	RXD0_B/MISO0_B/SCL0_B	SCK3_A	-	MISOA_B	-	ET0_ERXD0	RMII0_RXD1	-	SD0DAT1	-	-	TS06	IRQ5	-
C14	B15	42	B13	34	23	-	P409	-	-	-	GTOWUP_B	GTIOC10A_A	-	USB_EXICEN_A	-	TXD3_A/MOSI3_A/SDA3_A	-	-	-	ET0_RX_CLK	RMII0_RX_ER	USBHS_EXICEN	-	-	-	TS05	IRQ6	-
B15	D13	43	D10	35	24	-	P408	-	-	-	GTOWLO_B	GTIOC10B_A	-	USB_ID_A	-	RXD3_A/MISO3_A/SCL3_A	-	-	-	ET0_CRS	RMII0_CRS_DV	USBHS_ID	-	-	-	TS04	IRQ7	-
A15	A15	44	A13	36	25	-	P407	-	-	-	-	-	RTCOUT	USB_VBUS	CTS4_RTS4_A/SS4_A	-	SDA0_B	SSLB3_A	-	ET0_EXOUT	ET0_EXOUT	-	-	ADTRG0	-	TS03	-	-
B13	C13	45	B11	37	26	VSS_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	B14	46	A12	38	27		-	-	-	-	-	-	-	USB_DM	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	A14	47	B12	39	28		-	-	-	-	-	-	-	USB_DP	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A13	B13	48	A11	40	29	VCC_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C13	C12	49	C11	41	30	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2_A	-	-	-	-	-	-	-	TS02	-	-
G9	D12	50	B10	42	31	-	P206	WAIT	-	-	GTIU_A	-	-	USB_VBUSEN_A	RXD4_A/MISO4_A/SCL4_A	-	SDA1_A	SSLB1_A	SSIDATA1_A	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT2	-	-	TS01	IRQ0-DS	-
C12	E12	51	A10	43	32	CLKOUT_A	P205	A16	-	AGTO1	GTIV_A	GTIOC4A_B	-	USB_OVRCURA_A-DS	TXD4_A/MOSI4_A/SDA4_A	CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A	SSIWS1_A	ET0_WOL	ET0_WOL	-	SD0DAT3	-	-	TSCAP_A	IRQ1-DS	-
D11	A13	52	C10	44	-	CACREF_A	P204	A18	-	AGTIO1_A	GTIW_A	GTIOC4B_B	-	USB_OVRCURB_A-DS	SCK4_A	SCK9_A	SCL0_B	RSPCKB_A	SSISCK1_A	ET0_RX_DV	-	-	SD0DAT4	-	-	TS00	-	-
B12	D11	53	A9	45	-	-	P203	A19	-	-	-	GTIOC5A_A	-	CTX0_A	CTS2_RTS2_A/SS2_A	TXD9_A/MOSI9_A/SDA9_A	-	MOSIB_A	-	ET0_COL	-	-	SD0DAT5	-	-	TSCAP_B	IRQ2-DS	-

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1/2)

Item				Symbol	LDO mode			DCDC mode			Unit	Test conditions
					Min	Typ	Max	Min	Typ	Max		
Supply current*1	High-speed mode	Maximum*2		I_{CC}	-	-	330	-	-	140	mA	ICLK = 240 MHz PCLKA = 120 MHz*6 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*4			-	45	-	-	24	-		
		Normal mode*3	All peripheral clocks enabled, code executing from flash		-	75	-	-	38	-		
			All peripheral clocks disabled, code executing from flash		-	32	-	-	18	-		
		Sleep mode*4			-	25	150	-	15	75		
		Increase during BGO operation	Data flash P/E		-	7	-	-	7	-		
			Code flash P/E		-	10	-	-	10	-		
	Low-speed mode*4				-	4.4	-	-	3	-		ICLK = 1 MHz
	Subosc-speed mode*4				-	3	-	-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	2.4	110	-	1.2	55		-
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	37	255	-	37	255	µA	VBAT ≠ VCC*7
					-	37	285	-	37	285		VBAT = VCC
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		VBAT ≠ VCC*7
					-	25	80	-	25	80		VBAT = VCC
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		VBAT ≠ VCC*7
					-	16	65	-	16	65		VBAT = VCC
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	9	-	-	9	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-	-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	3.0	-	-	3.0	-		-
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		-	0.9	-	-	0.9	-		V_{BATT} = 2.0 V, VCC = 0 V
					-	1.6	-	-	1.6	-		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.7	-	-	1.7	-		V_{BATT} = 2.0 V, VCC = 0 V
					-	3.3	-	-	3.3	-		V_{BATT} = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	-	1	3	mA	-
	ACMPHS (1unit)					100	150		100	150	µA	AVCC ≥ 2.7 V
	Temperature sensor				-	0.1	0.2	-	0.1	0.2	mA	-
	During D/A conversion (per unit)	Without AMP output			-	0.1	0.2	-	0.1	0.2	mA	-
		With AMP output			-	0.5	0.8	-	0.5	0.8	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)				-	2	6	-	2	6	µA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	-	70	120	µA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.4	-	0.07	0.4	µA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.2	-	0.07	0.2	µA	-

Table 2.13 Clock timing except for sub-clock oscillator (2/2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.61	16	16.39	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.56	18	18.44		
		f_{HOCO20}	19.52	20	20.48		
		f_{HOCO16}	15.52	16	16.48		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.46	18	18.54		
		f_{HOCO20}	19.40	20	20.60		
	With FLL	f_{HOCO16}	15.91	16	16.09		SOSC frequency is 32.768kHz ± 50ppm
		f_{HOCO18}	17.90	18	18.10		
		f_{HOCO20}	19.89	20	20.11		
HOCO clock oscillation stabilization wait time *2		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	3	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 2.7

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*1	s	-

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the value shown is recommended.

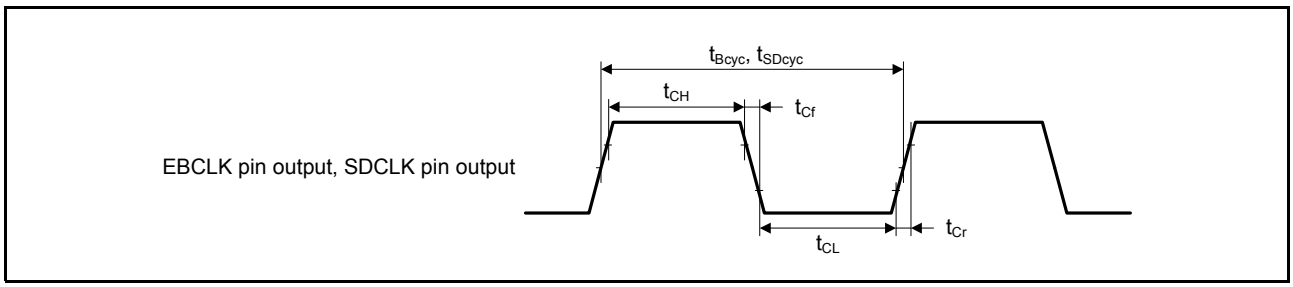


Figure 2.3 EBCLK and SDCLK output timing

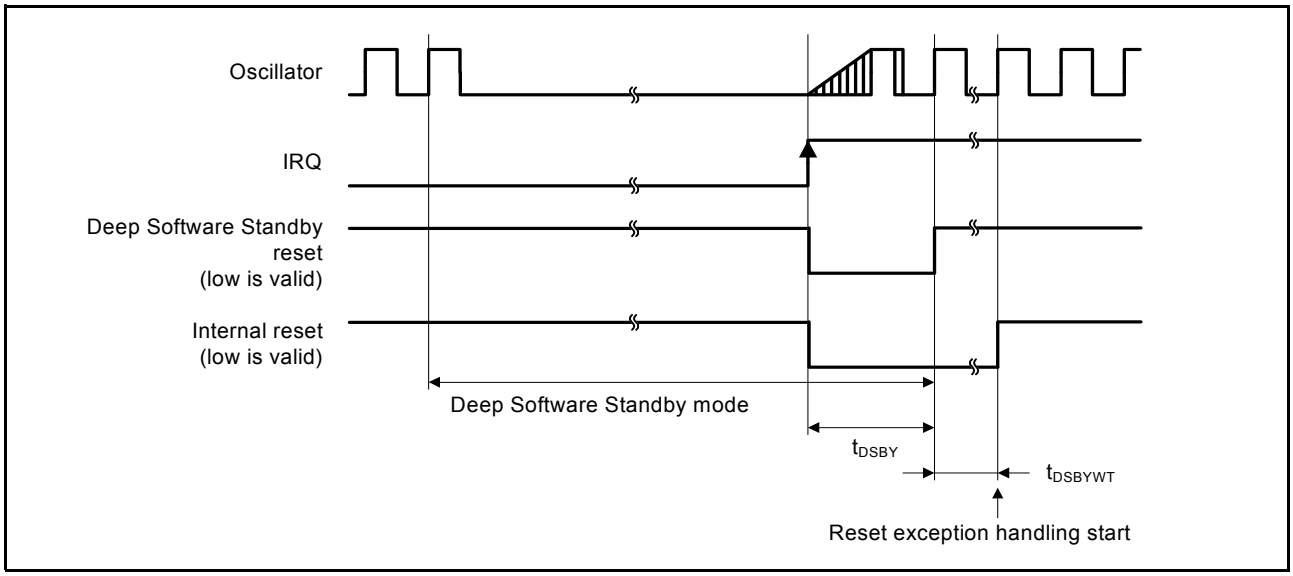


Figure 2.11 Deep Software Standby mode cancellation timing

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

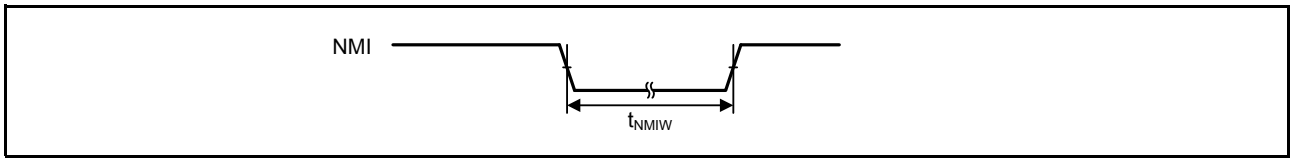


Figure 2.12 NMI interrupt input timing

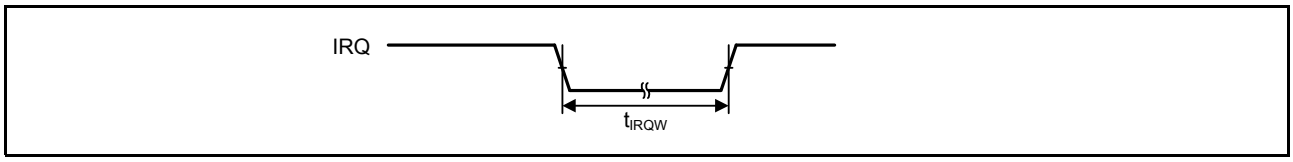


Figure 2.13 IRQ interrupt input timing

2.3.6 Bus Timing

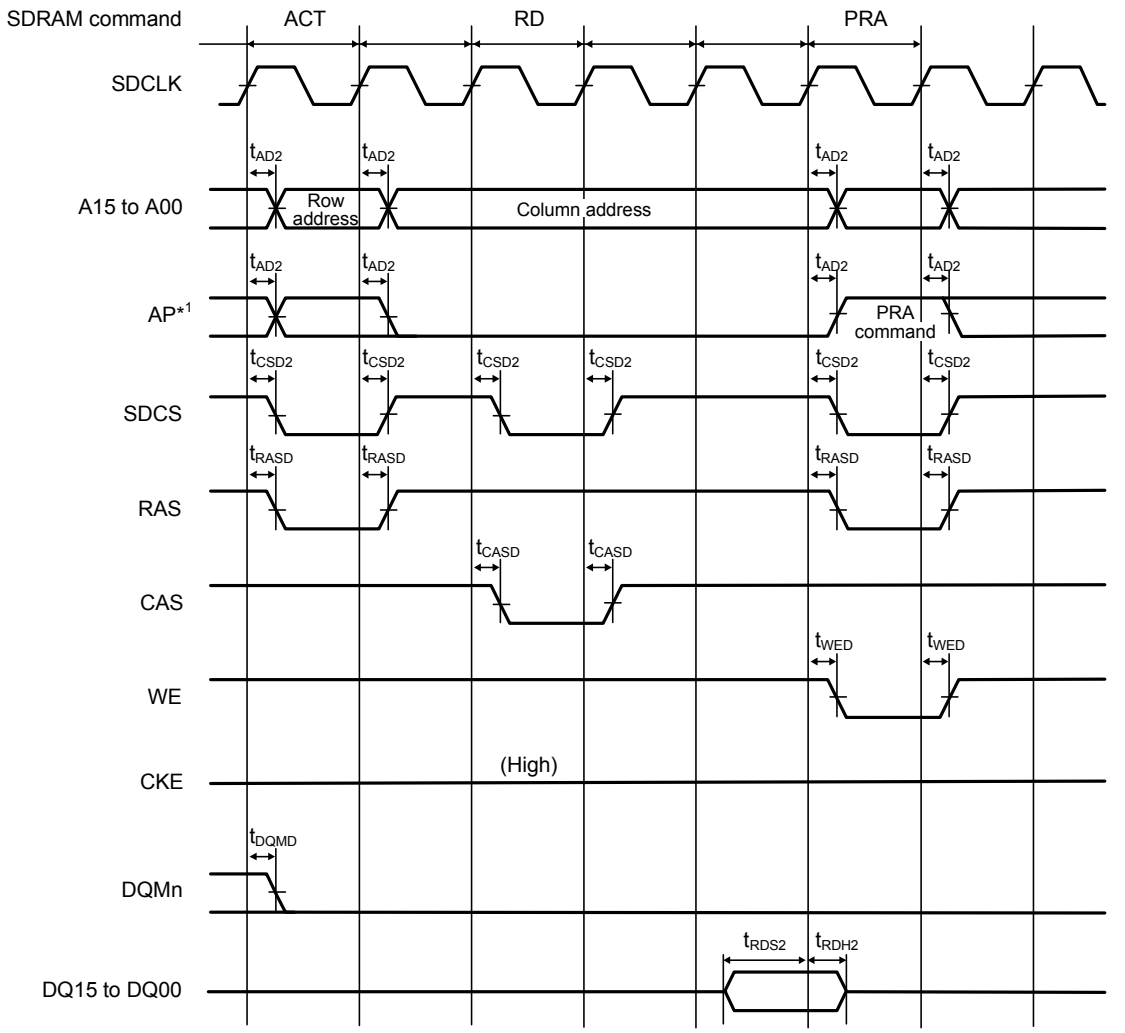
Table 2.18 Bus timing

Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	12.5	ns	Figure 2.14 to Figure 2.17
Byte control delay	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
Read data setup time	t_{RDS}	12.5	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
Write data delay	t_{WDD}	-	12.5	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	12.5	-	ns	Figure 2.18
WAIT hold time	t_{WTH}	0	-	ns	
Address delay 2 (SDRAM)	t_{AD2}	0.8	6.8	ns	Figure 2.19 to Figure 2.25
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	2.9	-	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	1.5	-	ns	
Write data delay 2 (SDRAM)	t_{WDD2}	-	6.8	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	-	ns	
WE delay (SDRAM)	t_{WED}	0.8	6.8	ns	
RAS delay (SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS delay (SDRAM)	t_{CASD}	0.8	6.8	ns	



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.19 SDRAM single read timing

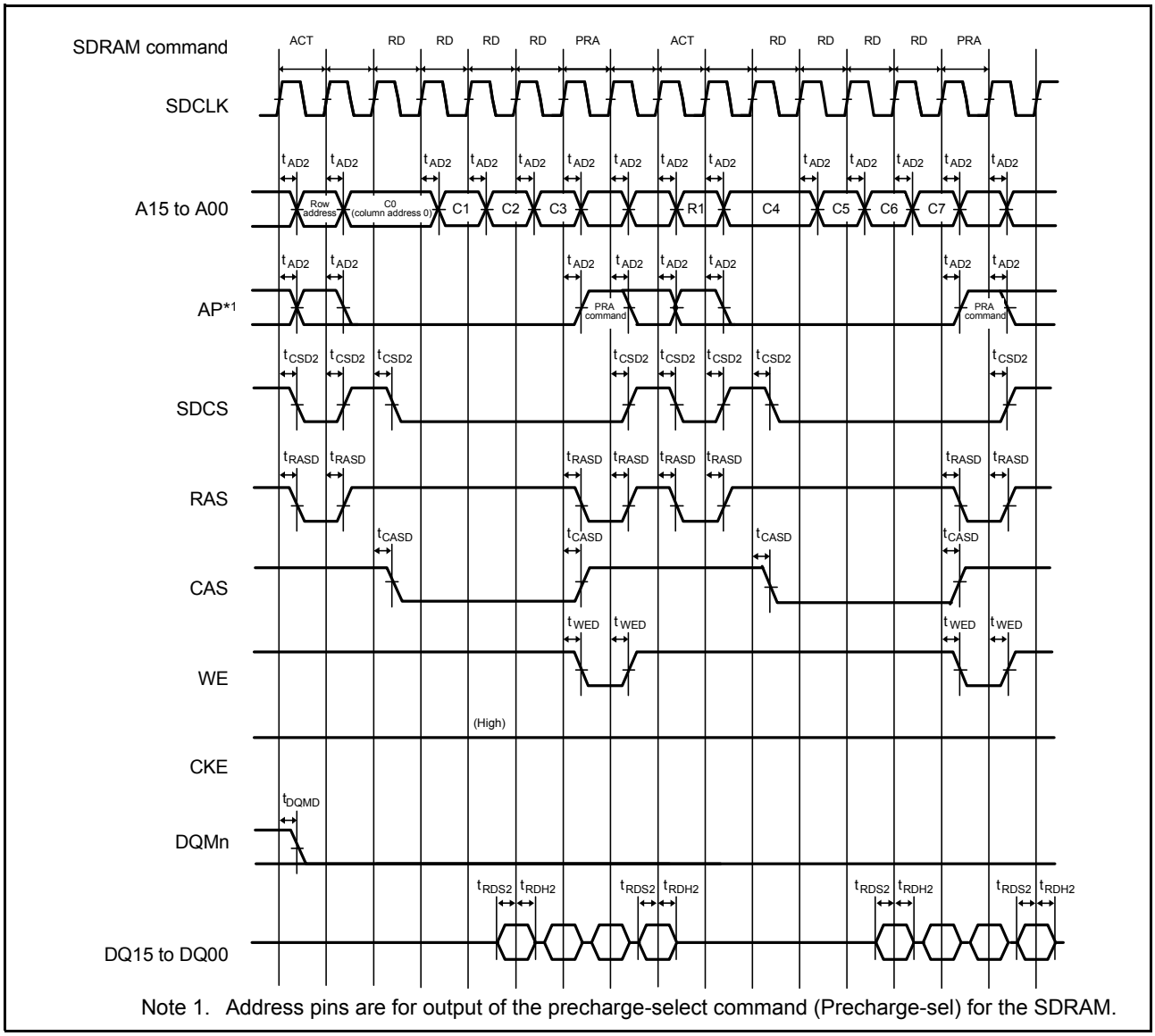
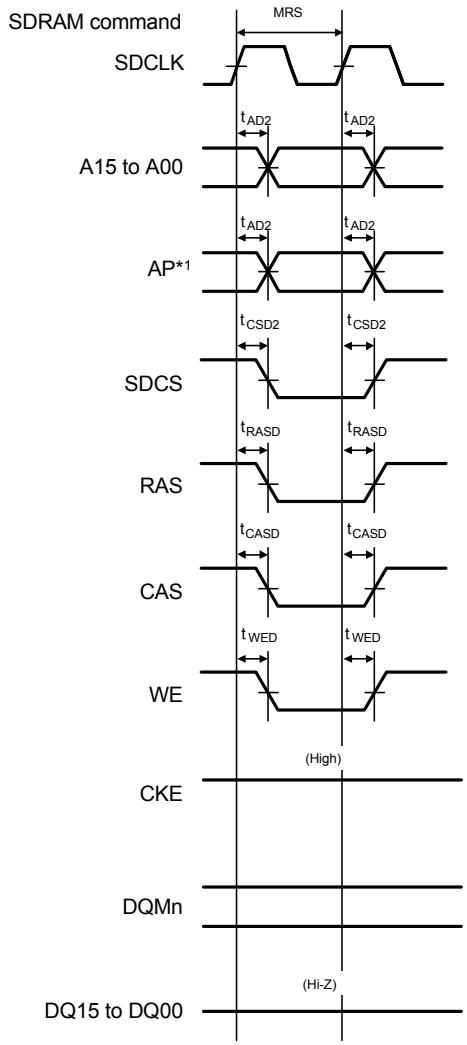


Figure 2.23 SDRAM multiple read line stride timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.24 SDRAM mode register set timing

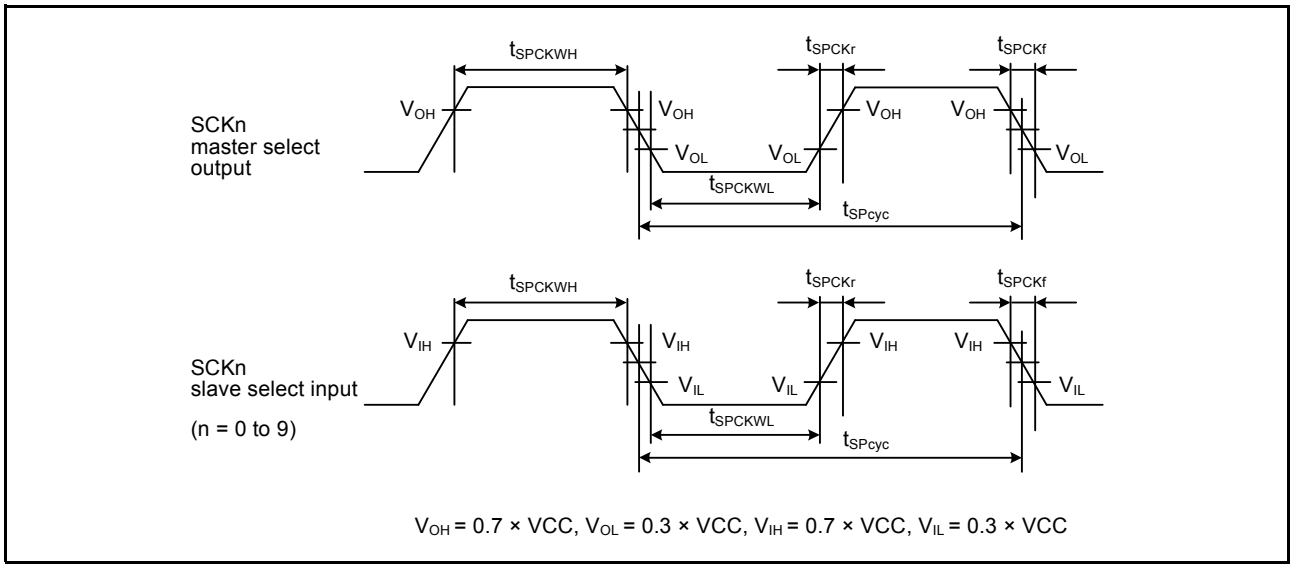


Figure 2.37 SCI simple SPI mode clock timing

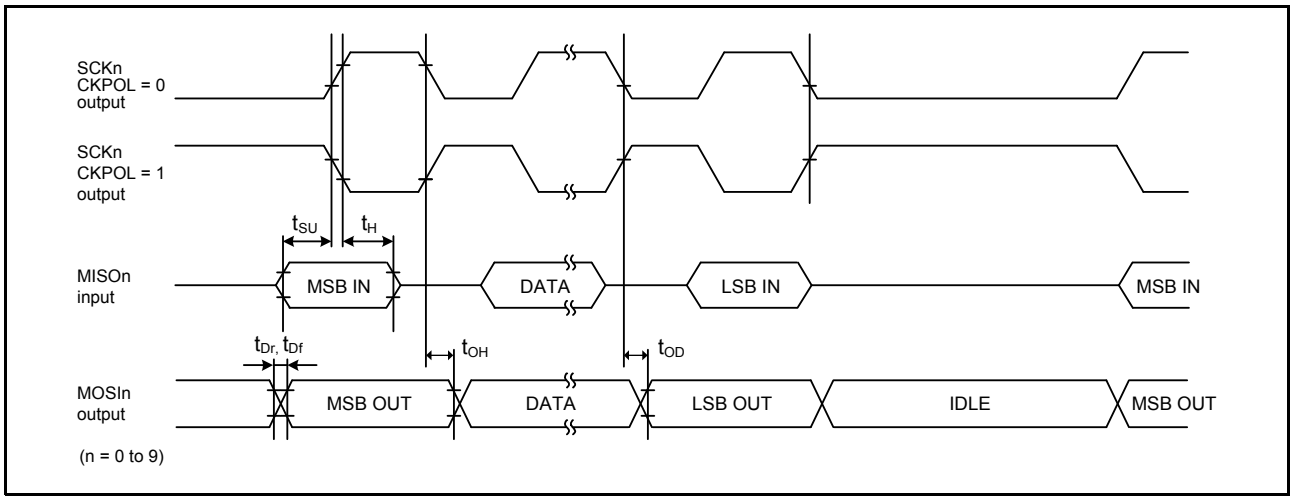


Figure 2.38 SCI simple SPI mode timing for master when CKPH = 1

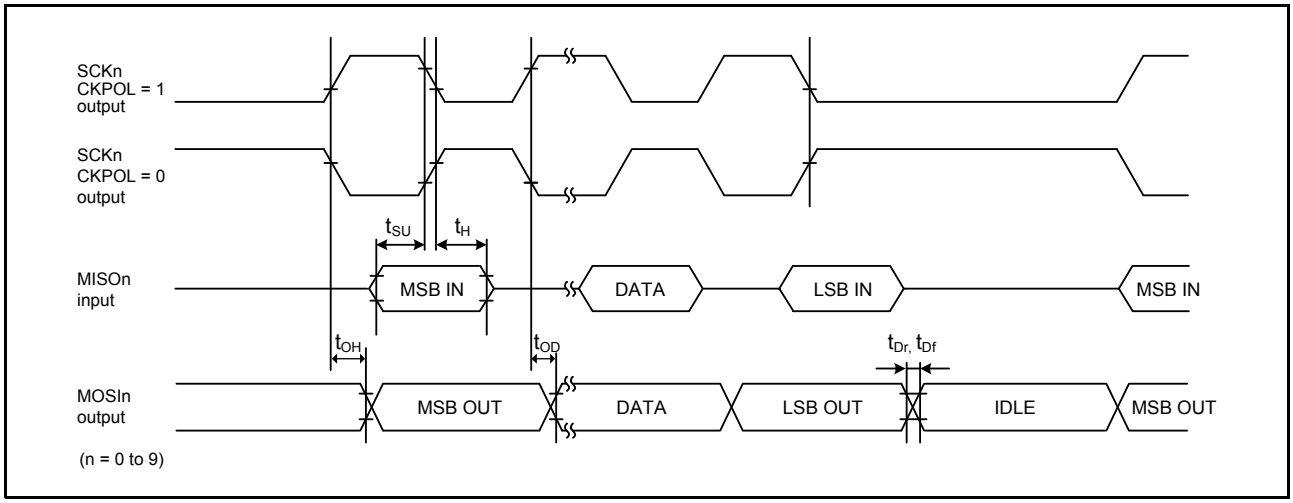


Figure 2.39 SCI simple SPI mode timing for master when CKPH = 0

2.3.11 SPI Timing

Table 2.25 SPI timing

Conditions:
(1) Middle drive output is selected with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.

Item			Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.43 C = 30 pF
		Slave		6	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 2.44 to Figure 2.49 C = 30 pF
		Slave		5	-		
	Data input hold time	Master	t_{HF}*4	0	-	ns	-
		Master	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		-
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc}$ - 10*2	$N \times t_{SPcyc}$ + 100 *2	ns	-
		Slave		6 x t_{Pcyc}	-	ns	-
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc}$ - 10 *3	$N \times t_{SPcyc}$ + 100 *3	ns	-
		Slave		6 x t_{Pcyc}	-	ns	-
	Data output delay	Master	t_{OD}	-	6.3	ns	Figure 2.44 to Figure 2.49 C = 30pF
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$6 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	2 x t_{Pcyc} + 28	ns	Figure 2.48 and Figure 2.49 C = 30pF
	Slave output release time		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set to an integer from 1 to 8 by the SPCKD register.
Note 3. N is set to an integer from 1 to 8 by the SSLND register.
Note 4. PCLKA division ratio set to 1/2.

2.3.17 PDC Timing

Table 2.32 PDC timing
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item		Symbol	Min	Max	Unit	Test conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 2.68
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 2.69
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	-	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 2.70
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

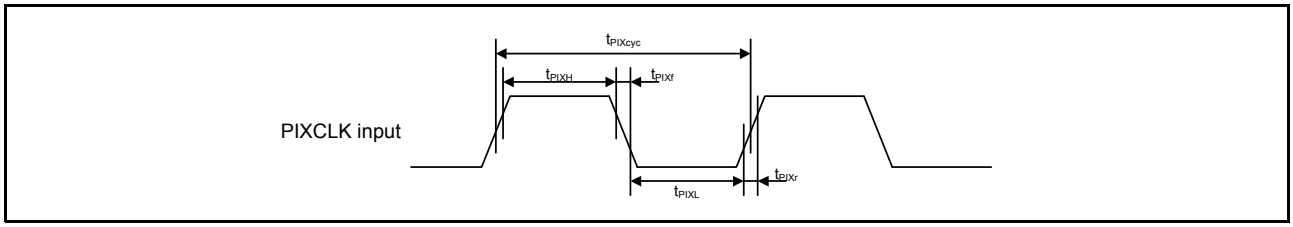


Figure 2.68 PDC input clock timing

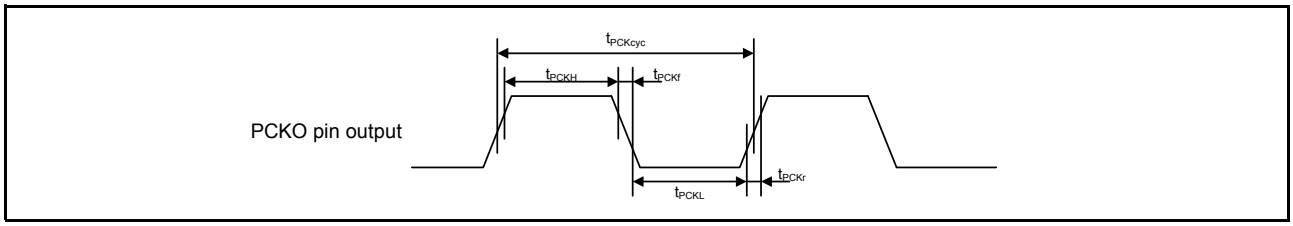


Figure 2.69 PDC output clock timing

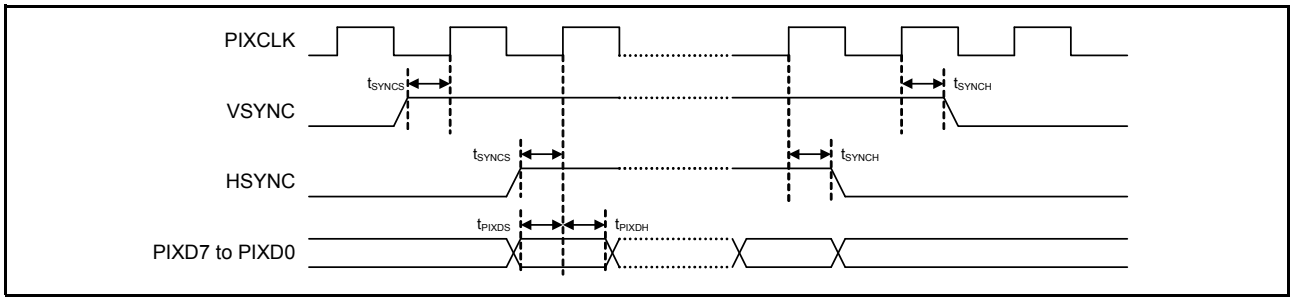


Figure 2.70 PDC AC timing

2.3.18 Graphics LCD Controller Timing

Table 2.33 Graphics LCD Controller timing
Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Typ	Max	Unit	Test conditions
LCD_EXTCLK input clock frequency		t_{Ecyc}	-	-	60*1	MHz	Figure 2.71
LCD_EXTCLK input clock low pulse width		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK input clock high pulse width		t_{WH}	0.45	-	0.55		
LCD_CLK output clock frequency		t_{Lcyc}	-	-	60*1	MHz	Figure 2.72
LCD_CLK output clock low pulse width		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 2.72
LCD_CLK output clock high pulse width		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 2.72
LCD data output delay timing	_A or _B combinations*2	t_{DD}	–3.5	-	4	ns	Figure 2.73
	_A and _B combinations*3		–5.0	-	5.5		
LCD data output rise time (0.8 to 2.0 V)		t_{Dr}	-	-	2		Figure 2.74
LCD data output fall time (2.0 to 0.8 V)		t_{Df}	-	-	2		

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz
Serial RGB888: Maximum 60 MHz (4x speed)
Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate
Note 3. Pins of group“_A” and “_B” combinations are used.

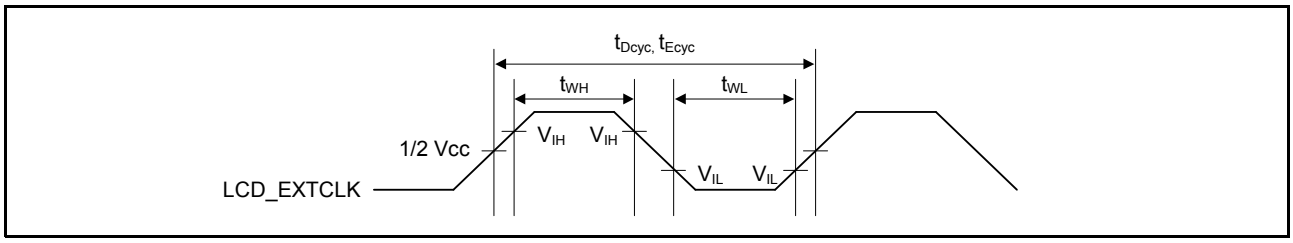


Figure 2.71 LCD_EXTCLK clock input timing

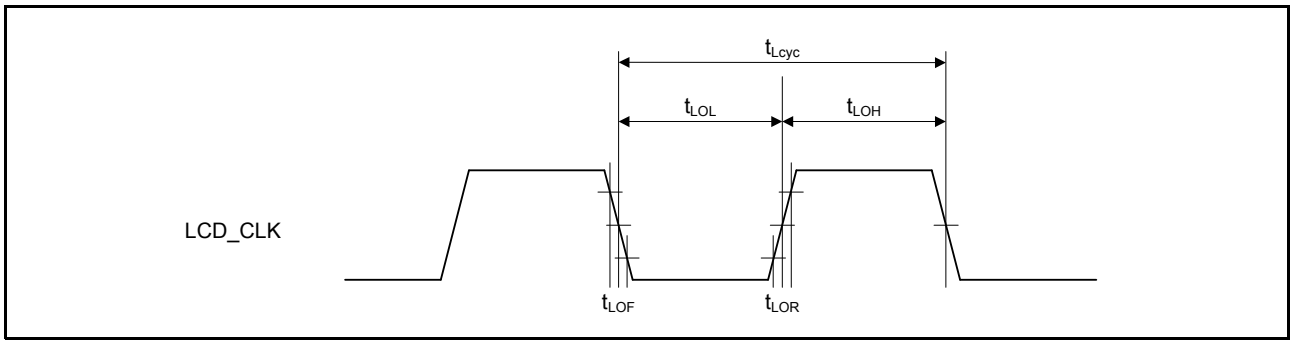


Figure 2.72 LCD_CLK clock output timing

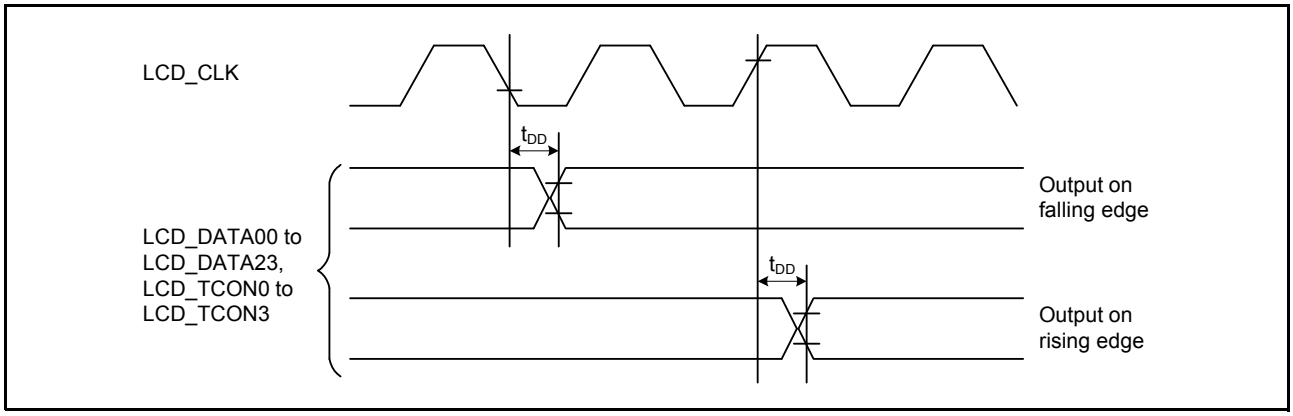


Figure 2.73 Display output timing

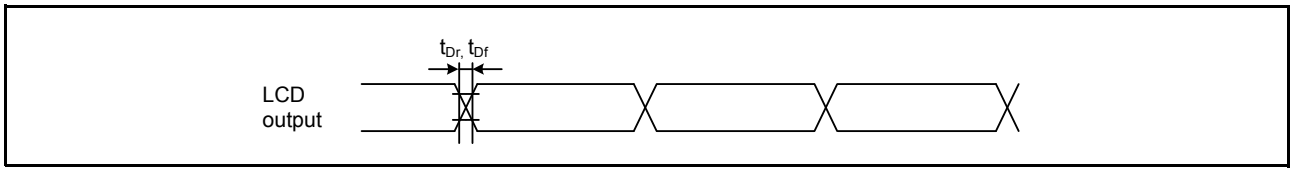


Figure 2.74 LCD output rise and fall times

2.4 USB Characteristics

2.4.1 USBHS Timing

Table 2.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics) (1/2)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-	-
	Input low voltage	V_{IL}	-	-	0.8	V	-	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-	-

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.83
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

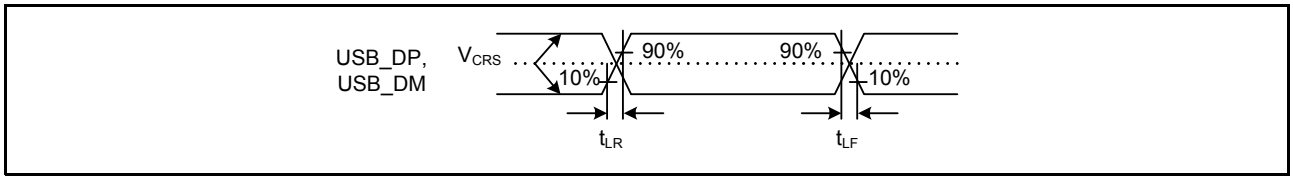


Figure 2.83 USB_DP and USB_DM output timing in low-speed mode

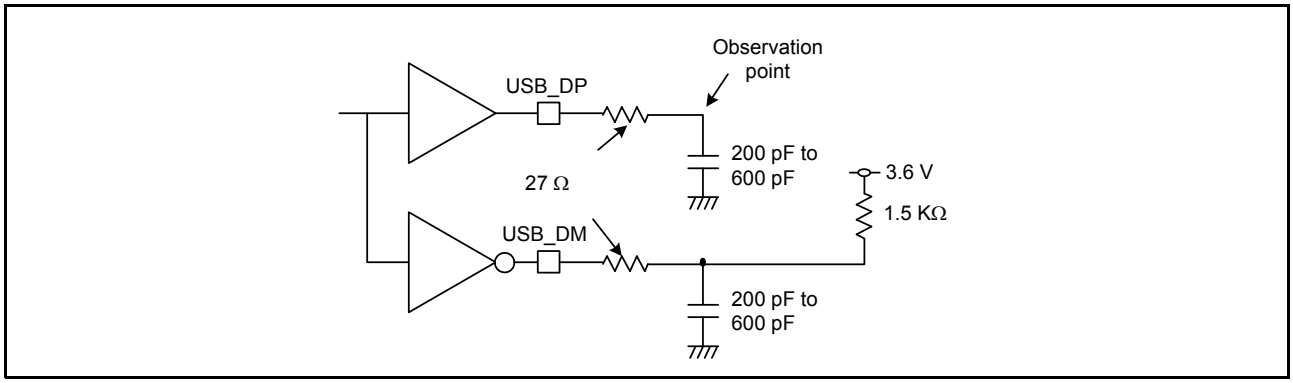


Figure 2.84 Test circuit in low-speed mode

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (1/2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-

Table 2.41 A/D conversion characteristics for unit 1 (2/2)
Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH – 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN103 to AN106)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 300Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116 to AN120)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
Note 1. The conversion time is the sum of the sampling and the comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 2.42 A/D internal reference voltage characteristics

Item	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.20	1.25	1.30	V	-