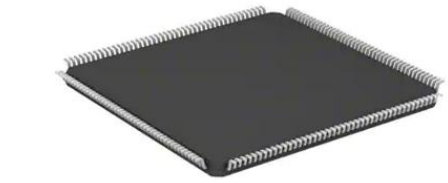
# Renesas Electronics America Inc - R7FS7G27G3A01CFC#AA0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 240MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB |
| Peripherals | DMA, LCD, LVD, POR, PWM, WDT |
| Number of I/O | 126 |
| Program Memory Size | 3MB (3M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LFQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27g3a01cfc-aa0 |

# 1. Overview

The S7G2 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

## 1.1 Function Outline

**Table 1.1 ARM core**

| Feature | Functional description |
|---|---|
| ARM Cortex-M4 | • Maximum operating frequency: up to 240 MHz<br>• ARM Cortex-M4 core:<br>- Revision: r0p1-01rel0<br>- ARMv7E-M architecture profile<br>- Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008<br>• ARM Memory Protection Unit (MPU):<br>- ARMv7 Protected Memory System Architecture<br>- 8 protect regions<br>• SysTick timer:<br>- Driven by LOCO clock |

**Table 1.2 Memory**

| Feature | Functional description |
|---|---|
| Code flash memory | Maximum 4 MB of code flash memory. See section 54, Flash Memory in User's Manual. |
| Data flash memory | 64 KB of data flash memory. See section 54, Flash Memory in User's Manual. |
| Memory Mirror Function (MMF) | The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual. |
| SRAM | On-chip high-speed SRAM providing either parity-bit or double-bit error detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 52, SRAM in User's Manual. |
| Standby SRAM | On-chip SRAM that can retain data in Deep Software Standby mode. See section 53, Standby SRAM in User's Manual. |

**Table 1.3 System (1/2)**

| Feature | Functional description |
|---|---|
| Operating modes | Two operating modes:<br>- Single-chip mode<br>- SCI or USB boot mode.<br>See section 3, Operating Modes in User's Manual. |

**Table 1.9 Communication interfaces (1/2)**

| Feature | Functional description |
|---|---|
| Serial Communications Interface (SCI) | The SCI is configurable to five asynchronous and synchronous serial interfaces:<br>• Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))<br>• 8-bit clock synchronous interface<br>• Simple IIC (master-only)<br>• Simple SPI<br>• Smart card interface.<br>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.<br>Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual. |
| IrDA Interface (IrDA) | The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual. |
| $I^2C$ Bus Interface (IIC) | The three-channel IIC conforms with and provides a subset of the NXP $I^2C$ bus (Inter-Integrated Circuit bus) interface functions. See section 36, $I^2C$ Bus Interface (IIC) in User's Manual. |
| Serial Peripheral Interface (SPI) | Two independent SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual. |
| Serial Sound Interface (SSI) | The SSI peripheral provides functionality to interface with digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSI supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSI includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface (SSI) in User's Manual. |
| Quad Serial Peripheral Interface (QSPI) | The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual. |
| Controller Area Network (CAN) Module | The CAN module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications.<br>The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual. |
| USB 2.0 Full-Speed Module (USBFS) | Full-Speed USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0.<br>The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual. |
| USB 2.0 High-Speed Module (USBHS) | High-Speed USB controller that can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0.<br>The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual. |

**Table 1.11 Human machine interfaces (2/2)**

| Feature | Functional description |
|---|---|
| Capacitive Touch Sensing Unit (CTSU) | The CTSU measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by the software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that fingers do not come into direct contact with the electrodes. See section 50, Capacitive Touch Sensing Unit (CTSU) in User's Manual. |

**Table 1.12 Graphics**

| Feature | Functional description |
|---|---|
| Graphics LCD Controller (GLCDC) | The GLCDC provides multiple functions and supports various data formats and panels. Key GLCDC features include:<br>• GPX bus master function for accessing graphics data<br>• Superimposition of three planes (single color background plane, graphic 1 plane, and graphic 2 plane)<br>• Support for many types of 32- or 16-bit per pixel graphics data and 8-, 4-, or 1-bit LUT data format<br>• Digital interface signal output supporting a video image size of WVGA or greater.<br>See section 57, Graphics LCD Controller (GLCDC) in User's Manual. |
| 2D Drawing Engine (DRW) | The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased.<br>Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box.<br>The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object.<br>If a pixel is inside the object, it is selected for rendering. If it is outside it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing.<br>Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW.<br>The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write).<br>The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write.<br>See section 55, 2D Drawing Engine (DRW) in User's Manual. |
| JPEG Codec (JPEG) | The JPEG Codec (JPEG) incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 56, JPEG Codec in User's Manual. |
| Parallel Data Capture Unit (PDC) | One PDC unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual. |

**Table 1.13 Data processing (1/2)**

| Feature | Functional description |
|---|---|
| Cyclic Redundancy Check (CRC) calculator | The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |
| Data Operation Circuit (DOC) | The DOC compares, adds, and subtracts 16-bit data. See section 51, Data Operation Circuit (DOC) in User's Manual. |

## 1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

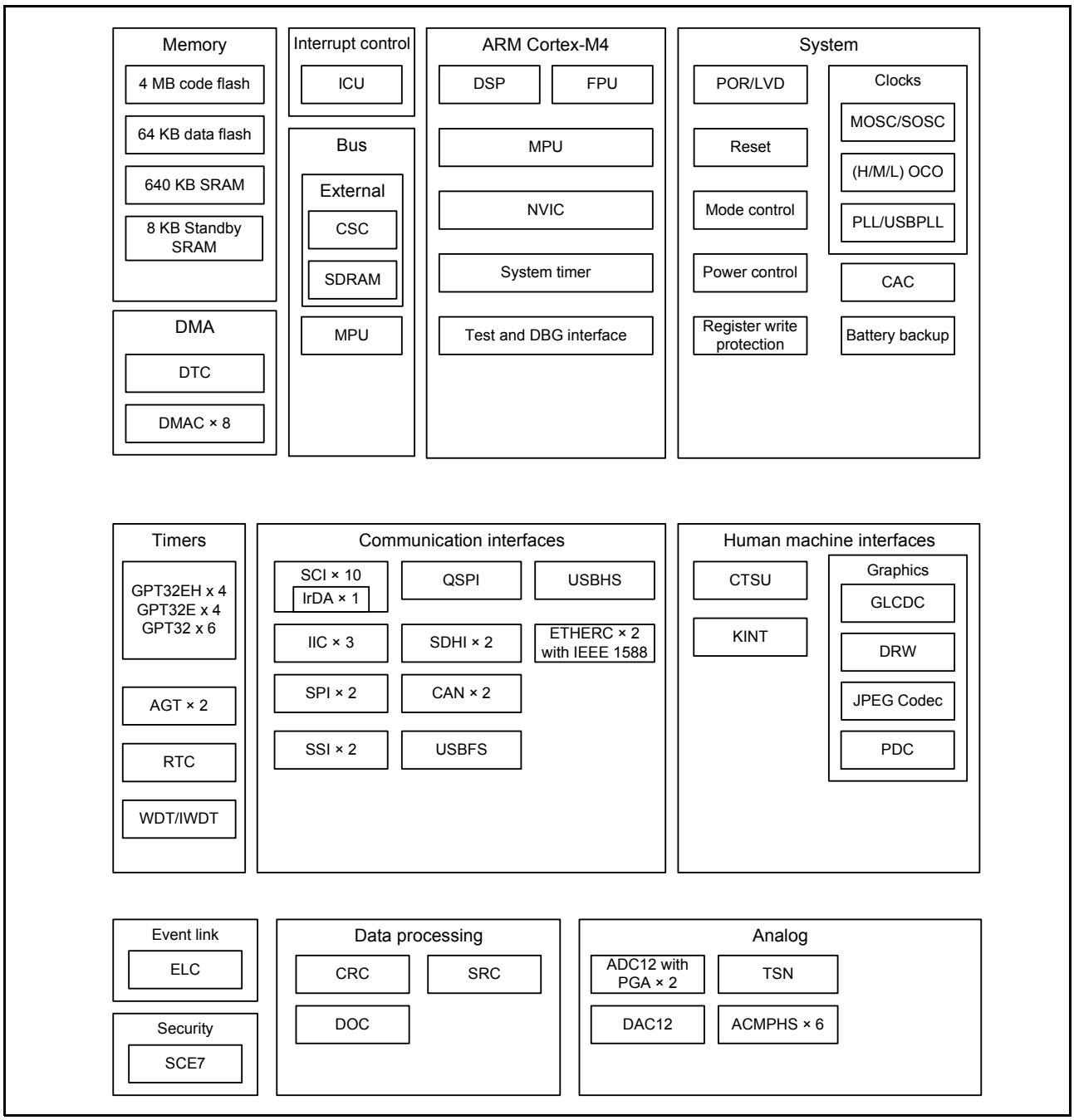



**Figure 1.1 Block diagram**

**Table 1.16 Pin functions (2/5)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| SDRAM interface | CKE | Output | SDRAM clock enable signal. |
| | SDCS | Output | SDRAM chip select signal, active LOW. |
| | RAS | Output | SDRAM low address strobe signal, active LOW. |
| | CAS | Output | SDRAM column address strobe signal, active LOW. |
| | WE | Output | SDRAM write enable signal, active LOW. |
| | DQM0 | Output | SDRAM I/O data mask enable signal for DQ07 to DQ00. |
| | DQM1 | Output | SDRAM I/O data mask enable signal for DQ15 to DQ08. |
| | A00 to A15 | Output | Address bus. |
| | DQ00 to DQ15 | I/O | Data bus. |
| Interrupt | NMI | Input | Non-maskable interrupt request pin. |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request pins. |
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pins. |
| | GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B | I/O | Input capture, output compare, or PWM output pins. |
| | GTIU | Input | Hall sensor input pin U. |
| | GTIV | Input | Hall sensor input pin V. |
| | GTIW | Input | Hall sensor input pin W. |
| | GTOUUP | Output | Three-phase PWM output for BLDC motor control (positive U phase). |
| | GTOULO | Output | Three-phase PWM output for BLDC motor control (negative U phase). |
| | GTOVUP | Output | Three-phase PWM output for BLDC motor control (positive V phase). |
| | GTOVLO | Output | Three-phase PWM output for BLDC motor control (negative V phase). |
| | GTOWUP | Output | Three-phase PWM output for BLDC motor control (positive W phase). |
| | GTOWLO | Output | Three-phase PWM output for BLDC motor control (negative W phase). |
| AGT | AGTEE0, AGTEE1 | Input | External event input enable signals. |
| | AGTIO0, AGTIO1 | I/O | External event input and pulse output pins. |
| | AGTO0, AGTO1 | Output | Pulse output pins. |
| | AGTOA0, AGTOA1 | Output | Output compare match A output pins. |
| | AGTOB0, AGTOB1 | Output | Output compare match B output pins. |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock. |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins. |
| SCI | SCK0 to SCK9 | I/O | Input/output pins for the clock (clock synchronous mode). |
| | RXD0 to RXD9 | Input | Input pins for received data (asynchronous mode/clock synchronous mode). |
| | TXD0 to TXD9 | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode). |
| | CTS0_RTS0 to CTS9_RTS9 | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active LOW. |
| | SCL0 to SCL9 | I/O | Input/output pins for the IIC clock (simple IIC). |
| | SDA0 to SDA9 | I/O | Input/output pins for the IIC data (simple IIC). |
| | SCK0 to SCK9 | I/O | Input/output pins for the clock (simple SPI). |
| | MISO0 to MISO9 | I/O | Input/output pins for slave transmission of data (simple SPI). |
| | MOSI0 to MOSI9 | I/O | Input/output pins for master transmission of data (simple SPI). |
| | SS0 to SS9 | Input | Chip-select input pins (simple SPI), active LOW. |
| IIC | SCL0 to SCL2 | I/O | Input/output pins for the clock. |
| | SDA0 to SDA2 | I/O | Input/output pins for data. |

**Table 1.17 Pin list (9/12)**

| Pin number | | | | | | Power, System, Clock, Debug, | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BGA224 | BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSI | MII (25 MHz) | RMII (50 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | Interrupt | GLCDC, PDC |
| J5 | - | - | - | - | - | | PA03 | - | - | - | - | - | - | - | - | RXD7_B/MISO7_B/SCL7_B | - | - | - | - | - | - | - | - | - | - | IRQ9 | - |
| H6 | - | - | - | - | - | | PA02 | - | - | - | - | - | - | - | - | TXD7_B/MOSI7_B/SDA7_B | - | - | - | - | - | - | - | - | - | - | IRQ10 | - |
| J6 | H2 | 113 | - | - | - | | PA01 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA06_B |
| J7 | H4 | 114 | - | - | - | | PA00 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA05_B |
| K5 | J4 | 115 | - | - | - | | P607 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA04_B |
| K6 | J1 | 116 | - | - | - | | P606 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA03_B |
| K1 | J2 | 117 | H2 | 93 | - | | P605 | D11 | DQ11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K2 | J3 | 118 | G4 | 94 | - | | P604 | D12 | DQ12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K3 | K3 | 119 | H3 | 95 | - | | P603 | D13 | DQ13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| L1 | K1 | 120 | J1 | 96 | 65 | | P602 | EBCLK | SDCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA04_A |
| L2 | K2 | 121 | J2 | 97 | 66 | - | P601 | WR/WR0 | DQM0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA03_A |
| L3 | L1 | 122 | H4 | 98 | 67 | - | P600 | RD | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA02_A |
| M2 | K4 | 123 | K2 | 99 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| M1 | L4 | 124 | K1 | 100 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K4 | L2 | 125 | J3 | 101 | 68 | - | P107 | D07 | DQ07 | - | - | GTIOC8A_A | - | - | CTS8_RTS8_A/SS8_A | - | - | - | - | - | - | - | - | - | - | - | KR07 | LCD_DATA01_A |
| L4 | M1 | 126 | K3 | 102 | 69 | - | P106 | D06 | DQ06 | - | - | GTIOC8B_A | - | - | SCK8_A | - | - | SSLA3_A | - | - | - | - | - | - | - | - | KR06 | LCD_DATA00_A |
| M3 | L3 | 127 | J4 | 103 | 70 | - | P105 | D05 | DQ05 | - | GTETRGA_C | - | - | - | TXD8_A/MOSI8_A/SDA8_A | - | - | SSLA2_A | - | - | - | - | - | - | - | - | IRQ0/KR05 | LCD_TCON3_A |
| N3 | M2 | 128 | L3 | 104 | 71 | - | P104 | D04 | DQ04 | - | GTETRGB_B | - | - | - | RXD8_A/MISO8_A/SCL8_A | - | - | SSLA1_A | - | - | - | - | - | - | - | - | IRQ1/KR04 | LCD_TCON2_A |

# 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr

Figure 2.1 shows the timing conditions.

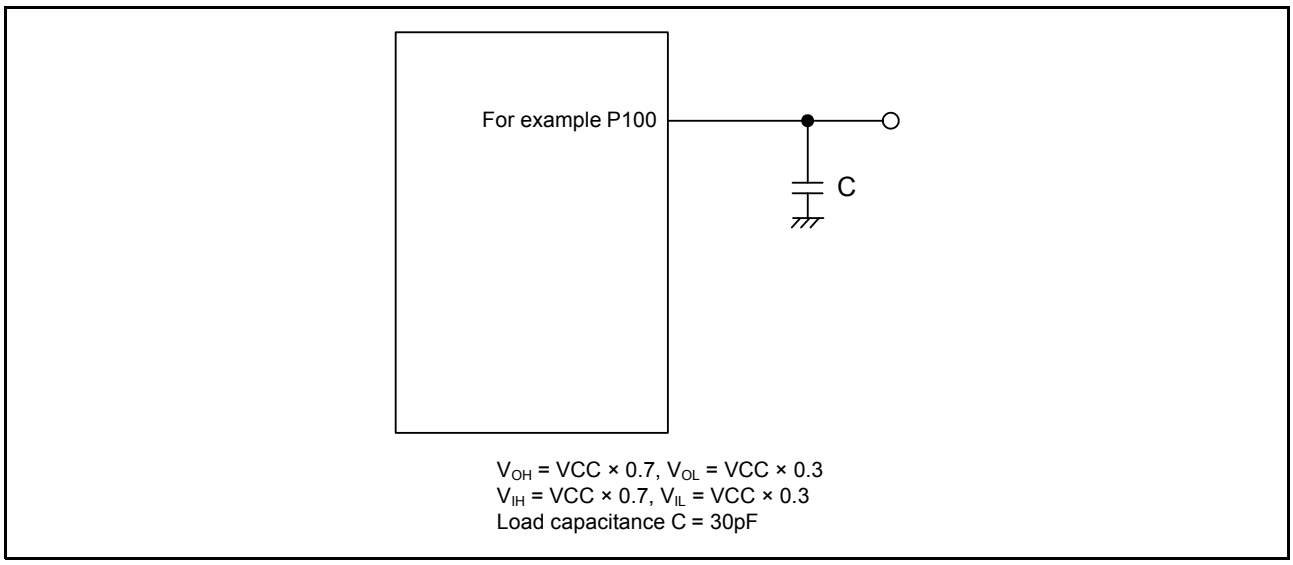



**Figure 2.1 Input or output timing measurement conditions**

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VCC, VCC_USB *2 | –0.3 to +4.6 | V |
| VBATT power supply voltage | VBATT | –0.3 to +4.6 | V |
| Input voltage (except for 5V-tolerant ports*1) | $V_{in}$ | –0.3 to VCC + 0.3 | V |
| Input voltage (5V-tolerant ports*1) | $V_{in}$ | –0.3 to +5.8 | V |
| Reference power supply voltage | VREFH/VREFH0 | –0.3 to VCC + 0.3 | V |
| Analog power supply voltage | AVCC0 *2 | –0.3 to +4.6 | V |
| USBHS power supply voltage | VCC_USBHS | –0.3 to +4.6 | V |
| USBHS analog power supply voltage | AVCC_USBHS | –0.3 to +4.6 | V |
| Switching regulator power supply voltage | VCC_DCDC | –0.3 to +4.6 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to AVCC0 + 0.3 | V |
| Operating temperature*3 *4 | $T_{opr}$ | –40 to +105 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

**Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.**

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.

Note 2. Connect AVCC0 and VCC_USB to VCC.

Note 3. See section 2.2.1, Tj/Ta Definition.

Note 4. Contact a Renesas Electronics sales office for information on derating operation when $T_a$ = +85°C to +105°C.

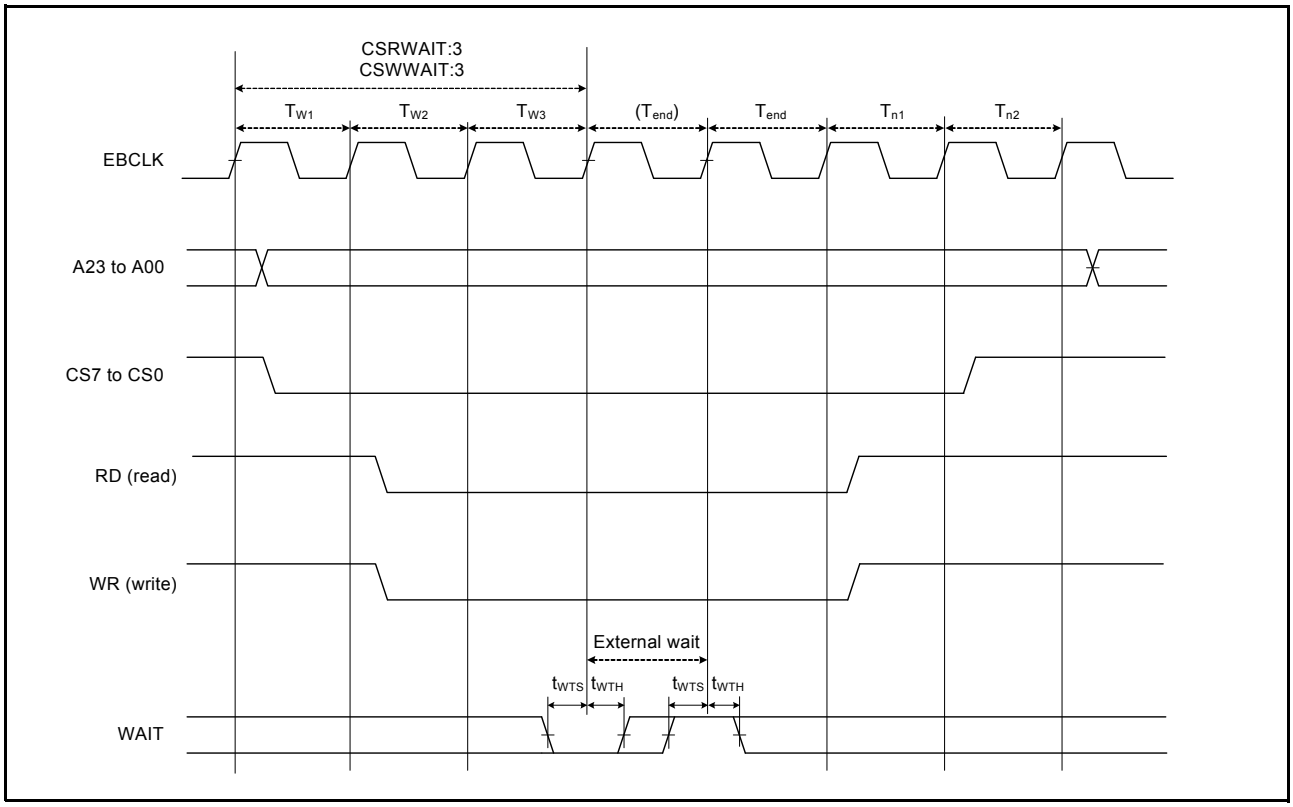
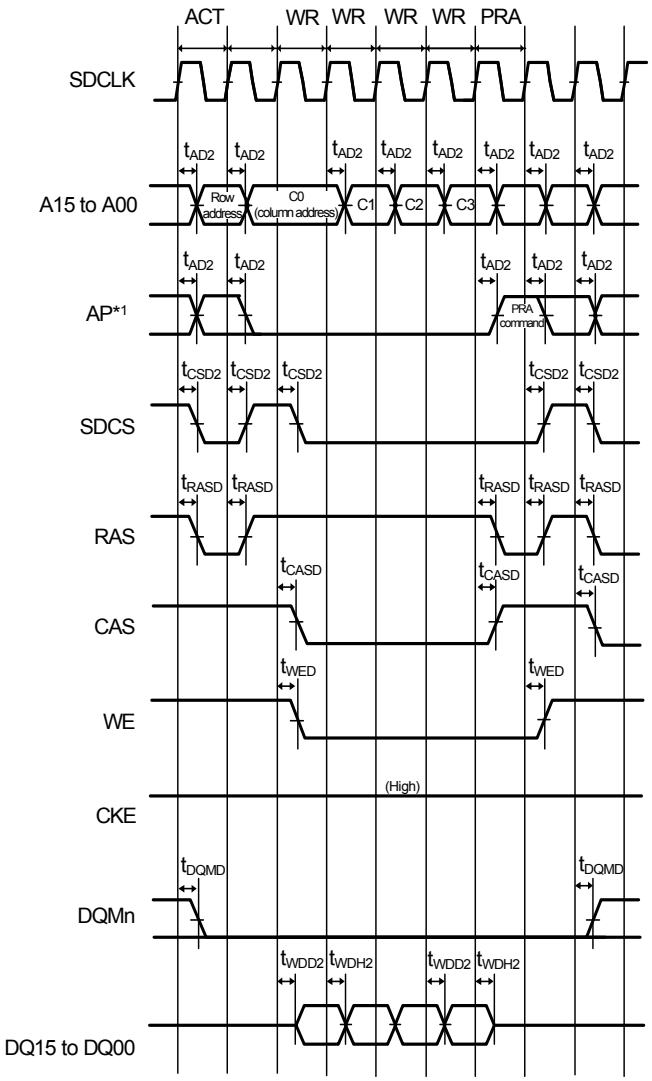



**Figure 2.18 External bus timing for external wait control**




Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

**Figure 2.22 SDRAM multiple write timing**

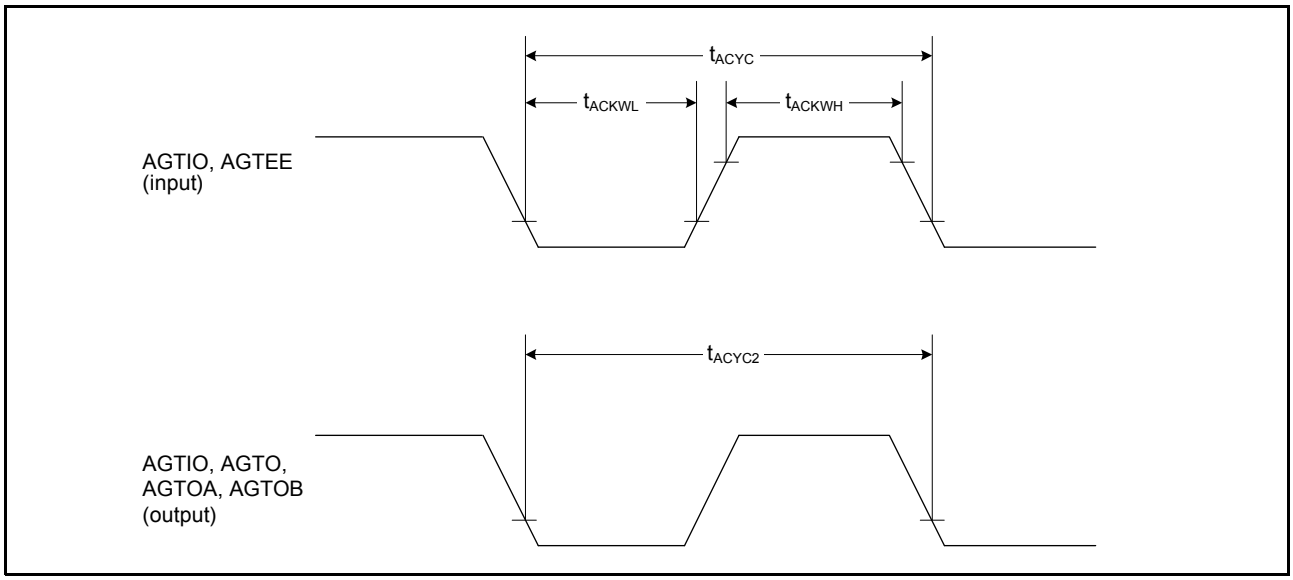



**Figure 2.32 AGT input/output timing**

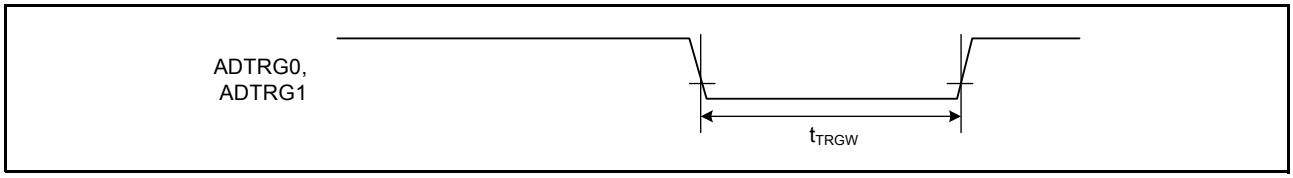



**Figure 2.33 ADC12 trigger input timing**

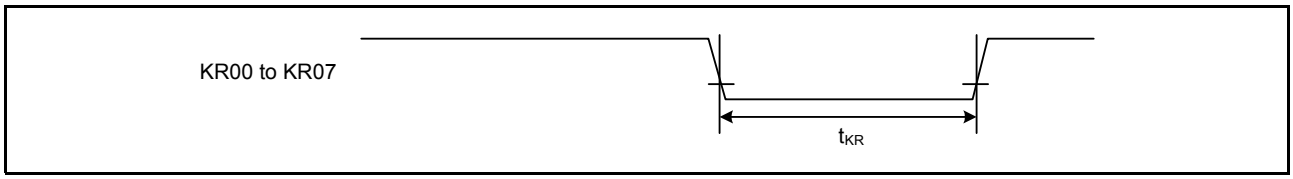



**Figure 2.34 Key interrupt input timing**

## 2.3.8 PWM Delay Generation Circuit Timing

**Table 2.20 PWM Delay Generation Circuit timing**

| Item | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | - | 260 | - | ps | PCLKD = 120 MHz |
| DNL*1 | - | ±2.0 | - | LSB | - |

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

## 2.3.9 CAC Timing

**Table 2.21 CAC timing**

| Item | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq tcac$*2 | $t_{CACREF}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | - | - | ns | - |
| | | $t_{PBcyc} > tcac$*2 | | $5 \times t_{cac} + 6.5 \times t_{PBcyc}$ | - | - | ns | |

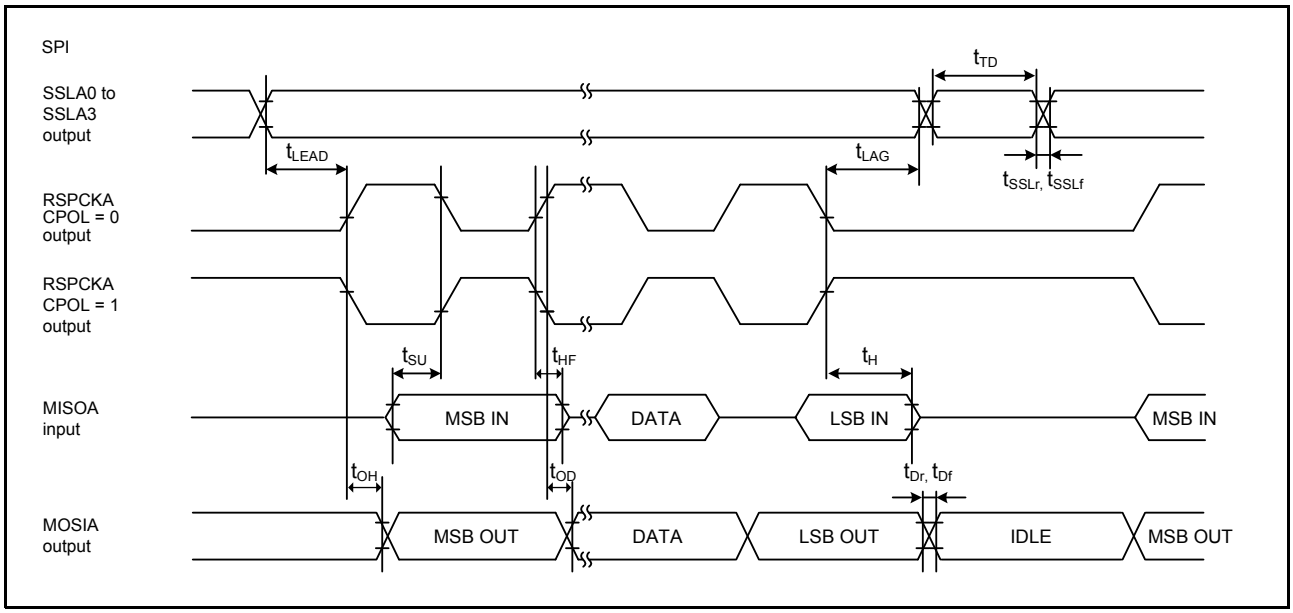



**Figure 2.47 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2**

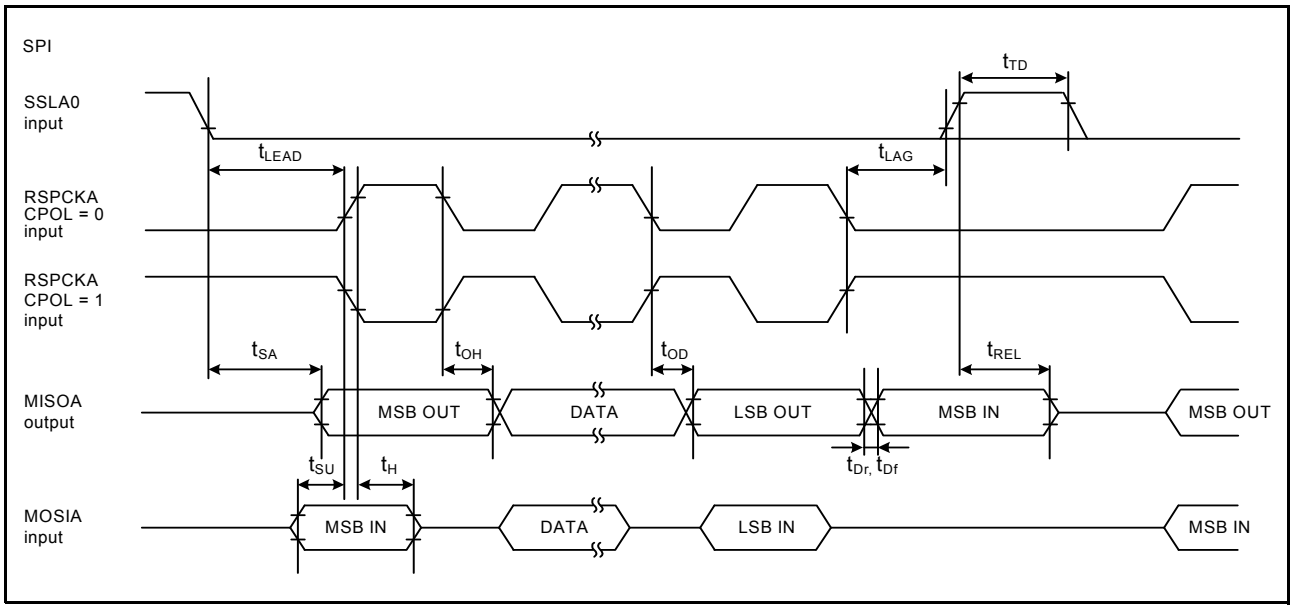



**Figure 2.48 SPI timing for slave when CPHA = 0**

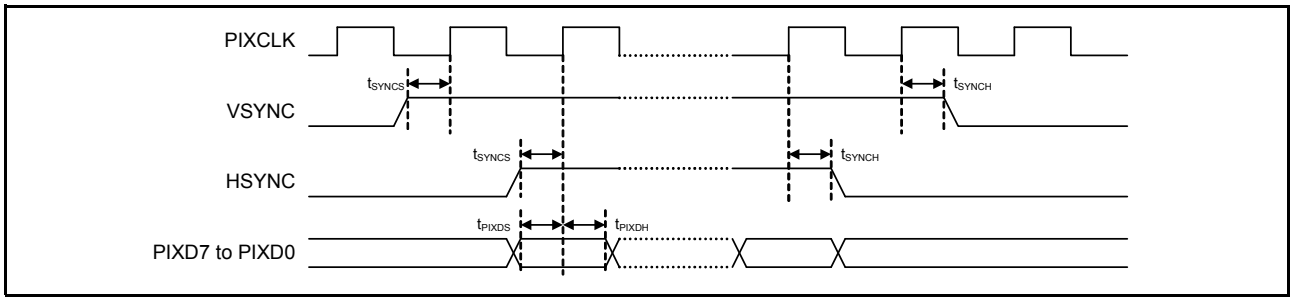



**Figure 2.70 PDC AC timing**

## 2.3.18 Graphics LCD Controller Timing

**Table 2.33 Graphics LCD Controller timing**
Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| LCD_EXTCLK input clock frequency | | $t_{Ecyc}$ | - | - | 60*1 | MHz | Figure 2.71 |
| LCD_EXTCLK input clock low pulse width | | $t_{WL}$ | 0.45 | - | 0.55 | $t_{Ecyc}$ | |
| LCD_EXTCLK input clock high pulse width | | $t_{WH}$ | 0.45 | - | 0.55 | | |
| LCD_CLK output clock frequency | | $t_{Lcyc}$ | - | - | 60*1 | MHz | Figure 2.72 |
| LCD_CLK output clock low pulse width | | $t_{LOL}$ | 0.4 | - | 0.6 | $t_{Lcyc}$ | Figure 2.72 |
| LCD_CLK output clock high pulse width | | $t_{LOH}$ | 0.4 | - | 0.6 | $t_{Lcyc}$ | Figure 2.72 |
| LCD data output delay timing | _A or _B combinations*2 | $t_{DD}$ | –3.5 | - | 4 | ns | Figure 2.73 |
| | _A and _B combinations*3 | | –5.0 | - | 5.5 | | |
| LCD data output rise time (0.8 to 2.0 V) | | $t_{Dr}$ | - | - | 2 | | Figure 2.74 |
| LCD data output fall time (2.0 to 0.8 V) | | $t_{Df}$ | - | - | 2 | | |

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz
Serial RGB888: Maximum 60 MHz (4x speed)
Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate
Note 3. Pins of group“_A” and “_B” combinations are used.

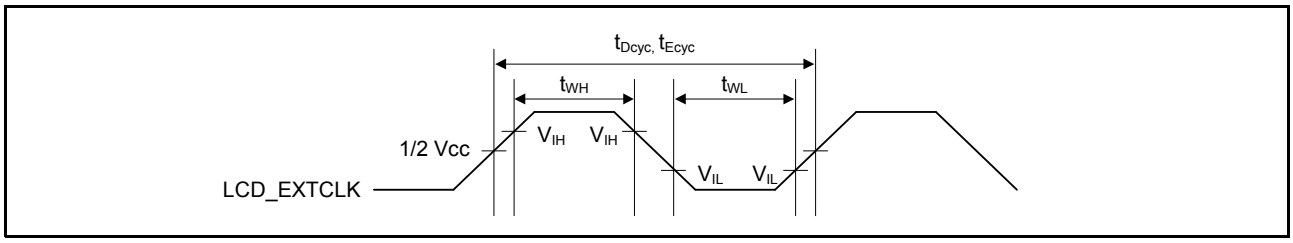



**Figure 2.71 LCD_EXTCLK clock input timing**

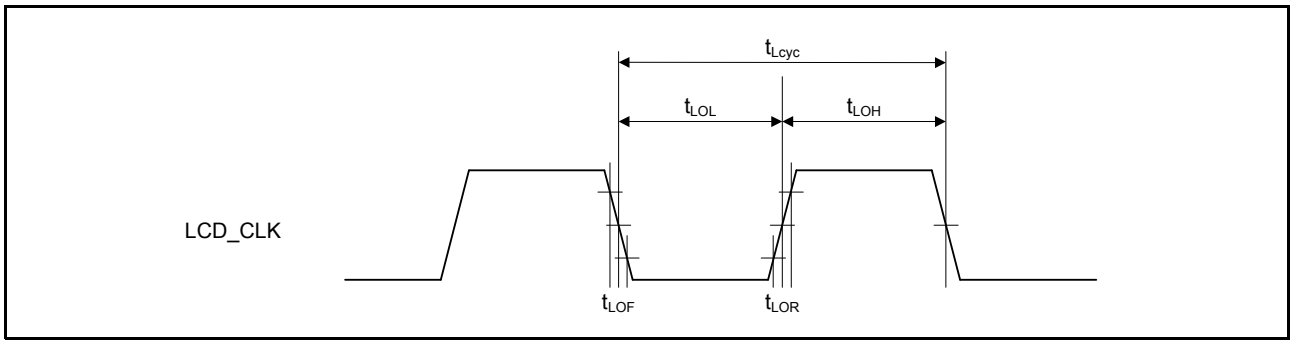



**Figure 2.72 LCD_CLK clock output timing**

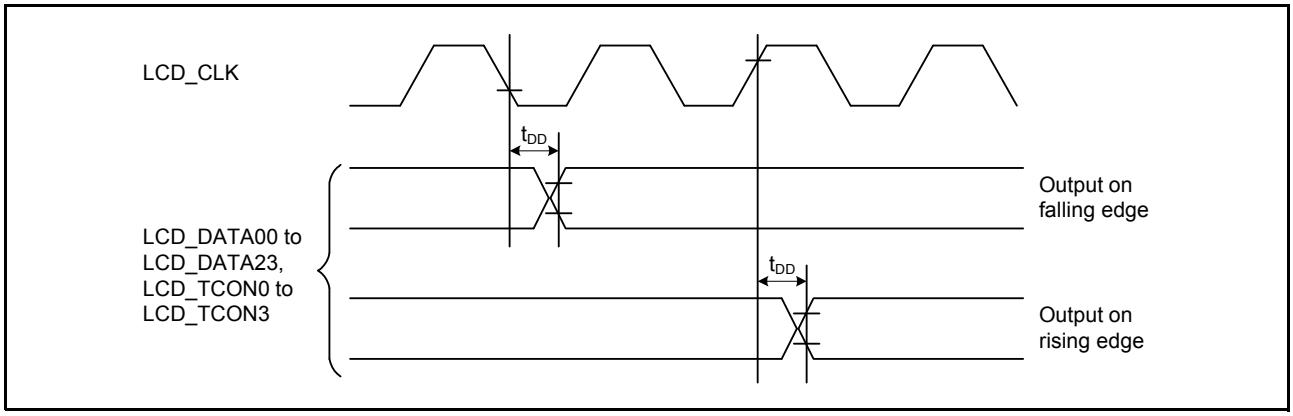



**Figure 2.73 Display output timing**

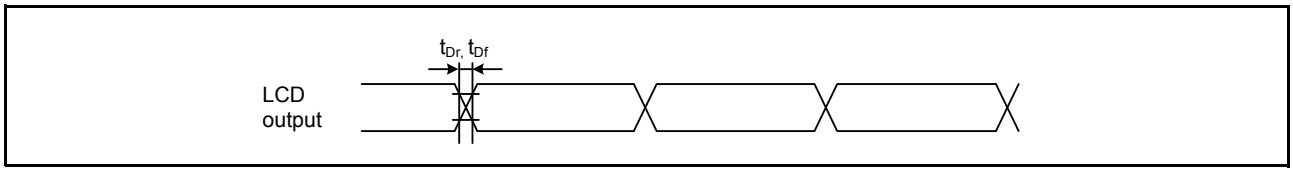



**Figure 2.74 LCD output rise and fall times**

## 2.4 USB Characteristics

### 2.4.1 USBHS Timing

**Table 2.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics) (1/2)**

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|---|
| Input characteristics | Input high voltage | $V_{IH}$ | 2.0 | - | - | V | - | - |
| | Input low voltage | $V_{IL}$ | - | - | 0.8 | V | - | - |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | - | - | V | \| USBHS_DP - USBHS_DM \| | - |
| | Differential common-mode range | $V_{CM}$ | 0.8 | - | 2.5 | V | - | - |

**Table 2.35 USBHS full-speed characteristics (USBHS_DP and USBHS_DM pin characteristics) (2/2)**
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|---|
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | - | 3.6 | V | $I_{OH}$ = –200 μA | - |
| | Output low voltage | $V_{OL}$ | 0.0 | - | 0.3 | V | $I_{OL}$= 2 mA | - |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | - | 2.0 | V | - | Figure 2.77, Figure 2.78 |
| | Rise time | $t_{LR}$ | 4 | - | 20 | ns | - | |
| | Fall time | $t_{LF}$ | 4 | - | 20 | ns | - | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 90 | - | 111.11 | % | $t_{FR}$ / $t_{FF}$ | - |
| | Output resistance | $Z_{DRV}$ | 40.5 | - | 49.5 | Ω | Rs Not used (PHYSET.REPSEL[1:0] = 01b and PHYSET. HSEB = 0) | |
| DC characteristics | USBHS_DM pull-up resistor (device) | $R_{pu}$ | 0.900 | - | 1.575 | kΩ | During idle state | |
| | | | 1.425 | - | 3.090 | kΩ | During transmission and reception | |
| | USBHS_DP/USBHS_DM pull-down resistor (host) | $R_{pd}$ | 14.25 | - | 24.80 | kΩ | - | |

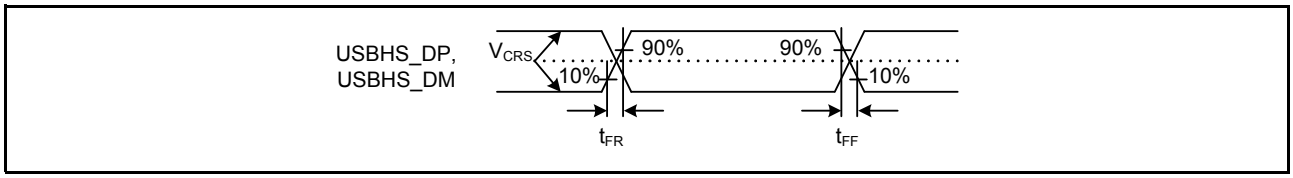



**Figure 2.77 USBHS_DP and USBHS_DM output timing in full-speed mode**

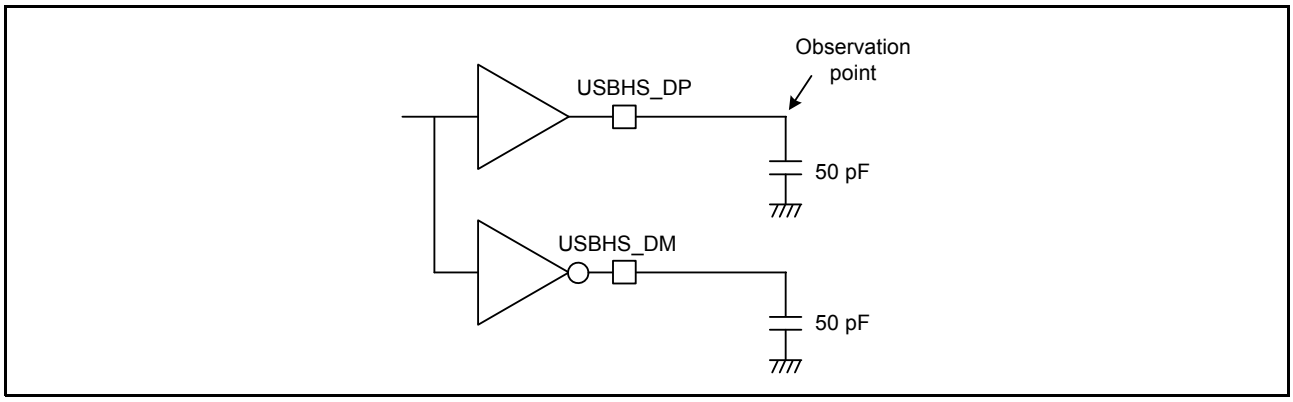



**Figure 2.78 Test circuit in full-speed mode**

**Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics) (1/2)**
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Squelch detect sensitivity | $V_{HSSQ}$ | 100 | - | 150 | mV | Figure 2.79 |
| | Disconnect detect sensitivity | $V_{HSDSC}$ | 525 | - | 625 | mV | Figure 2.80 |
| | Common-mode voltage | $V_{HSCM}$ | –50 | - | 500 | mV | - |
| Output characteristics | Idle state | $V_{HSOI}$ | –10.0 | - | 10 | mV | - |
| | Output high voltage | $V_{HSOH}$ | 360 | - | 440 | mV | |
| | Output low voltage | $V_{HSOL}$ | –10.0 | - | 10 | mV | |
| | Chirp J output voltage (difference) | $V_{CHIRPJ}$ | 700 | - | 1100 | mV | |
| | Chirp K output voltage (difference) | $V_{CHIRPK}$ | –900 | - | –500 | mV | |

**Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics) (2/2)**
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| AC characteristics | Rise time | $t_{HSR}$ | 500 | - | - | ps | Figure 2.81 |
| | Fall time | $t_{HSF}$ | 500 | - | - | ps | |
| | Output resistance | $Z_{HSDRV}$ | 40.5 | - | 49.5 | Ω | - |

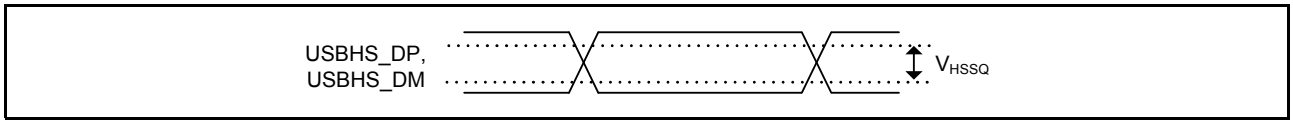



**Figure 2.79 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode**

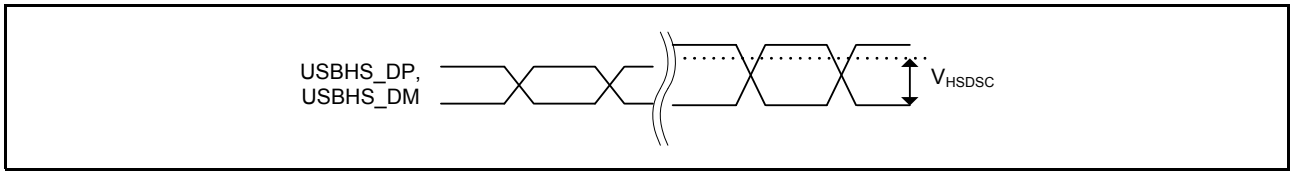



**Figure 2.80 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode**

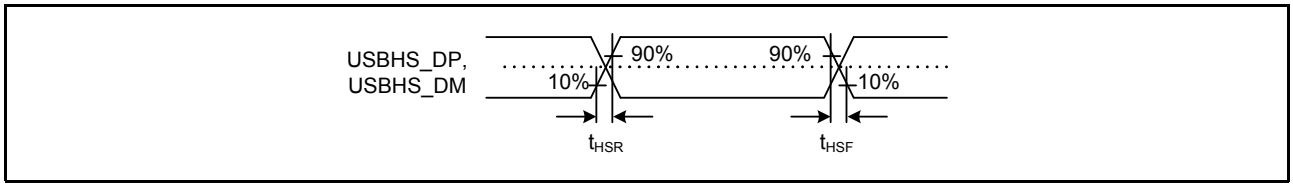



**Figure 2.81 USBHS_DP and USBHS_DM output timing in high-speed mode**

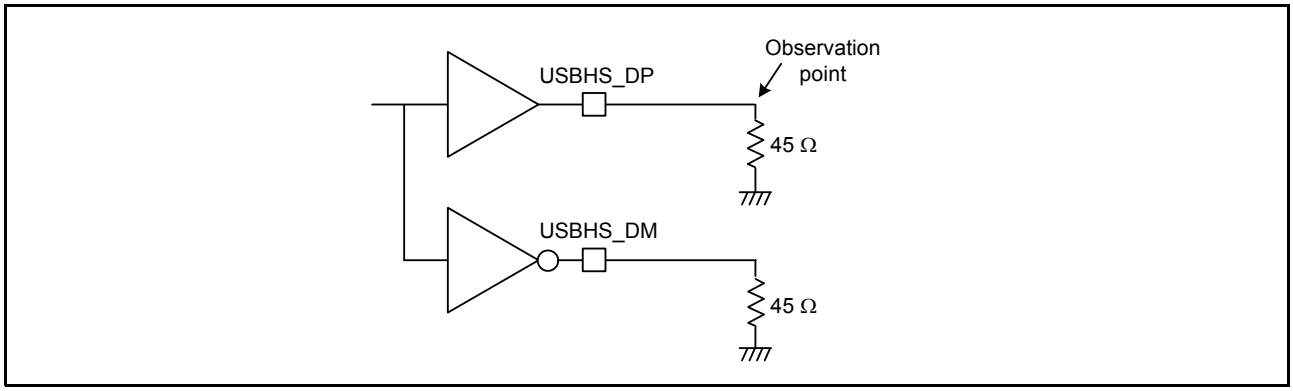



**Figure 2.82 Test circuit in high-speed mode**

**Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)**
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

| Item | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Battery Charging Specification | D+ sink current | $I_{DP\_SINK}$ | 25 | 175 | μA | - |
| | D– sink current | $I_{DM\_SINK}$ | 25 | 175 | μA | - |
| | DCD source current | $I_{DP\_SRC}$ | 7 | 13 | μA | - |
| | Data detection voltage | $V_{DAT\_REF}$ | 0.25 | 0.4 | V | - |
| | D+ source voltage | $V_{DP\_SRC}$ | 0.5 | 0.7 | V | Output current = 250 μA |
| | D– source voltage | $V_{DM\_SRC}$ | 0.5 | 0.7 | V | Output current = 250 μA |

**Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (2/2)**
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | - | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output low voltage | $V_{OL}$ | 0.0 | - | 0.3 | V | $I_{OL}$= 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | - | 2.0 | V | Figure 2.85 |
| | Rise time | $t_{LR}$ | 4 | - | 20 | ns | |
| | Fall time | $t_{LF}$ | 4 | - | 20 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 90 | - | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | - | 44 | Ω | USBFS: Rs = 27 Ω included |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | $R_{pu}$ | 0.900 | - | 1.575 | kΩ | During idle state |
| | | | 1.425 | - | 3.090 | kΩ | During transmission and reception |
| | USB_DP and USB_DM pull-down resistance in host controller mode | $R_{pd}$ | 14.25 | - | 24.80 | kΩ | - |

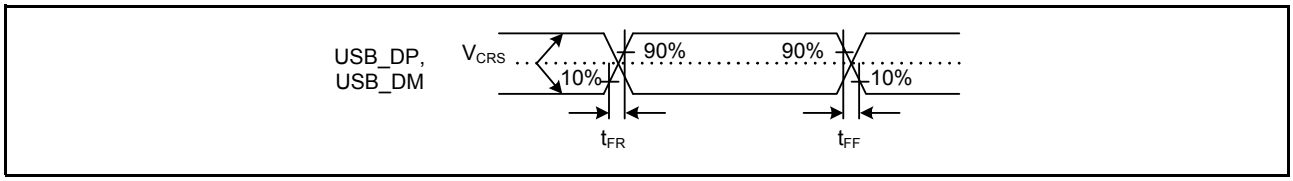



**Figure 2.85 USB_DP and USB_DM output timing in full-speed mode**

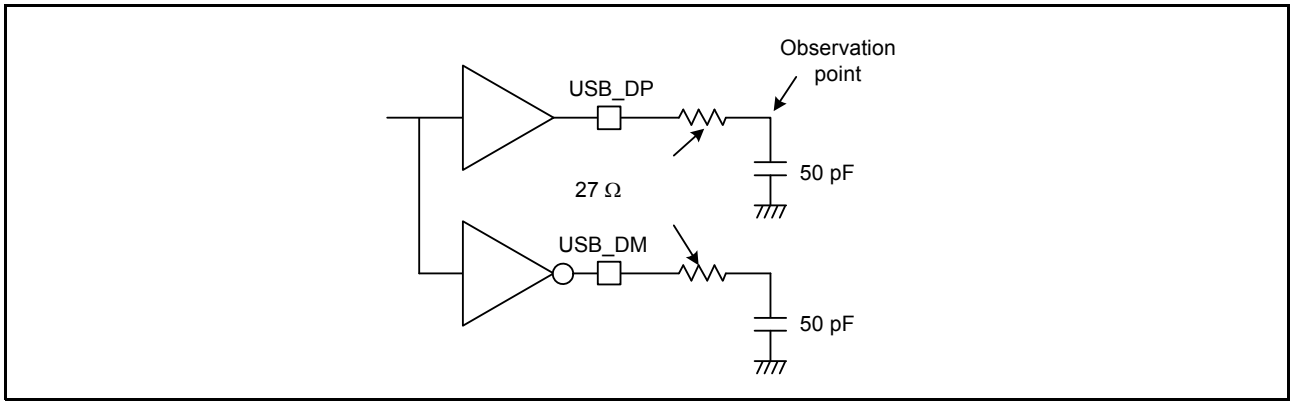



**Figure 2.86 Test circuit in full-speed mode**

## 2.5 ADC12 Characteristics

[Normal-precision channel]

**Table 2.40 A/D conversion characteristics for unit 0 (1/2)**
Conditions: PCLKC = 1 to 60 MHz

| Item | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Frequency | 1 | - | 60 | MHz | - |
| Analog input capacitance | - | - | 30 | pF | - |
| Quantization error | - | ±0.5 | - | LSB | - |
| Resolution | - | - | 12 | Bits | - |

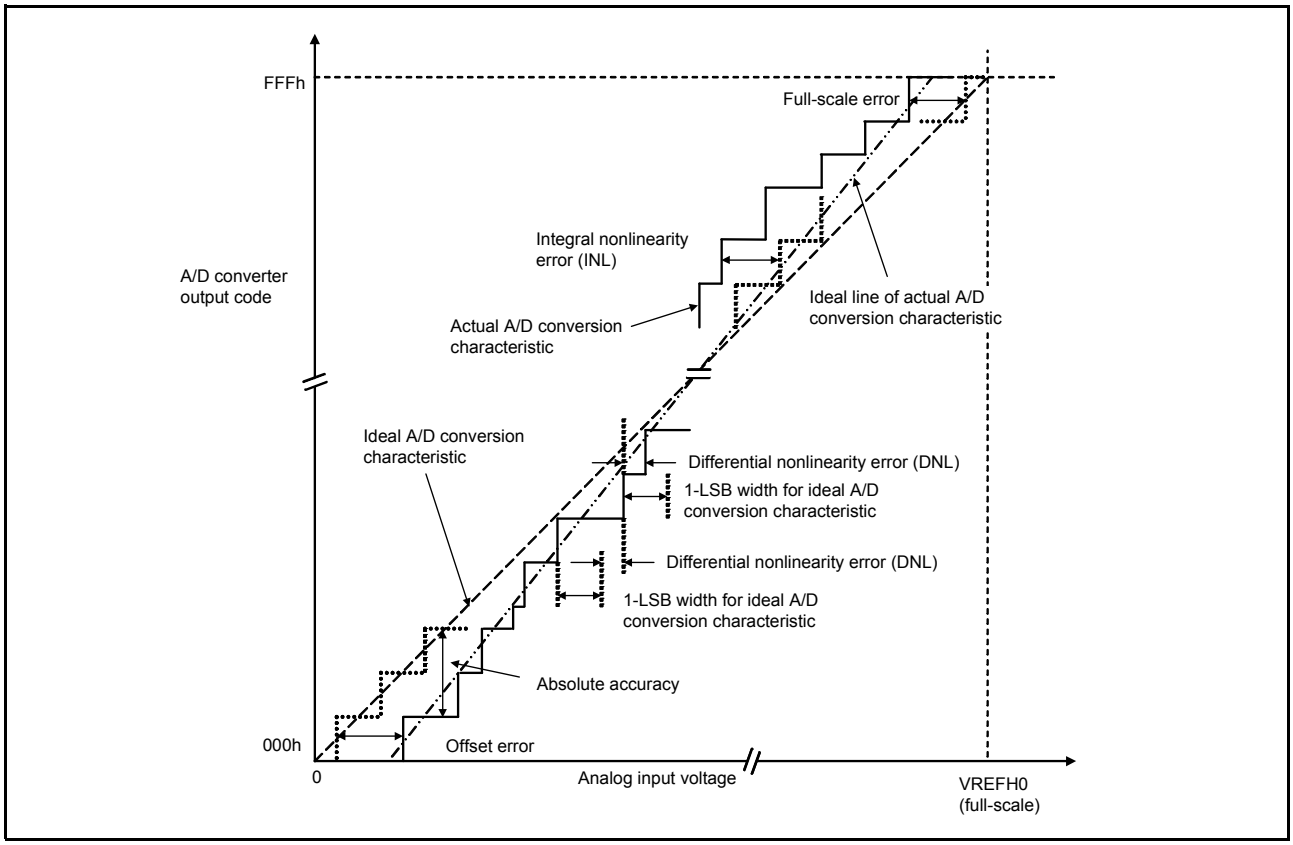



**Figure 2.87 Illustration of ADC12 characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

**Table 2.52 Code flash memory characteristics (2/2)**
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| Erasure time $N_{PEC}$ > 100 times | 8-KB | $t_{E8K}$ | - | 85 | 260 | - | 47 | 144 | ms |
| | 32-KB | $t_{E32K}$ | - | 304 | 1040 | - | 169 | 576 | ms |
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 1000*2 | - | - | 1000*2 | - | - | Times |
| Suspend delay during programming | | $t_{SPD}$ | - | - | 264 | - | - | 120 | µs |
| First suspend delay during erasure in suspend priority mode | | $t_{SESD1}$ | - | - | 216 | - | - | 120 | µs |
| Second suspend delay during erasure in suspend priority mode | | $t_{SESD2}$ | - | - | 1.7 | - | - | 1.7 | ms |
| Suspend delay during erasure in erasure priority mode | | $t_{SEED}$ | - | - | 1.7 | - | - | 1.7 | ms |
| Forced stop command | | $t_{FD}$ | - | - | 32 | - | - | 20 | µs |
| Data hold time*3 | | $t_{DRP}$ | 20 | - | - | 20 | - | - | Years |
| FCU reset time | | $t_{FCUR}$ | 35 | - | - | 35 | - | - | µs |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For example, when 256-byte programming is performed 32 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the characteristics when reprogramming is performed within the specified range, including the minimum value.

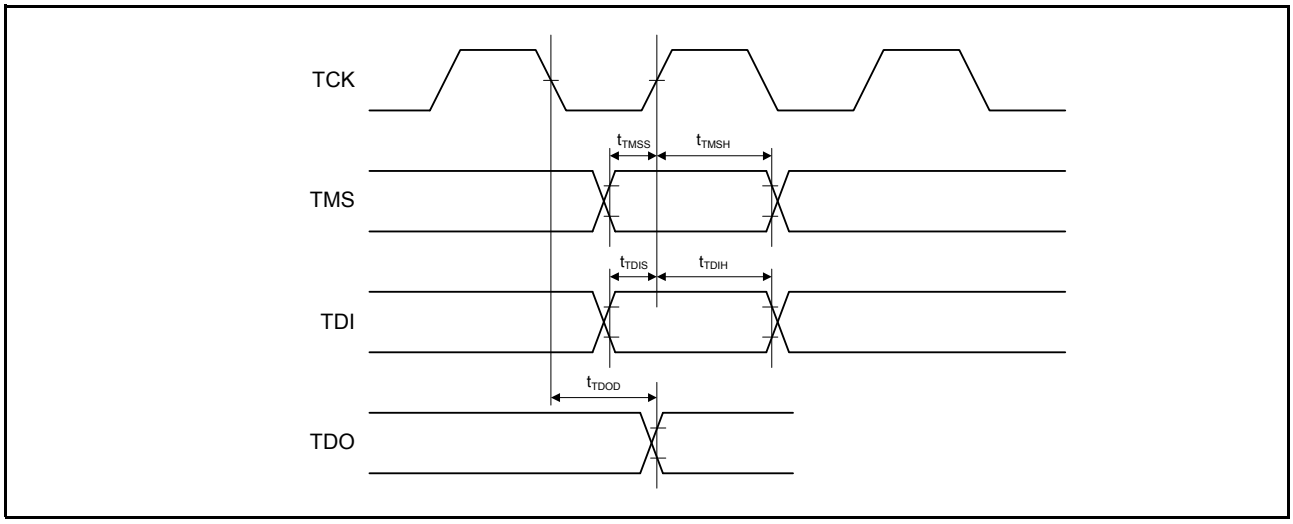



**Figure 2.96 Boundary scan input/output timing**

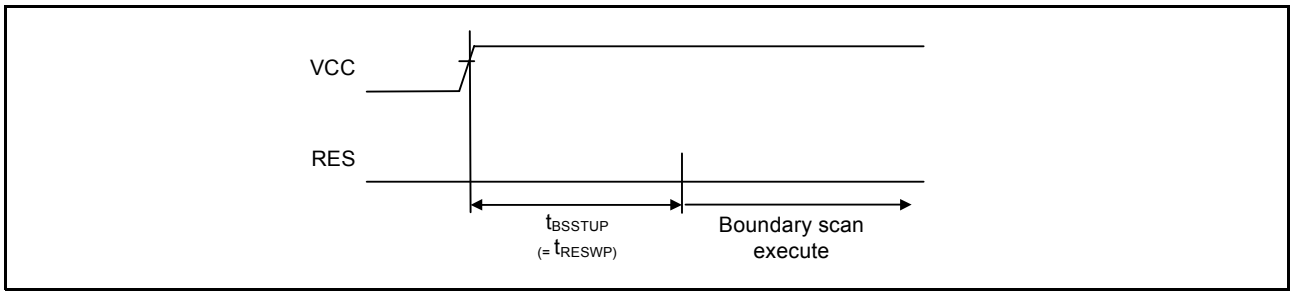



**Figure 2.97 Boundary scan circuit startup timing**

## 2.16 Joint European Test Action Group (JTAG)

**Table 2.55 JTAG**

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 40 | - | - | ns | Figure 2.95 |
| TCK clock high pulse width | $t_{TCKH}$ | 15 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 15 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 8 | - | - | ns | Figure 2.96 |
| TMS hold time | $t_{TMSH}$ | 8 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 8 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 8 | - | - | ns | |
| TDO data delay time | $t_{TDOD}$ | - | - | 28 | ns | |

| Revision History | S7G2 Datasheet |
|---|---|

| Rev. | Date | Chapter | Summary |
|---|---|---|---|
| 0.80 | Oct. 12, 2015 | — | First Edition issued |
| 0.85 | Dec. 15, 2015 | — | Second Edition issued |
| 1.00 | Feb. 23, 2016 | section 1, Overview | Updated VREFH and VREFL descriptions in Table 1.16, Pin functions |
| | | section 2, Electrical Characteristics | Updated operating and standby current information in section 2.2.5, Operating and Standby Current |
| | | | Added section 2.16, Joint European Test Action Group (JTAG) |
| | | | Added section 2.17, Serial Wire Debug (SWD) |
| | | | Added section 2.18, Embedded Trace Macro Interface (ETM) |
| | | | Updated Table 2.13, Clock timing except for sub-clock oscillator |
| | | | Updated SPI data in Table 2.25, SPI timing |
| | | | Updated Table 2.40, A/D conversion characteristics for unit 0 |
| | | | Updated Table 2.41, A/D conversion characteristics for unit 1 |
| | | | Updated SPI data in Figure 2.45, SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2 |
| | | | Updated Table 2.5, I/O IOH, IOL |
| | | All | Deleted # from pin names |