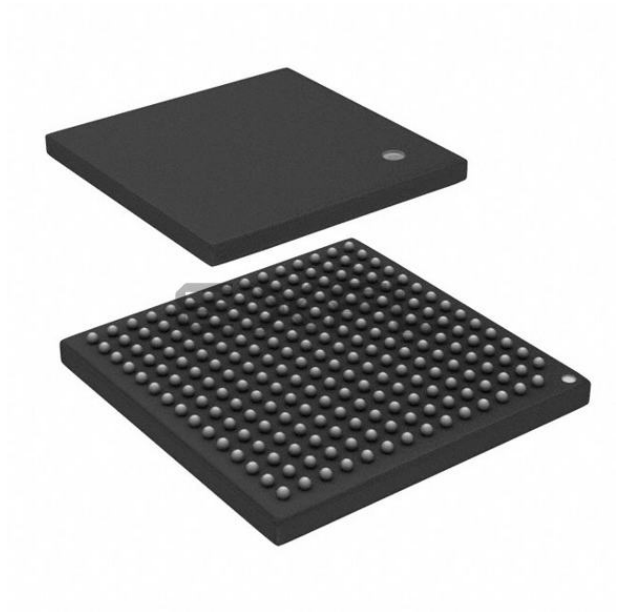
Renesas Electronics America Inc - R7FS7G27H2A01CBD#AC0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	172
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	224-LFBGA
Supplier Device Package	224-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27h2a01cbd-ac0

1. Overview

The S7G2 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 240 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 4 MB of code flash memory. See section 54, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 54, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or double-bit error detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 52, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 53, Standby SRAM in User's Manual.

Table 1.3 System (1/2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	VSS	USBHS_ DM	PVSS_ USBHS	P212 /EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_ DP	AVSS_ USBHS	P213 /XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_ USB	VSS_ USB	P408	P413	VCC_ USBHS	USBHS_ RREF	AVCC_ USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_ USBHS	VSS2_ USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	VCL1	VSS	P901	VSS								VSS	P006	P008	P005	10
9	VLO	VLO	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	VCC_ DCDC	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	VCL2	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK /SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL_F	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.4 Pin assignment for 176-pin BGA (top view)

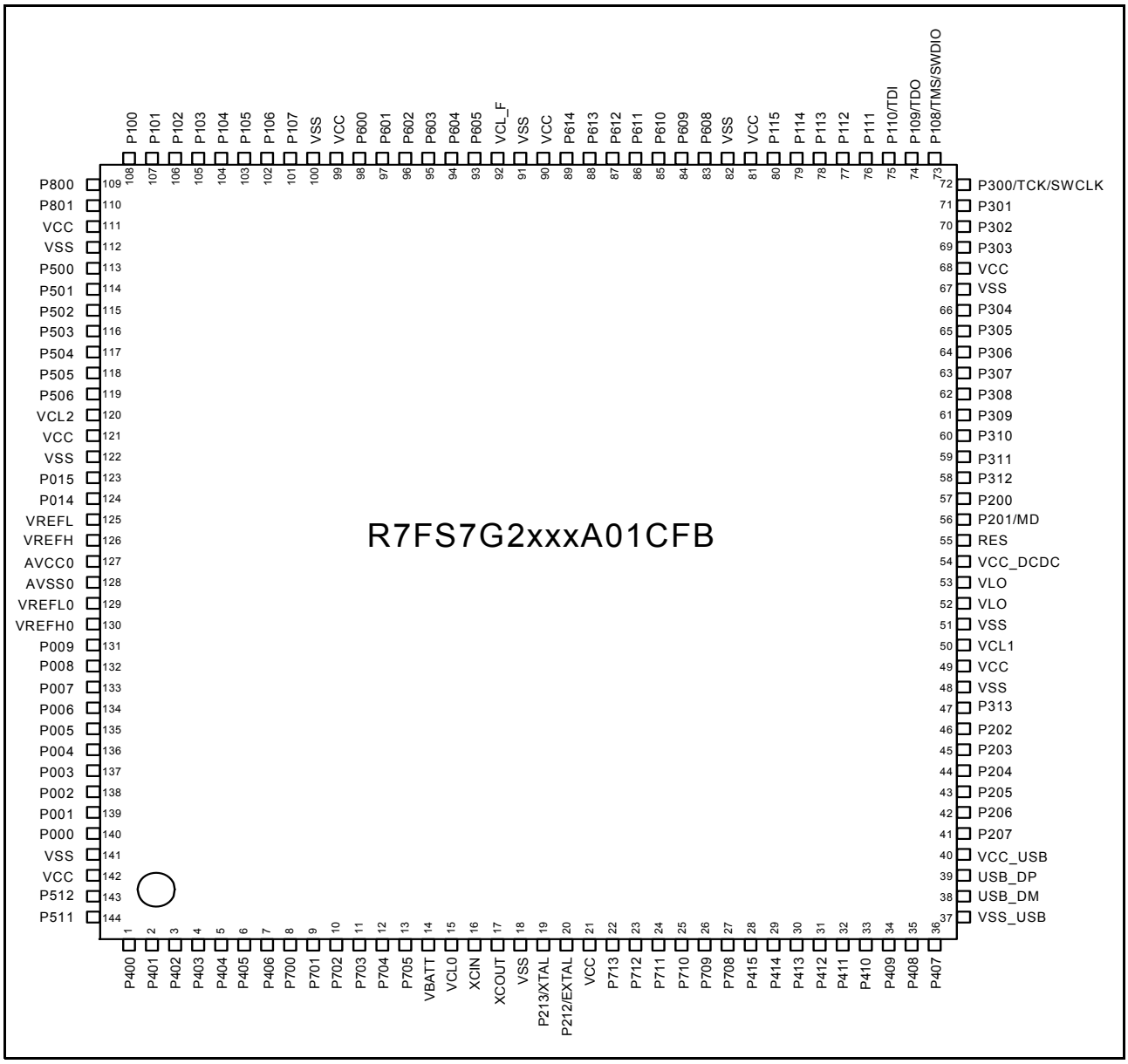


Figure 1.7 Pin assignment for 144-pin LQFP (top view)

Table 1.17 Pin list (11/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
P5	N5	143	K5	116	79	-	P503	-	-	-	GETRGC_B	GTIOC12B	-	USB_EXICEN_B	CTS6_RTS6_B/SS6_B	SCK5_A	-	QIO1	-	-	-	-	SD1DAT1	AN117	-	-		-
R5	P5	144	L5	117	80	-	P504	-	-	-	GETRGD_B	GTIOC13A	-	USB_ID_B	SCK6_B	CTS5_RTS5_A/SS5_A		QIO2	-	-	-	-	SD1DAT2	AN018	-	-		-
M5	P6	145	K6	118	-	-	P505	-	-	-	-	GTIOC13B	-	-	RXD6_B/MISO6_B/SCL6_B	-	-	QIO3	-	-	-	-	SD1DAT3	AN118	-	-	IRQ14	-
M6	R5	146	L6	119	-	-	P506	-	-	-	-	-	-	-	TXD6_B/MOSI6_B/SDA6_B	-	-	-	-	-	-	-	SD1CD	AN019	-	-	IRQ15	-
N6	N6	147	-	-	-	-	P507	-	-	-	-	-	-	-		CTS5_RTS5_B/SS5_B	-	-	-	-	-	-	SD1WP	AN119	-	-	-	-
M7	-	-	-	-	-	-	P508	-	-	-	-	-	-	-		SCK5_B	-	-	-	-	-	-	-	AN020	-	-	-	-
P6	-	-	-	-	-	-	P509	-	-	-	-	-	-	-		TXD5_B/MOSI5_B/SDA5_B	-	-	-	-	-	-	-	AN120	-	-	-	-
N7	-	-	-	-	-	-	P510	-	-	-	-	-	-	-	-	RXD5_B/MISO5_B/SCL5_B	-	-	-	-	-	-	-	AN021	-	-	-	-
R6	R6	148	N4	120	81	VCL2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R7	N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	P7	151	M6	123	84	-	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	IRQ13	-
M9	R7	152	N6	124	85	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-	-
N8	P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P8	N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. When the following ports are configured for high driving ability, they shift to middle driving ability during Deep Software Standby mode: P203 to P207, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01.
Note 4. Except for P000 to P007, P200, which are input ports.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1	V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
		V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*2	V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
		V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
		V_{OL}	-	-	0.4		I_{OL} = 1.0 mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, P813, PA12 to PA15, PB01 (total 24 pins)*3	V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
		V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
		V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES	$\|I_{in}\|$	-	-	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P007, P200		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports	$\|I_{TSI}\|$	-	-	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB (except for ports P000 to P007)	I_p	–300	-	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015,P400, P415, P401, P511, P512	C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	Other input pins		-	-	8		

Note 1. SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B, SCL2, SDA2 (total 8 pins).
Note 2. SCL0_A, SDA0_A (total 2 pins).
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. Even when high driving ability is selected, I_{OH} and I_{OL} shift to middle driving ability during Deep Software Standby mode.

Table 2.7 Operating and standby current (2/2)

Item			Symbol	LDO mode			DCDC mode			Unit	Test conditions
				Min	Typ	Max	Min	Typ	Max		
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)		AI_{REFH}	-	70	120	-	70	120	µA	-
	During D/A conversion (per unit)	Without AMP output		-	0.24	0.4	-	0.24	0.4	mA	-
		With AMP ouput		-	0.1	0.2	-	0.1	0.2	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion			-	0.07	0.4	-	0.07	0.4	µA	-
	ADC12 unit 1 in standby modes			-	0.07	0.2	-	0.07	0.2	µA	-
USB operating current	Low speed	USB	$I_{CCUSBLS}$	-	3.5	6.5	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	Full speed	USB	$I_{CCUSBFS}$	-	4.0	10.0	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	High speed	USBHS	$I_{CCUSBHS}$	-	50	65	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	Standby mode (direct power down)	USBHS	$I_{CCUSBSBY}$	-	0.5	3.0	-	0.5	3.0	µA	VCC_USBHS = AVCC_USBHS

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. This does not include the BGO operation.
Note 4. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 5. When V_{BATT} is used.
Note 6. When using ETHERC, PCLKA frequency is:
12.5MHz ≤ PCLKA ≤ 120MHz
Note 7. When VCC is < VDETBATT and > (VBATT + 0.6 V), the injected current connects from the VCC to the VBATT pin through an internal diode.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.8 Rise and fall gradient characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	SrVCC	0.0084	-	20	ms/V	-
VCC falling gradient*1	SfVCC	0.0084	-	-	ms/V	-

Note 1. This applies when VBATT is used.

Table 2.9 Rise and fall gradient and ripple frequency characteristics
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	-	-	10	kHz	Figure 2.2 $V_{r\ (VCC)}$ ≤ VCC × 0.2
		-	-	1	MHz	Figure 2.2 $V_{r\ (VCC)}$ ≤ VCC × 0.08
		-	-	10	MHz	Figure 2.2 $V_{r\ (VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

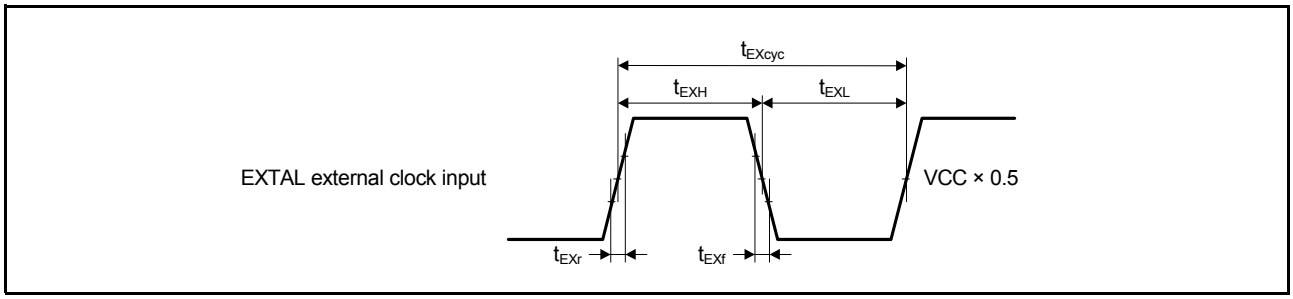


Figure 2.4 EXTAL external clock input timing

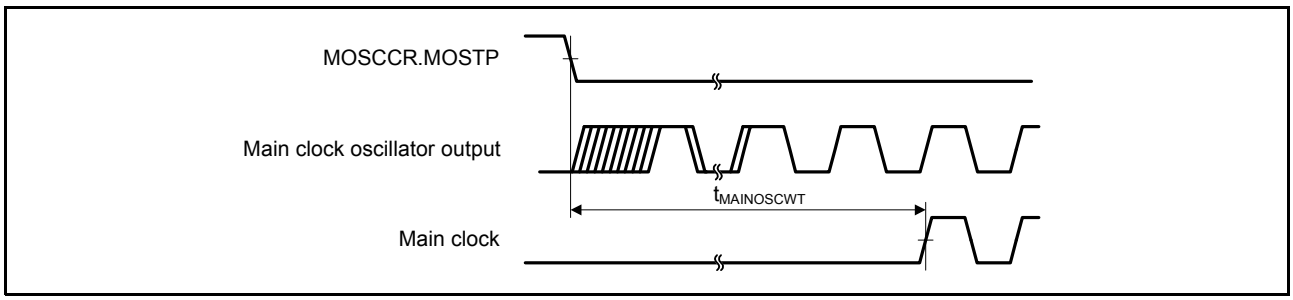


Figure 2.5 Main clock oscillation start timing

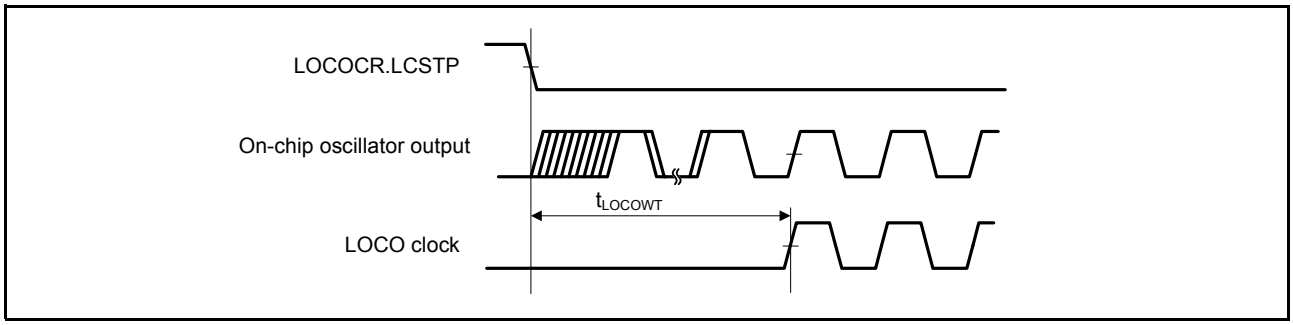


Figure 2.6 LOCO clock oscillation start timing

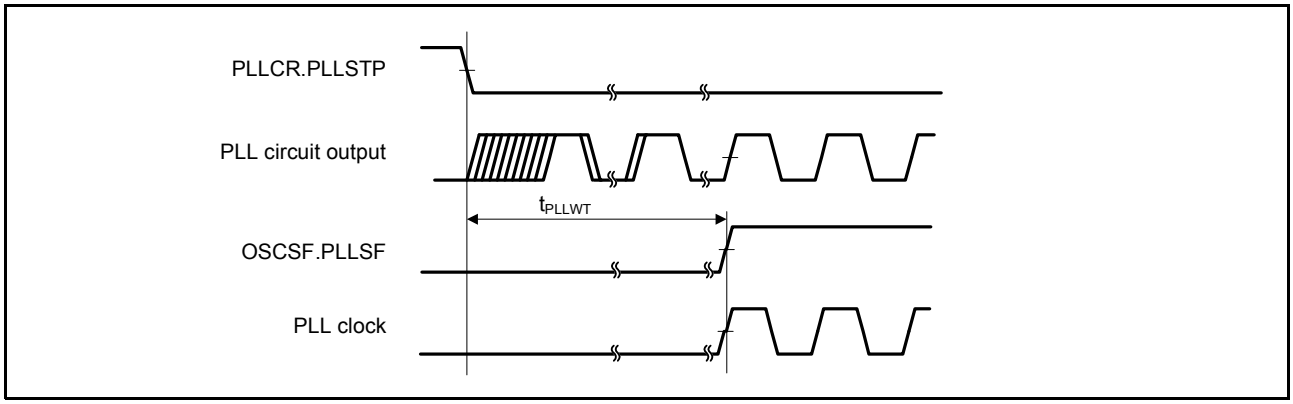


Figure 2.7 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

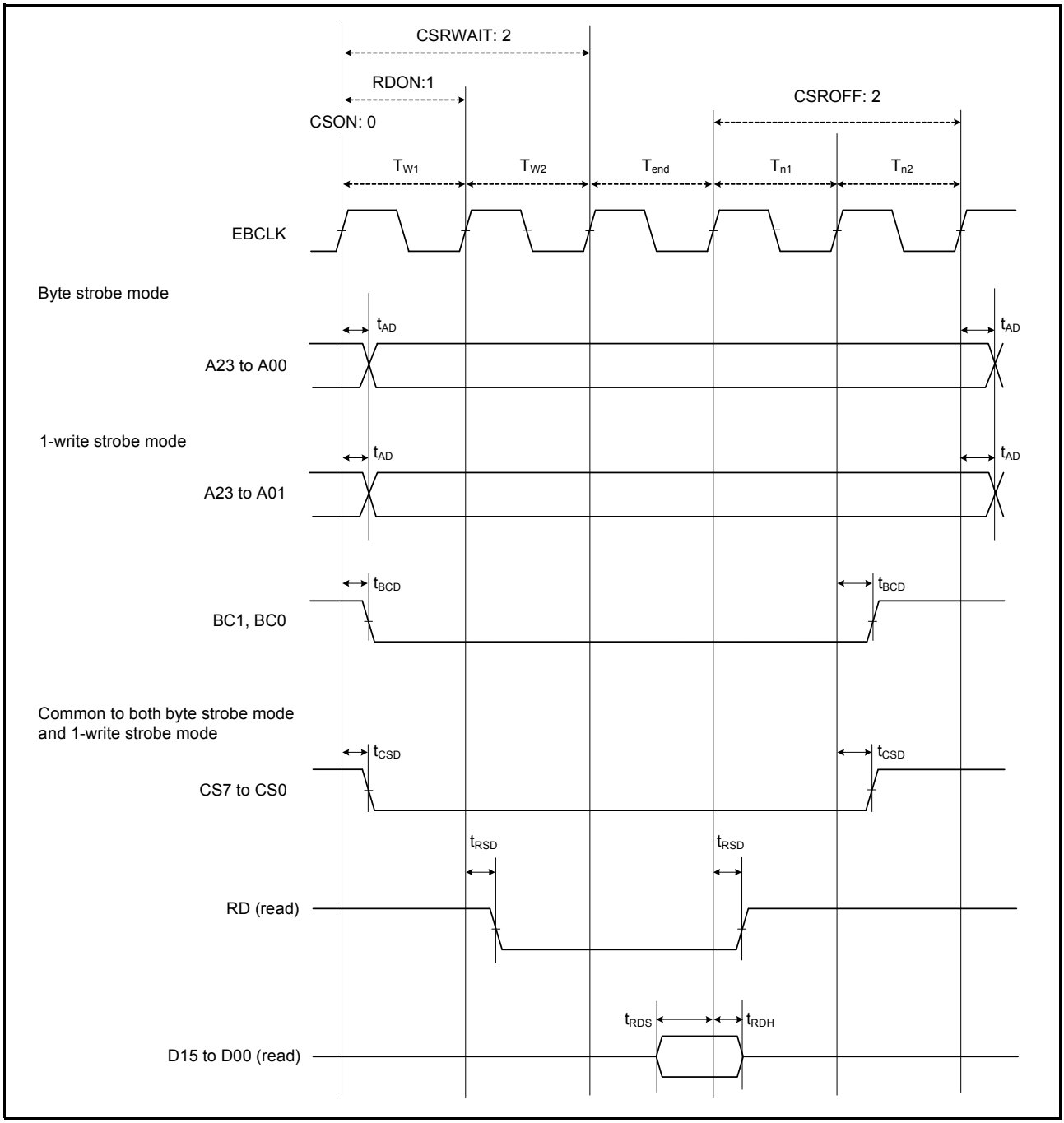


Figure 2.14 External bus timing for normal read cycle with bus clock synchronized

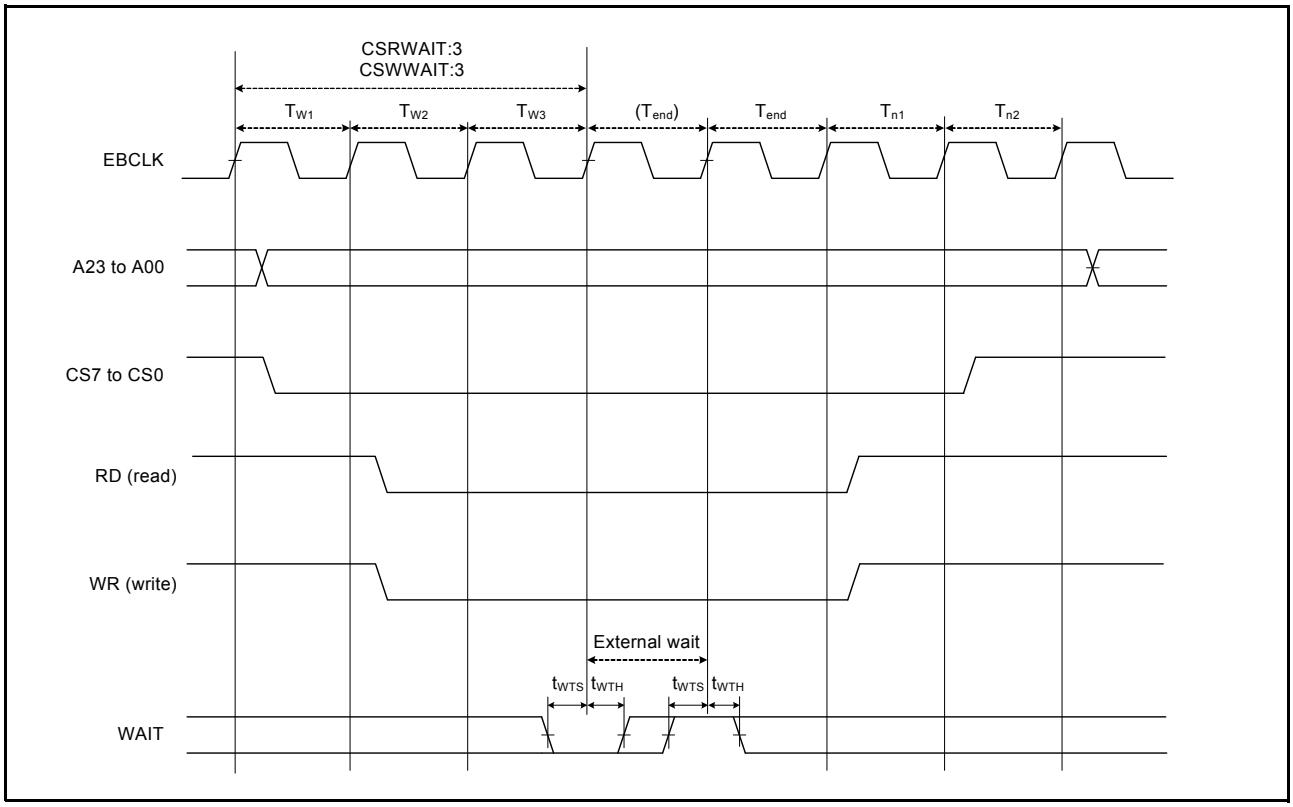
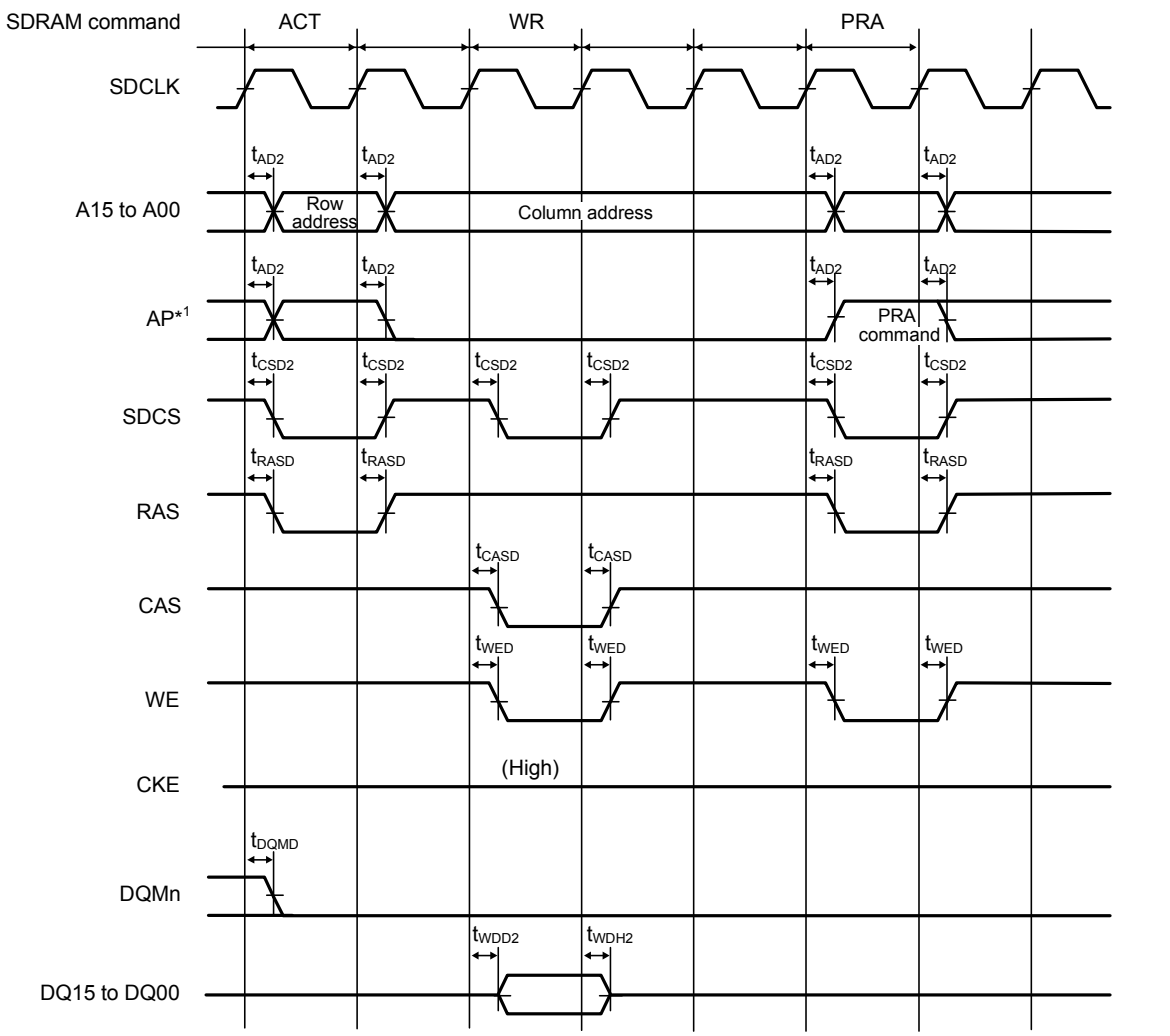
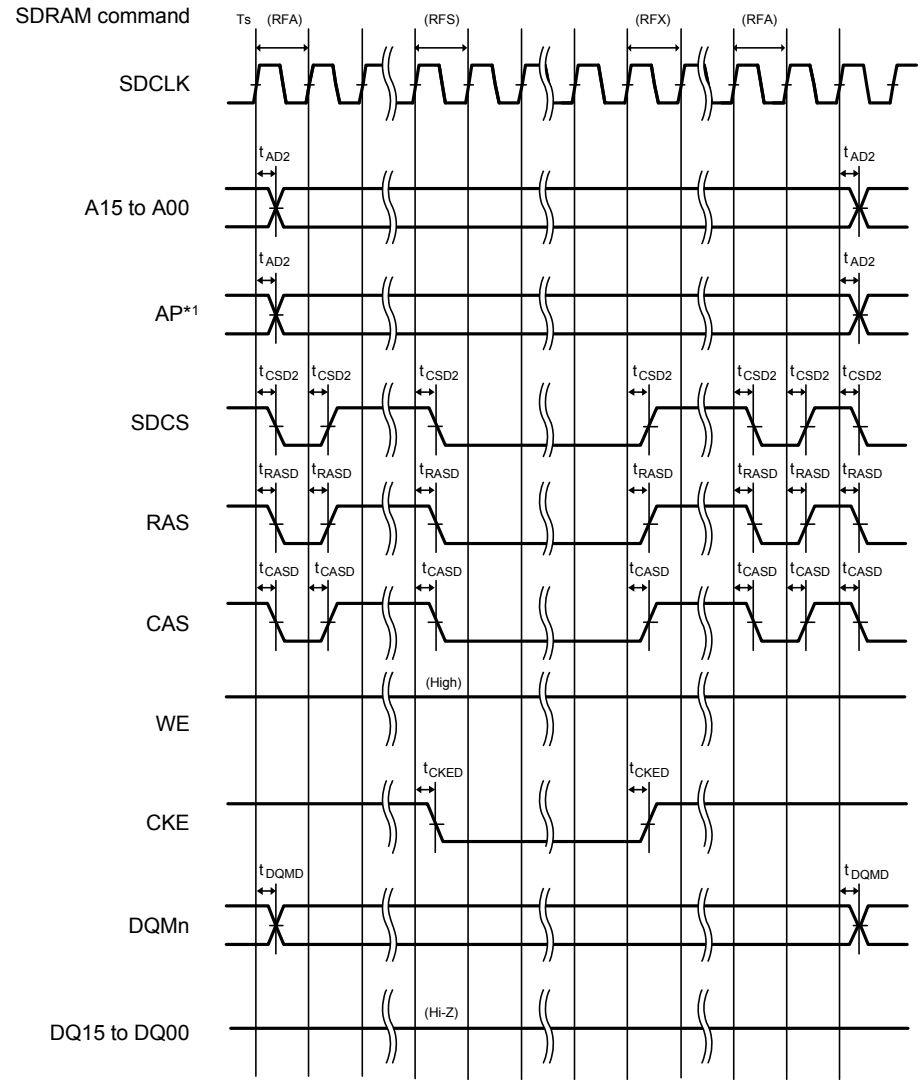


Figure 2.18 External bus timing for external wait control



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.20 SDRAM single write timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.25 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1/2)

GPT32 Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: GTIOC6A_A, GTIOC6B_A, GTIOC3A_B, GTIOC3B_B, GTIOC0A_B, GTIOC0B_B, GTIOC9A_B, GTIOC9B_B.
High drive output is selected in the port drive capability bit in the PmnPFS register for all other pins.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.26
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.27

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2/2)

GPT32 Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: GTIOC6A_A, GTIOC6B_A, GTIOC3A_B, GTIOC3B_B, GTIOC0A_B, GTIOC0B_B, GTIOC9A_B, GTIOC9B_B.
High drive output is selected in the port drive capability bit in the PmnPFS register for all other pins.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.28
		Dual edge		2.5	-		
	GTIOCxY_Z output skew (x = 0 to 7, Y= A or B , Z = A or B)	Middle drive buffer	t_{GTISK}*2	-	4	ns	Figure 2.29
		High drive buffer		-	4		
	GTIOCxY_Z output skew (x = 8 to 13, Y = A or B, Z = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY_Z output skew (x = 0 to 13, Y = A or B, Z = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP_x, GTOULO_x, GTOVUP_x, GTOVLO_x, GTOWUP_x, GTOWLO_x (x = A or B)		t_{GTOSK} *2	-	5	ns	Figure 2.30
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*3	-	2.0	ns	Figure 2.31
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*1	100	-	ns	Figure 2.32
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.33
KINT	Key interrupt input low width		t_{KR}	250	-	ns	Figure 2.34

Note 1. t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 3. The load is 30 pF.
Note 4. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

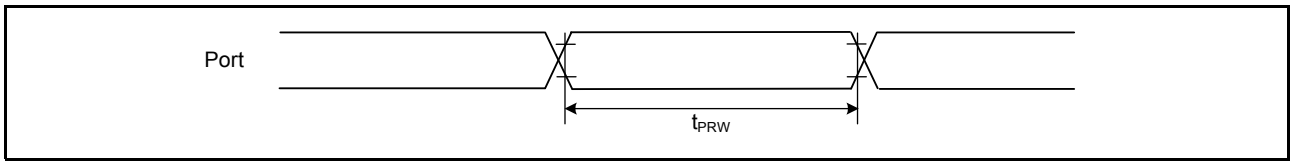


Figure 2.26 I/O ports input timing

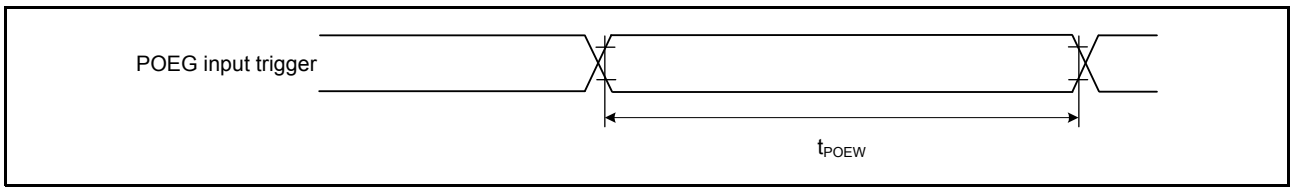


Figure 2.27 POEG input trigger timing

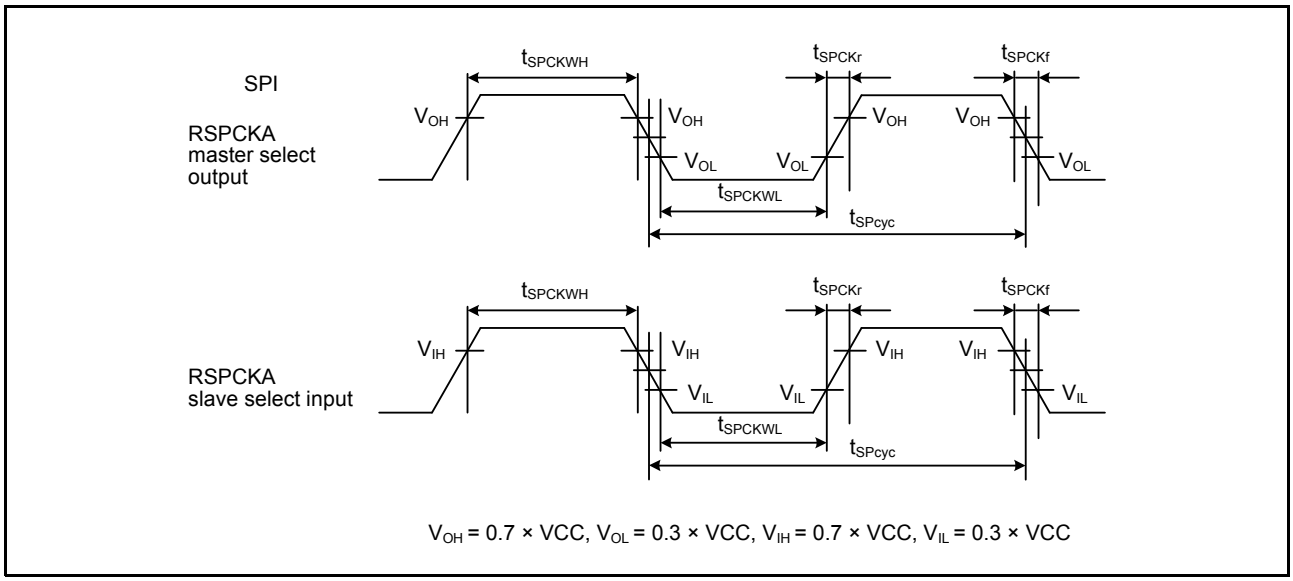


Figure 2.43 SPI clock timing

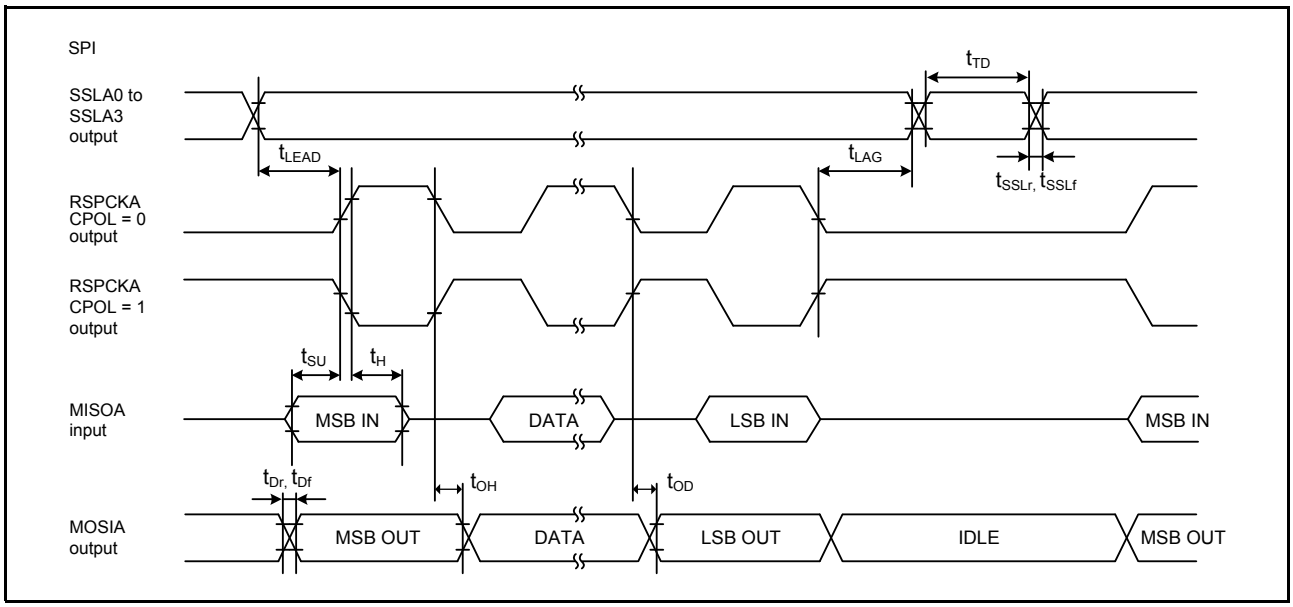


Figure 2.44 SPI timing for master when CPHA = 0

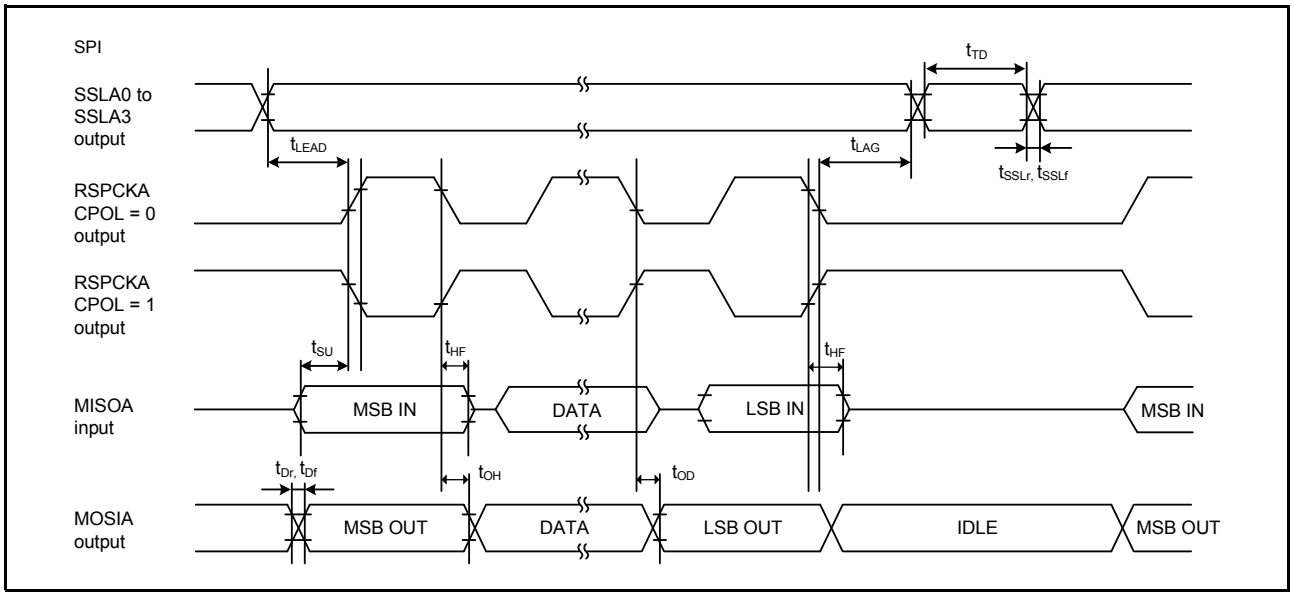


Figure 2.45 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

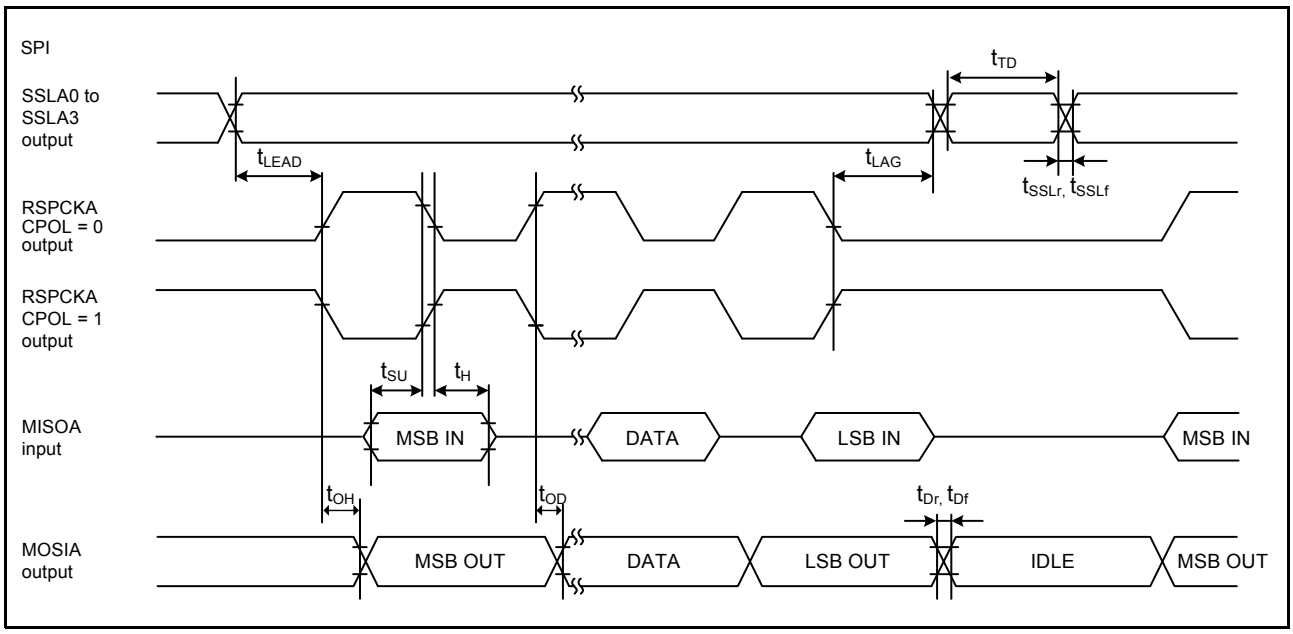
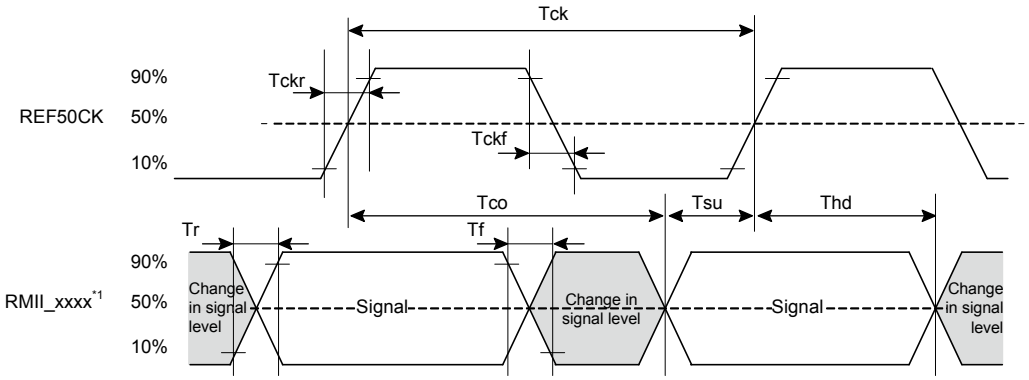


Figure 2.46 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

Table 2.27 IIC timing (1) (2/2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

Item		Symbol	Min*1, *2	Max	Unit	Test conditions
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 2.58 REF50CK and RMII signal timing

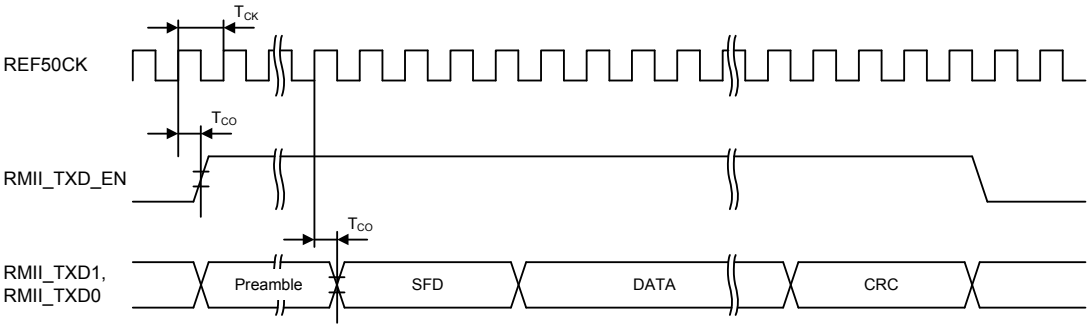


Figure 2.59 RMII transmission timing

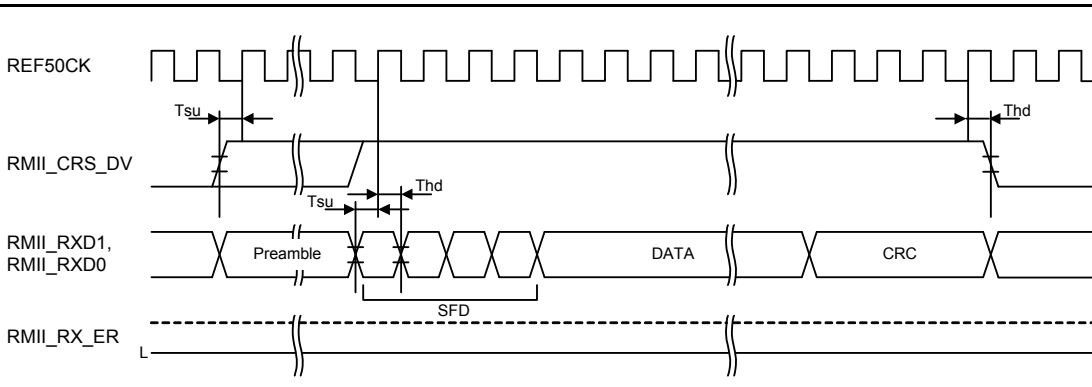


Figure 2.60 RMII reception timing in normal operation

2.3.17 PDC Timing

Table 2.32 PDC timing
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item		Symbol	Min	Max	Unit	Test conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 2.68
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 2.69
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	-	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 2.70
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

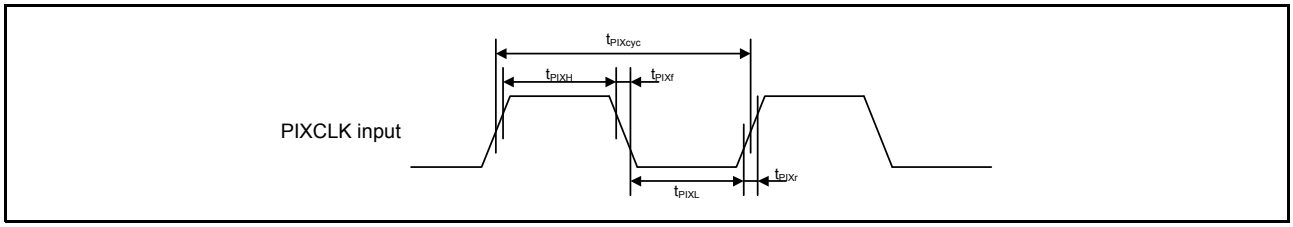


Figure 2.68 PDC input clock timing

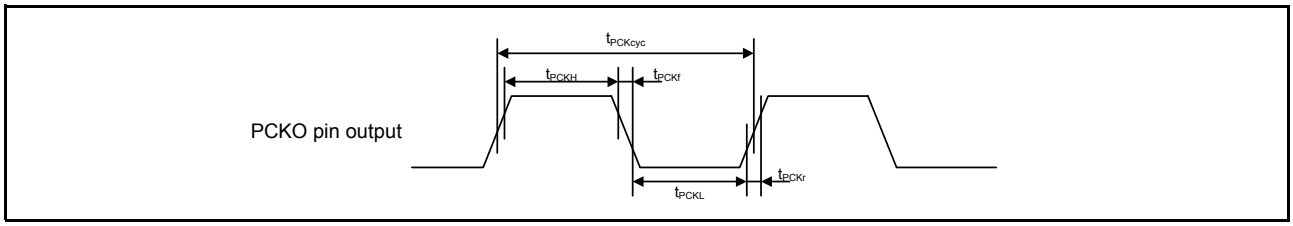


Figure 2.69 PDC output clock timing

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.83
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

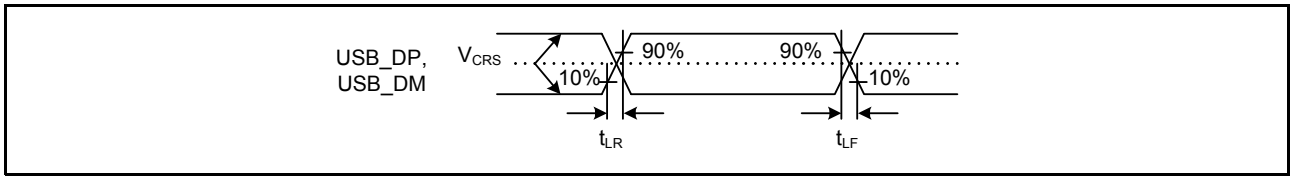


Figure 2.83 USB_DP and USB_DM output timing in low-speed mode

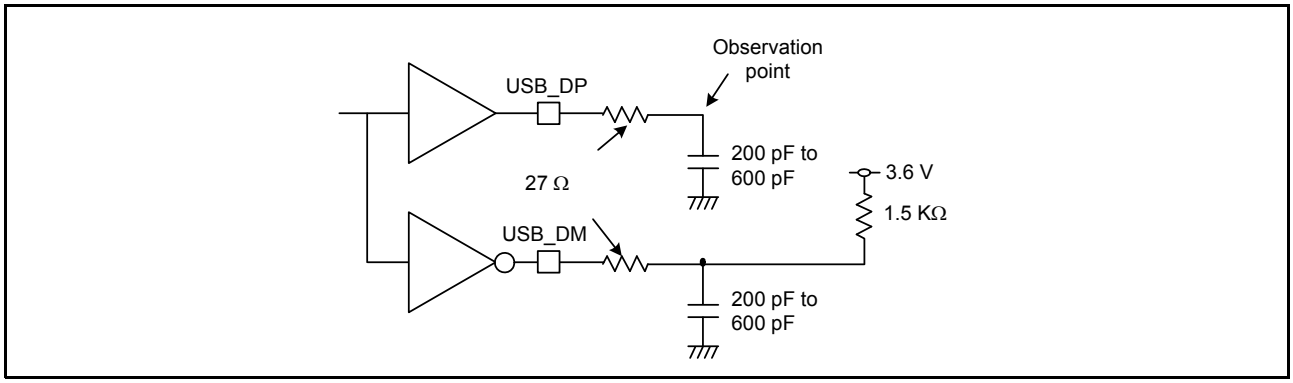


Figure 2.84 Test circuit in low-speed mode

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (1/2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-

Table 2.40 A/D conversion characteristics for unit 0 (2/2)
Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH 0 –0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN003 to AN006)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 300Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN021)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 2.41 A/D conversion characteristics for unit 1 (1/2)
Conditions: PCLKC = 1 to 60 MHz

Item	Min	Typ	Max	Unit	Test conditions
Frequency	1	-	60	MHz	-
Analog input capacitance	-	-	30	pF	-

Revision History	S7G2 Datasheet

Rev.	Date	Chapter	Summary
0.80	Oct. 12, 2015	—	First Edition issued
0.85	Dec. 15, 2015	—	Second Edition issued
1.00	Feb. 23, 2016	section 1, Overview	Updated VREFH and VREFL descriptions in Table 1.16, Pin functions
		section 2, Electrical Characteristics	Updated operating and standby current information in section 2.2.5, Operating and Standby Current
			Added section 2.16, Joint European Test Action Group (JTAG)
			Added section 2.17, Serial Wire Debug (SWD)
			Added section 2.18, Embedded Trace Macro Interface (ETM)
			Updated Table 2.13, Clock timing except for sub-clock oscillator
			Updated SPI data in Table 2.25, SPI timing
			Updated Table 2.40, A/D conversion characteristics for unit 0
			Updated Table 2.41, A/D conversion characteristics for unit 1
			Updated SPI data in Figure 2.45, SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2
			Updated Table 2.5, I/O IOH, IOL
		All	Deleted # from pin names