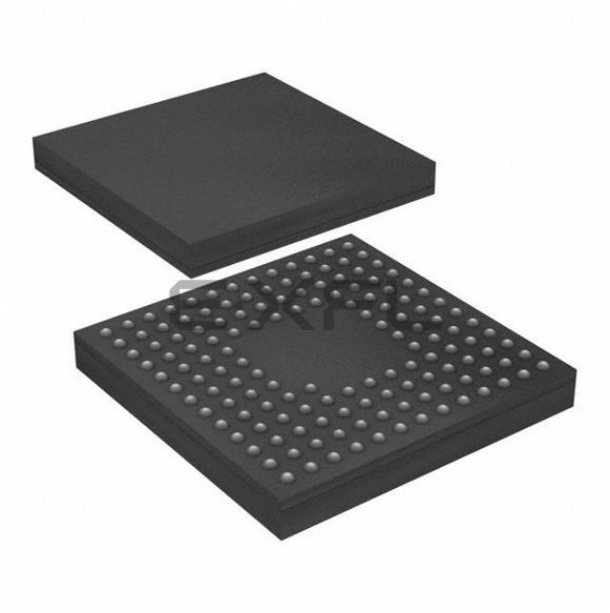
Renesas Electronics America Inc - R7FS7G27H2A01CLK#AC0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27h2a01clk-ac0

1. Overview

The S7G2 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 240 MHz with the following features:

- Up to 4-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 240 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 4 MB of code flash memory. See section 54, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 54, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or double-bit error detection (DED). The first 32 KB of SRAM0 is subject to DED. Parity check is performed for other areas. See section 52, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 53, Standby SRAM in User's Manual.

Table 1.3 System (1/2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.9 Communication interfaces (2/2)

Feature	Functional description
Ethernet MAC with IEEE 1588 PTP (ETHERC)	Two-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. Each ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: • Synchronization Frame Processing units (SYNFP0 and SYNFP1) • A Packet Relation Controller unit (PRC-TC) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface provide the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-, 4-, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.10 Analog

Feature	Functional description
12-Bit A/D Converter (ADC12)	Up to two successive approximation 12-Bit A/D Converters are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 12 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 46, 12-Bit A/D Converter (ADC12) in User's Manual.
12-Bit D/A Converter (DAC12)	The DAC12 D/A converts data and includes an output amplifier. See section 47, 12-Bit D/A Converter (DAC12) in User's Manual.
Temperature sensor (TSN)	The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 48, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	Analog comparators can be used to compare a test voltage with a reference voltage and to provide a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 49, High-Speed Analog Comparator (ACMPHS) in User's Manual.

Table 1.11 Human machine interfaces (1/2)

Feature	Functional description
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.

Table 1.13 Data processing (2/2)

Feature	Functional description
Sampling Rate Converter (SRC)	The SRC converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. The sampling rate of the input signal can be one of the following: • 8 kHz • 11.025 kHz • 12 kHz • 16 kHz • 22.05 kHz • 24 kHz • 32 kHz • 44.1 kHz • 48 kHz. The sampling rate of the output signal can be one of the following: • 8 kHz • 16 kHz • 32 kHz • 44.1 kHz • 48 kHz. Independent FIFOs are provided for input and output. In a typical application, a DMA controller can be used to transfer PCM audio data from SRAM, for example, to the SRC. Sample-converted audio data from the SRC can then be transferred using the DMA Controller to the SSI, from where it can be transmitted to an external audio codec. See section 42, Sampling Rate Converter (SRC) in User's Manual.

Table 1.14 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and DLP. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH - 128-bit unique ID.

Table 1.16 Pin functions (4/5)

Function	Signal	I/O	Description
ETHERC	REF50CK0, REF50CK1	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timing in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	Indicate carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode.
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode.
	RMII0_TXD_EN, RMII1_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode.
	RMII0_RX_ER, RMII1_RX_ER	Input	Indicate an error occurred during reception of data in RMII mode.
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable signals.
	ET0_RX_DV, ET1_RX_DV	Input	Indicate valid receive data on ET_ERXD3 to ET_ERXD0.
	ET0_EXOUT, ET1_EXOUT	Input	General-purpose external output pins.
	ET0_LINKSTA, ET1_LINKSTA	Output	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3, ET1_ETXD0 to ET1_ETXD3	output	4 bits of MII transmit data.
	ET0_ERXD0 to ET0_ERXD3, ET1_ERXD0 to ET1_ERXD3	Input	4 bits of MII receive data.
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable signals. Function as signals indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. Function as signals notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. Function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	Input	Transmit clock pins. These pins input reference signals for output timing from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins. These pins input reference signals for input timing to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	ET0_WOL, ET1_WOL	Output	Receive Magic packets.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer through ET_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management data with PHY-LSI.
SDHI	SD0CLK, SD1CLK	Output	SD clock output pin.
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pin.
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins.
	SD0CD, SD1CD	Input	SD card detection pin.
	SD0WP, SD1WP	Input	SD write-protect signal.

R7FS7G2xxxA01CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	VCL1	VSS	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	VLO	VLO	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	VCC_ DCDC	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	VCL2	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL_F	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.6 Pin assignment for 145-pin LGA (top view)

Table 1.17 Pin list (4/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
D14	C15	40	D11	32	21	-	P411	-	-	AGTOA1	GTOVUP_B	GTIOC9A_A	-	-	TXD0_B/MOSI0_B/SDA0_B	CTS3_RTS3_A/SS3_A	-	MOSIA_B	-	ET0_ERXD1	RMII0_RXD0	-	SD0DAT0	-	-	TS07	IRQ4	-
C15	C14	41	C12	33	22	-	P410	-	-	AGTOB1	GTOVLO_B	GTIOC9B_A	-	-	RXD0_B/MISO0_B/SCL0_B	SCK3_A	-	MISOA_B	-	ET0_ERXD0	RMII0_RXD1	-	SD0DAT1	-	-	TS06	IRQ5	-
C14	B15	42	B13	34	23	-	P409	-	-	-	GTOWUP_B	GTIOC10A_A	-	USB_EXICEN_A	-	TXD3_A/MOSI3_A/SDA3_A	-	-	-	ET0_RX_CLK	RMII0_RX_ER	USBHS_EXICEN	-	-	-	TS05	IRQ6	-
B15	D13	43	D10	35	24	-	P408	-	-	-	GTOWLO_B	GTIOC10B_A	-	USB_ID_A	-	RXD3_A/MISO3_A/SCL3_A	-	-	-	ET0_CRS	RMII0_CRS_DV	USBHS_ID	-	-	-	TS04	IRQ7	-
A15	A15	44	A13	36	25	-	P407	-	-	-	-	-	RTCOUT	USB_VBUS	CTS4_RTS4_A/SS4_A	-	SDA0_B	SSLB3_A	-	ET0_EXOUT	ET0_EXOUT	-	-	ADTRG0	-	TS03	-	-
B13	C13	45	B11	37	26	VSS_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	B14	46	A12	38	27		-	-	-	-	-	-	-	USB_DM	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	A14	47	B12	39	28		-	-	-	-	-	-	-	USB_DP	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A13	B13	48	A11	40	29	VCC_USB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C13	C12	49	C11	41	30	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2_A	-	-	-	-	-	-	-	TS02	-	-
G9	D12	50	B10	42	31	-	P206	WAIT	-	-	GTIU_A	-	-	USB_VBUSEN_A	RXD4_A/MISO4_A/SCL4_A	-	SDA1_A	SSLB1_A	SSIDATA1_A	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT2	-	-	TS01	IRQ0-DS	-
C12	E12	51	A10	43	32	CLKOUT_A	P205	A16	-	AGTO1	GTIV_A	GTIOC4A_B	-	USB_OVRCURA_A-DS	TXD4_A/MOSI4_A/SDA4_A	CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A	SSIWS1_A	ET0_WOL	ET0_WOL	-	SD0DAT3	-	-	TSCAP_A	IRQ1-DS	-
D11	A13	52	C10	44	-	CACREF_A	P204	A18	-	AGTIO1_A	GTIW_A	GTIOC4B_B	-	USB_OVRCURB_A-DS	SCK4_A	SCK9_A	SCL0_B	RSPCKB_A	SSISCK1_A	ET0_RX_DV	-	-	SD0DAT4	-	-	TS00	-	-
B12	D11	53	A9	45	-	-	P203	A19	-	-	-	GTIOC5A_A	-	CTX0_A	CTS2_RTS2_A/SS2_A	TXD9_A/MOSI9_A/SDA9_A	-	MOSIB_A	-	ET0_COL	-	-	SD0DAT5	-	-	TSCAP_B	IRQ2-DS	-

Table 1.17 Pin list (9/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
J5	-	-	-	-	-		PA03	-	-	-	-	-	-	-	-	RXD7_B/MISO7_B/SCL7_B	-	-	-	-	-	-	-	-	-	-	IRQ9	-
H6	-	-	-	-	-		PA02	-	-	-	-	-	-	-	-	TXD7_B/MOSI7_B/SDA7_B	-	-	-	-	-	-	-	-	-	-	IRQ10	-
J6	H2	113	-	-	-		PA01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_B
J7	H4	114	-	-	-		PA00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_B
K5	J4	115	-	-	-		P607	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_B
K6	J1	116	-	-	-		P606	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_B
K1	J2	117	H2	93	-		P605	D11	DQ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K2	J3	118	G4	94	-		P604	D12	DQ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	K3	119	H3	95	-		P603	D13	DQ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L1	K1	120	J1	96	65		P602	EBCLK	SDCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_A
L2	K2	121	J2	97	66	-	P601	WR/WR0	DQM0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_A
L3	L1	122	H4	98	67	-	P600	RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA02_A
M2	K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M1	L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K4	L2	125	J3	101	68	-	P107	D07	DQ07	-	-	GTIOC8A_A	-	-	CTS8_RTS8_A/SS8_A	-	-	-	-	-	-	-	-	-	-	-	KR07	LCD_DATA01_A
L4	M1	126	K3	102	69	-	P106	D06	DQ06	-	-	GTIOC8B_A	-	-	SCK8_A	-	-	SSLA3_A	-	-	-	-	-	-	-	-	KR06	LCD_DATA00_A
M3	L3	127	J4	103	70	-	P105	D05	DQ05	-	GETRGA_C	-	-	-	TXD8_A/MOSI8_A/SDA8_A	-	-	SSLA2_A	-	-	-	-	-	-	-	-	IRQ0/KR05	LCD_TCON3_A
N3	M2	128	L3	104	71	-	P104	D04	DQ04	-	GETRGB_B	-	-	-	RXD8_A/MISO8_A/SCL8_A	-	-	SSLA1_A	-	-	-	-	-	-	-	-	IRQ1/KR04	LCD_TCON2_A

Table 1.17 Pin list (11/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
P5	N5	143	K5	116	79	-	P503	-	-	-	GETRGC_B	GTIOC12B	-	USB_EXICEN_B	CTS6_RTS6_B/SS6_B	SCK5_A	-	QIO1	-	-	-	-	SD1DAT1	AN117	-	-		-
R5	P5	144	L5	117	80	-	P504	-	-	-	GETRGD_B	GTIOC13A	-	USB_ID_B	SCK6_B	CTS5_RTS5_A/SS5_A		QIO2	-	-	-	-	SD1DAT2	AN018	-	-		-
M5	P6	145	K6	118	-	-	P505	-	-	-	-	GTIOC13B	-	-	RXD6_B/MISO6_B/SCL6_B	-	-	QIO3	-	-	-	-	SD1DAT3	AN118	-	-	IRQ14	-
M6	R5	146	L6	119	-	-	P506	-	-	-	-	-	-	-	TXD6_B/MOSI6_B/SDA6_B	-	-	-	-	-	-	-	SD1CD	AN019	-	-	IRQ15	-
N6	N6	147	-	-	-	-	P507	-	-	-	-	-	-	-		CTS5_RTS5_B/SS5_B	-	-	-	-	-	-	-	SD1WP	AN119	-	-	-	-
M7	-	-	-	-	-	-	P508	-	-	-	-	-	-	-		SCK5_B	-	-	-	-	-	-	-	-	AN020	-	-	-	-
P6	-	-	-	-	-	-	P509	-	-	-	-	-	-	-		TXD5_B/MOSI5_B/SDA5_B	-	-	-	-	-	-	-	-	AN120	-	-	-	-
N7	-	-	-	-	-	-	P510	-	-	-	-	-	-	-	-	RXD5_B/MISO5_B/SCL5_B	-	-	-	-	-	-	-	-	AN021	-	-	-	-
R6	R6	148	N4	120	81	VCL2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R7	N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	P7	151	M6	123	84	-	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/AN106	DA1/IVCMP1	-	IRQ13	-
M9	R7	152	N6	124	85	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/AN105	DA0/IVREF3	-	-	-
N8	P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P8	N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr

Figure 2.1 shows the timing conditions.

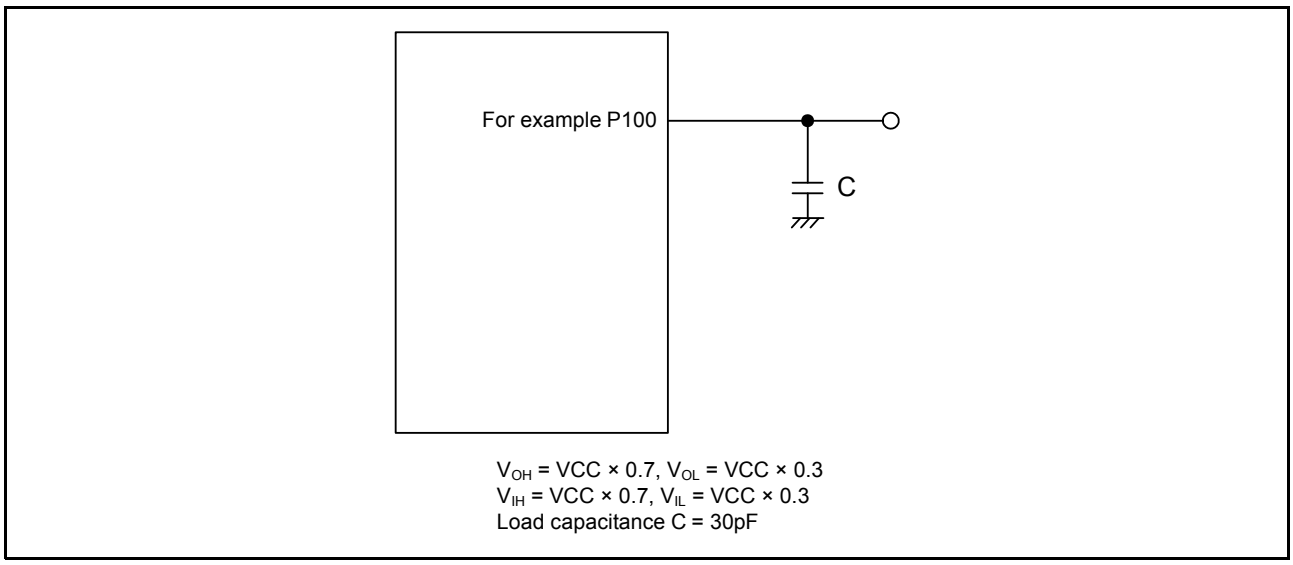


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	–0.3 to +4.6	V
VBATT power supply voltage	VBATT	–0.3 to +4.6	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	–0.3 to +5.8	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0 *2	–0.3 to +4.6	V
USBHS power supply voltage	VCC_USBHS	–0.3 to +4.6	V
USBHS analog power supply voltage	AVCC_USBHS	–0.3 to +4.6	V
Switching regulator power supply voltage	VCC_DCDC	–0.3 to +4.6	V
Analog input voltage	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

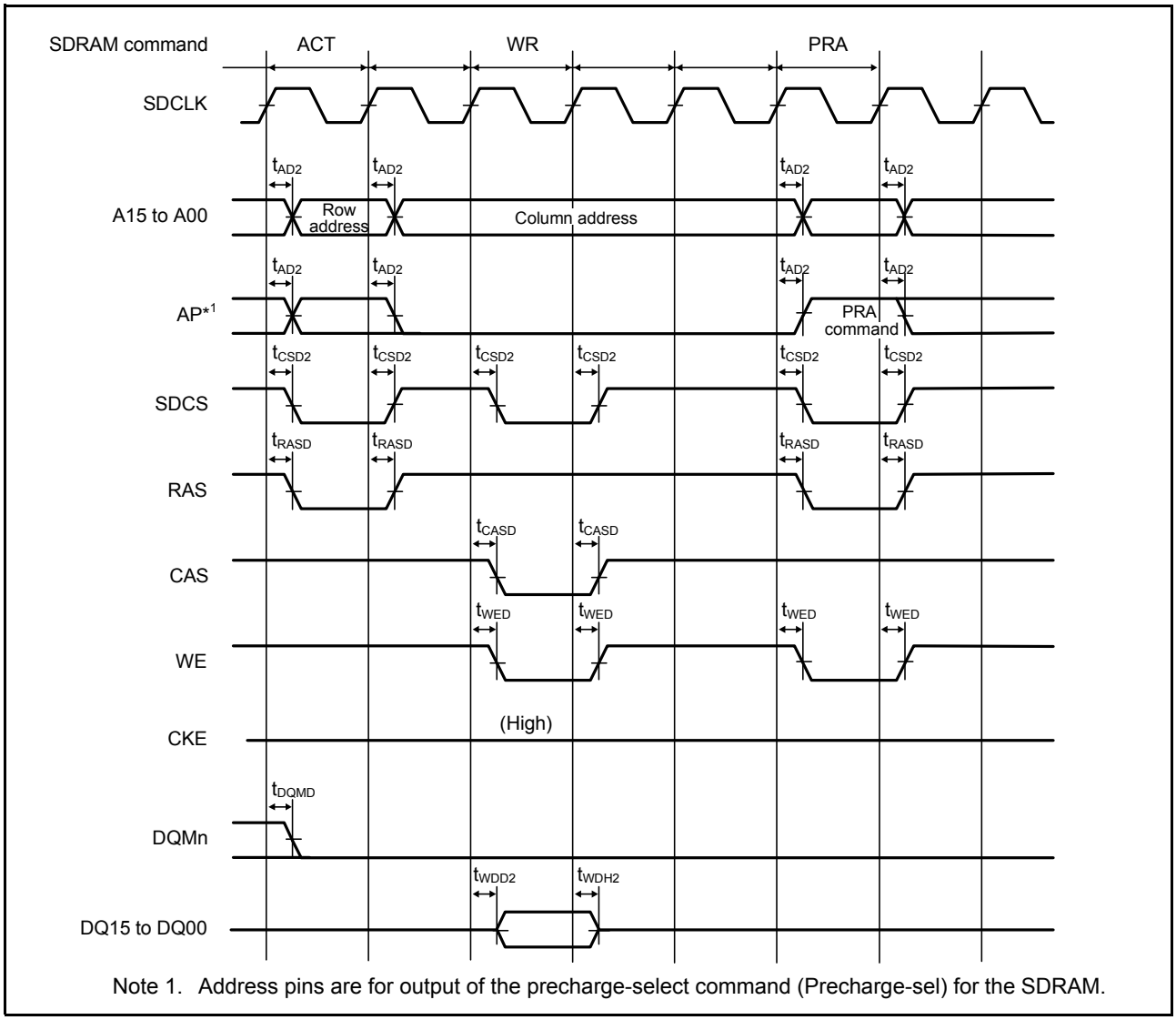
Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.

Note 2. Connect AVCC0 and VCC_USB to VCC.

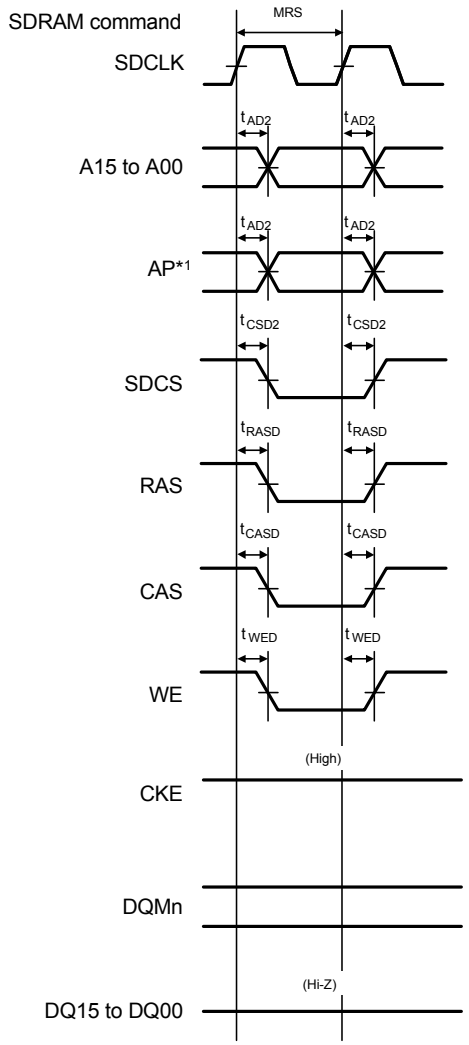
Note 3. See section 2.2.1, Tj/Ta Definition.

Note 4. Contact a Renesas Electronics sales office for information on derating operation when T_a = +85°C to +105°C.



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.20 SDRAM single write timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.24 SDRAM mode register set timing

Table 2.24 SCI timing (3) (2/2)

Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	-	300	ns	Figure 2.42
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: SCL1_A output is not supported in these specifications.
t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKA cycle.

Note 1. Cb indicates the total capacity of the bus line.

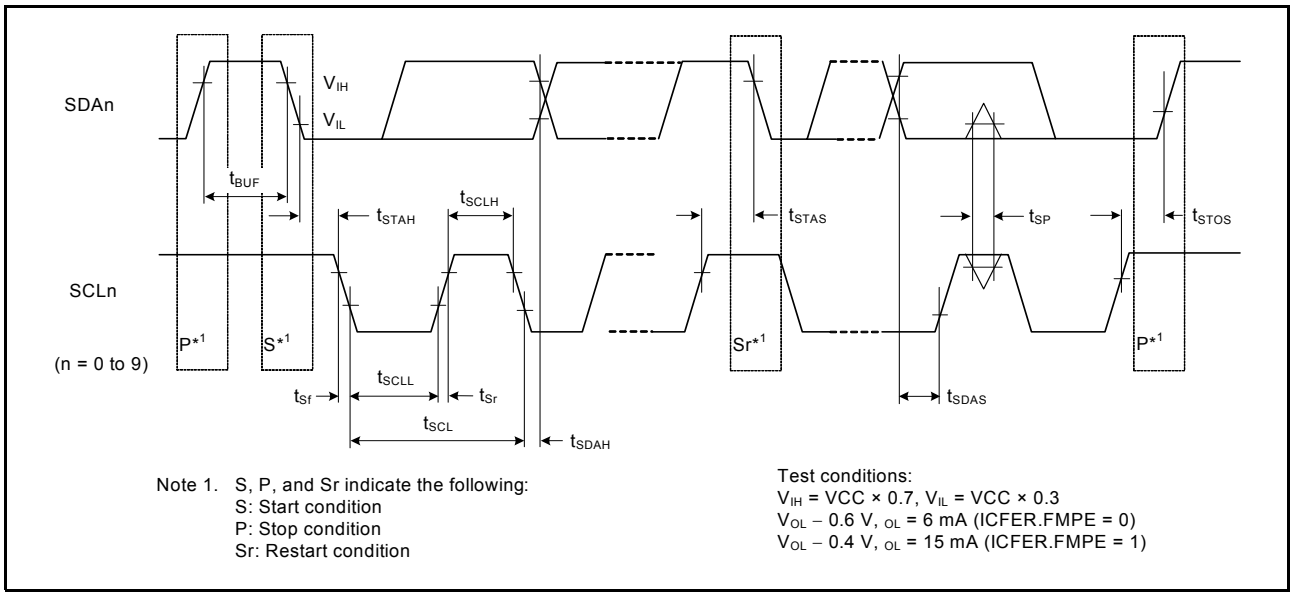


Figure 2.42 SCI simple IIC mode timing

2.3.11 SPI Timing

Table 2.25 SPI timing

Conditions:

(1) Middle drive output is selected with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.

Item			Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.43 C = 30 pF
		Slave		6	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	μs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 2.44 to Figure 2.49 C = 30 pF
		Slave		5	-		
	Data input hold time	Master	t_{HF}*4	0	-	ns	-
		Master	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		-
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc}$ - 10*2	$N \times t_{SPcyc}$ + 100 *2	ns	-
		Slave		$6 \times t_{Pcyc}$	-	ns	-
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc}$ - 10 *3	$N \times t_{SPcyc}$ + 100 *3	ns	-
		Slave		$6 \times t_{Pcyc}$	-	ns	-
	Data output delay	Master	t_{OD}	-	6.3	ns	Figure 2.44 to Figure 2.49 C = 30pF
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$6 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	μs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	μs	
	Slave access time		t_{SA}	-	$2 \times t_{Pcyc} + 28$	ns	Figure 2.48 and Figure 2.49 C = 30pF
	Slave output release time		t_{REL}	-	$2 \times t_{Pcyc} + 28$		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. N is set to an integer from 1 to 8 by the SPCKD register.

Note 3. N is set to an integer from 1 to 8 by the SSLND register.

Note 4. PCLKA division ratio set to 1/2.

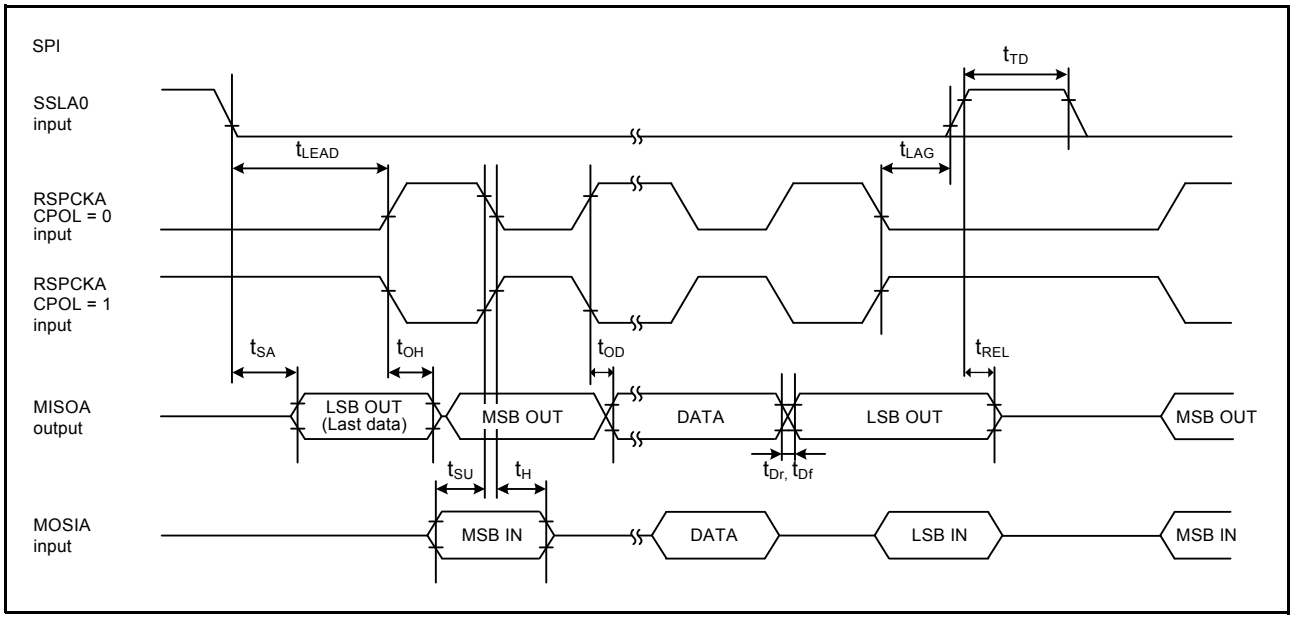


Figure 2.49 SPI timing for slave when CPHA = 1

2.3.12 QSPI Timing

Table 2.26 QSPI timing

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit*1	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 2.50
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	Data input setup time	t_{Su}	11	-	ns	Figure 2.51
	Data input hold time	t_{IH}	0	-	ns	
	QSSL setup time	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 *2	(N+0.5) x t_{Qscyc} +100 *2	ns	
	QSSL hold time	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 *3	(N+0.5) x t_{Qscyc} +100 *3	ns	
	Data output delay	t_{OD}	-	4	ns	
	Data output hold time	t_{OH}	–3.3	-	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set to 0 or 1 in SFMSLD.
Note 3. N is set to 0 or 1 in SFMSHD.

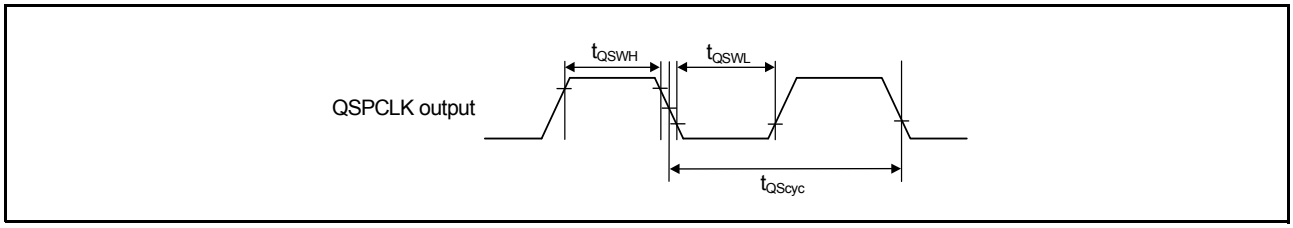


Figure 2.50 QSPI clock timing

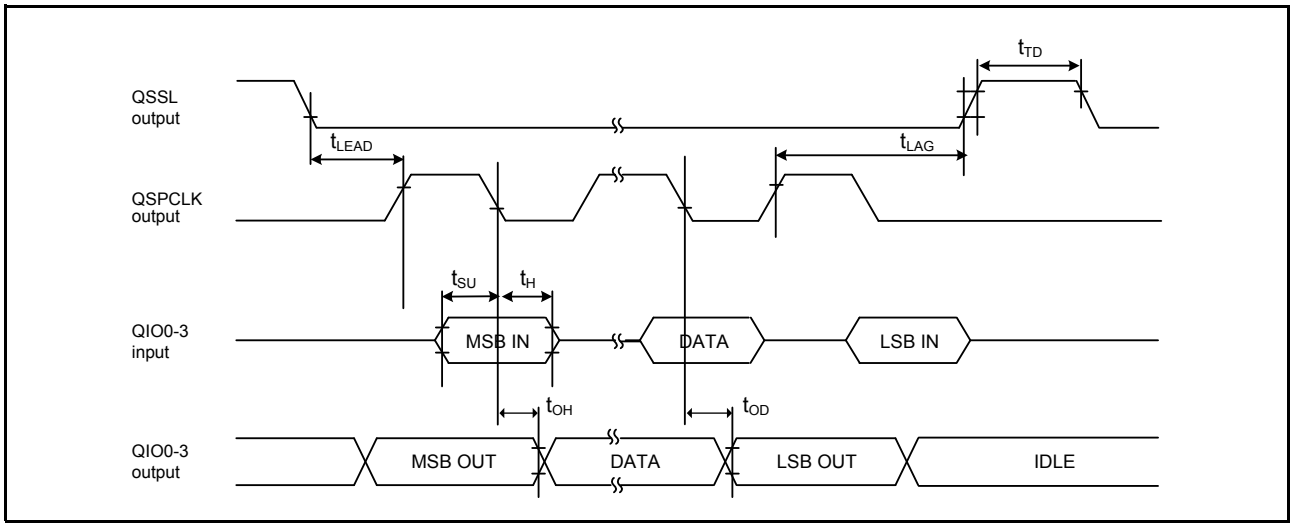


Figure 2.51 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1/2)

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

Item		Symbol	Min*1, *2	Max	Unit	Test conditions
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

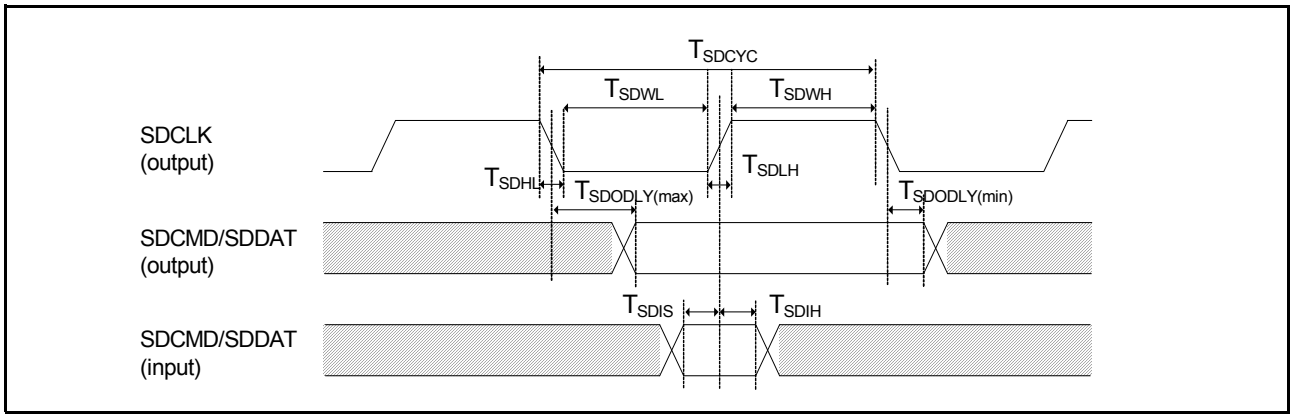


Figure 2.57 SD/MMC Host Interface signal timing

2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO, ET1_MDC, and ET1_MDIO
For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	-	ns	Figure 2.58 to Figure 2.61
	REF50CK frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay	T_{co}	2.5	12.0	ns	
	RMII_xxxx*2 setup time	T_{su}	3	-	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	-	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.4	4	ns	
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.62
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	-	ns	-
	ET_TX_EN output delay	t_{TENd}	1	20	ns	Figure 2.63
	ET_ETXD0 to ET_ETXD3 output delay	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	-	ns	
	ET_CRS hold time	t_{CRSh}	10	-	ns	
	ET_COL setup time	t_{COLs}	10	-	ns	Figure 2.64
	ET_COL hold time	t_{COLh}	10	-	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	-	ns	-
	ET_RX_DV setup time	t_{RDVs}	10	-	ns	Figure 2.65
	ET_RX_DV hold time	t_{RDVh}	10	-	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	-	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	-	ns	
	ET_RX_ER setup time	t_{RERs}	10	-	ns	Figure 2.66
	ET_RX_ER hold time	t_{RESh}	10	-	ns	
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 2.67

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.

2.3.17 PDC Timing

Table 2.32 PDC timing

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Item		Symbol	Min	Max	Unit	Test conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 2.68
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 2.69
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3$	-	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} – t_{PCKr} – t_{PCKf})/2 – 3$	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 2.70
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

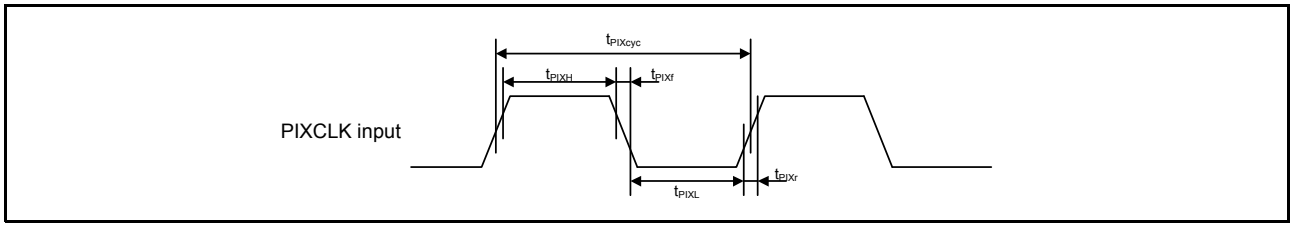


Figure 2.68 PDC input clock timing

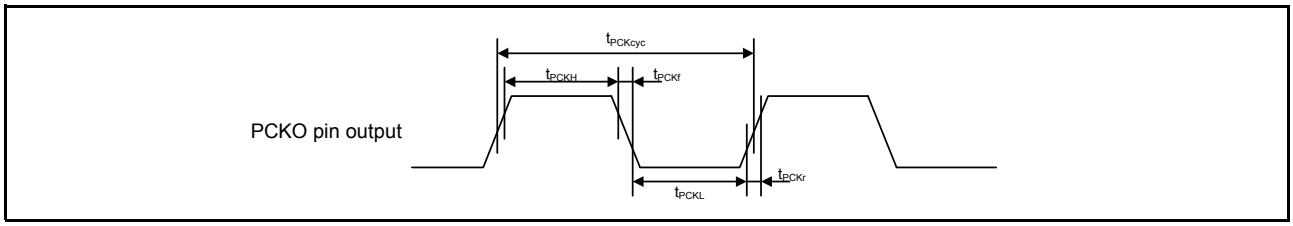


Figure 2.69 PDC output clock timing

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (2/2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.85
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

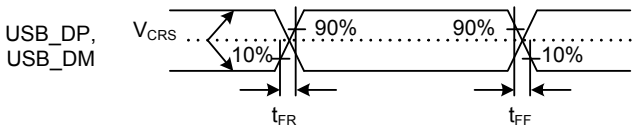


Figure 2.85 USB_DP and USB_DM output timing in full-speed mode

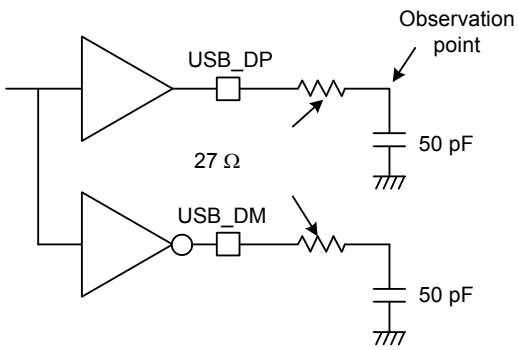


Figure 2.86 Test circuit in full-speed mode

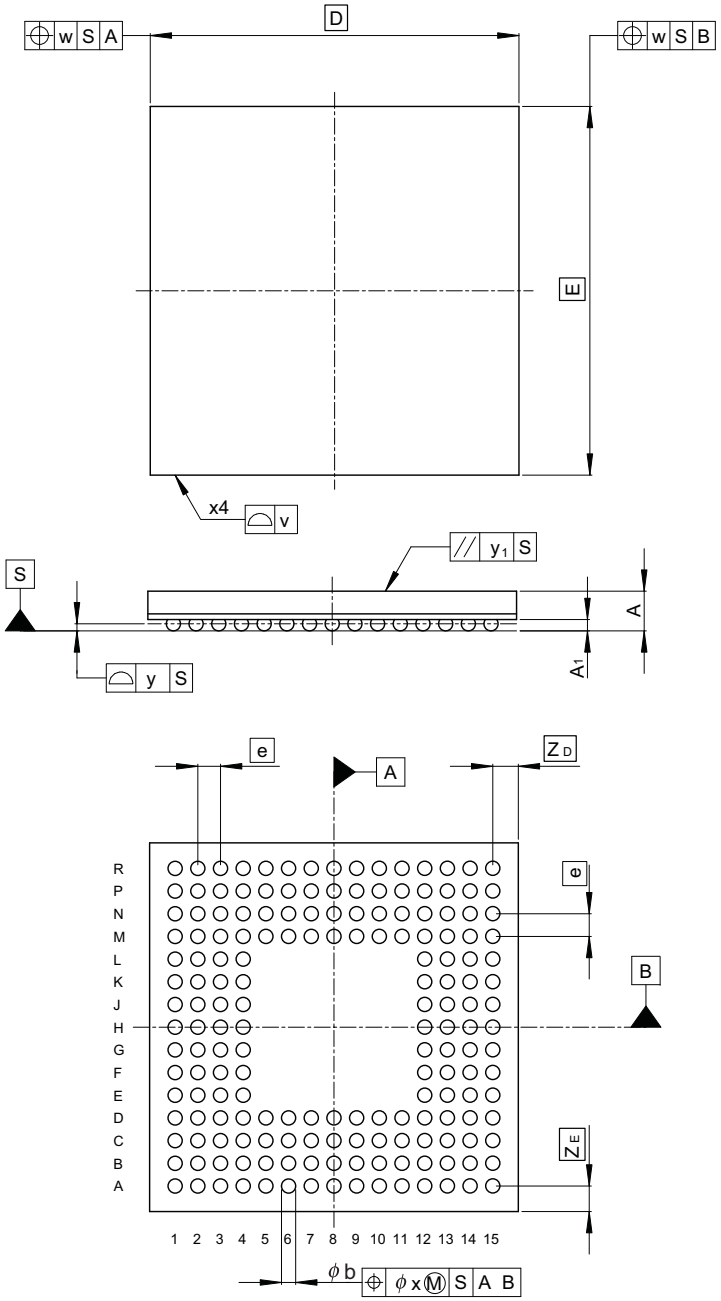
2.5 ADC12 Characteristics

[Normal-precision channel]

Table 2.40 A/D conversion characteristics for unit 0 (1/2)
Conditions: PCLKC = 1 to 60 MHz

Item	Min	Typ	Max	Unit	Test conditions
Frequency	1	-	60	MHz	-
Analog input capacitance	-	-	30	pF	-
Quantization error	-	±0.5	-	LSB	-
Resolution	-	-	12	Bits	-

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure 1.2 176-pin BGA

Revision History	S7G2 Datasheet

Rev.	Date	Chapter	Summary
0.80	Oct. 12, 2015	—	First Edition issued
0.85	Dec. 15, 2015	—	Second Edition issued
1.00	Feb. 23, 2016	section 1, Overview	Updated VREFH and VREFL descriptions in Table 1.16, Pin functions
		section 2, Electrical Characteristics	Updated operating and standby current information in section 2.2.5, Operating and Standby Current
			Added section 2.16, Joint European Test Action Group (JTAG)
			Added section 2.17, Serial Wire Debug (SWD)
			Added section 2.18, Embedded Trace Macro Interface (ETM)
			Updated Table 2.13, Clock timing except for sub-clock oscillator
			Updated SPI data in Table 2.25, SPI timing
			Updated Table 2.40, A/D conversion characteristics for unit 0
			Updated Table 2.41, A/D conversion characteristics for unit 1
			Updated SPI data in Figure 2.45, SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2
			Updated Table 2.5, I/O IOH, IOL
		All	Deleted # from pin names

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