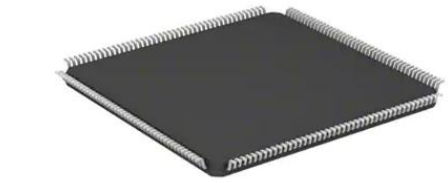
Renesas Electronics America Inc - R7FS7G27H3A01CFC#AA0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	126
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs7g27h3a01cfc-aa0

Table 1.13 Data processing (2/2)

Feature	Functional description
Sampling Rate Converter (SRC)	The SRC converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. The sampling rate of the input signal can be one of the following: • 8 kHz • 11.025 kHz • 12 kHz • 16 kHz • 22.05 kHz • 24 kHz • 32 kHz • 44.1 kHz • 48 kHz. The sampling rate of the output signal can be one of the following: • 8 kHz • 16 kHz • 32 kHz • 44.1 kHz • 48 kHz. Independent FIFOs are provided for input and output. In a typical application, a DMA controller can be used to transfer PCM audio data from SRAM, for example, to the SRC. Sample-converted audio data from the SRC can then be transferred using the DMA Controller to the SSI, from where it can be transmitted to an external audio codec. See section 42, Sampling Rate Converter (SRC) in User's Manual.

Table 1.14 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and DLP. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH - 128-bit unique ID.

Table 1.16 Pin functions (2/5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal.
	SDCS	Output	SDRAM chip select signal, active LOW.
	RAS	Output	SDRAM low address strobe signal, active LOW.
	CAS	Output	SDRAM column address strobe signal, active LOW.
	WE	Output	SDRAM write enable signal, active LOW.
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00.
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08.
	A00 to A15	Output	Address bus.
	DQ00 to DQ15	I/O	Data bus.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ15	Input	Maskable interrupt request pins.
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins.
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable signals.
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins.
	AGTO0, AGTO1	Output	Pulse output pins.
	AGTOA0, AGTOA1	Output	Output compare match A output pins.
	AGTOB0, AGTOB1	Output	Output compare match B output pins.
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active LOW.
	SCL0 to SCL9	I/O	Input/output pins for the IIC clock (simple IIC).
	SDA0 to SDA9	I/O	Input/output pins for the IIC data (simple IIC).
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI).
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI).
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI).
	SS0 to SS9	Input	Chip-select input pins (simple SPI), active LOW.
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock.
	SDA0 to SDA2	I/O	Input/output pins for data.

Table 1.17 Pin list (5/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
A12	B12	54	C9	46	-	-	P202	WR1/BC1	-	-	-	GTIOC5B_A	-	CRX0_A	SCK2_A	RXD9_A/MISO9_A/SDA9_A	-	MISOB_A		ET0_ERXD2	-	-	SD0DAT6	-	-	-	IRQ3-DS	LCD_TCON3_B
E10	A12	55	B9	47	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ERXD3	-	-	SD0DAT7	-	-	-	-	LCD_TCON2_B
F9	C11	56	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCON1_B
C11	B11	57	-	-	-	-	P315	A22	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCON0_B
E9	A11	58	-	-	-	-	P900	A23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_B
B11	C10	59	-	-	-	-	P901		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_B
A11	-	-	-	-	-	-	P902	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_B
C10	D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D10	D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	-	-	-	-	-	-	P903	-	-	-	-	GTIOC7A_B	-	-	-	-	-	-	-	-	-	-	SD0CD	-	-	-	-	-
C9	-	-	-	-	-	-	P904	-	-	-	-	GTIOC7B_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	A10	62	A8	50	33	VCL1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B10	B10	63	B8	51	34	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A9	A9	64	A7	52	35	VLO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B9	B9	65	B7	53	36	VLO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A8	A8	66	A6	54	37	VCC_DCDC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H8	-	-	-	-	-		P913	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F8	C9	67	C7	55	38	RES		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	B8	68	B6	56	39	MD	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	C8	69	C8	57	40	-	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	NMI	-
B7	-	-	-	-	-	-	P912	-	-	-	-	GTIOC8A_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A7	-	-	-	-	-	-	P911	-	-	-	-	GTIOC8B_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	-	-	-	-	-	-	P910	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA22_B
E8	-	-	-	-	-	-	P909	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA21_B

Table 1.17 Pin list (8/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces											Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
G4	D1	100	E2	84	60	-	P609	CS1	CKE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
E1	F3	101	F3	85	61	-	P610	CS0	WE	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	E2	102	E1	86	-	-	P611		SDCS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F2	E1	103	F2	87	-	-	P612	D08	DQ08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F3	F4	104	F1	88	-	-	P613	D09	DQ09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F1	F2	105	G3	89	-	-	P614	D10	DQ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G8	F1	106	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G7	G1	107	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B
G6	-	-	-	-	-	-	PA11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA18_B
G5	-	-	-	-	-	TCLK	PA12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
H4	G4	108	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA08_B
H7	-	-	-	-	-	TDATA0	PA13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G3	-	-	-	-	-	TDATA1	PA14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H5	G2	109	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_B
G2	-	-	-	-	-	TDATA2	PA15	-	-	-	-	GTIOC9A_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G1	-	-	-	-	-	TDATA3	P813	-	-	-	-	GTIOC9B_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	H1	112	H1	92	64	VCL_F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J1	-	-	-	-	-		PA07	-	-	-	-	GTIOC10A_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J2	-	-	-	-	-		PA06	-	-	-	-	GTIOC10B_B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	-	-	-	-	-		PA05	-	-	-	-	GTIOC11A_B	-	-	-	CTS7_RTS7_B/SS7_B	-	-	-	-	-	-	-	-	-	-	-	-
J4	-	-	-	-	-		PA04	-	-	-	-	GTIOC11B_B	-	-	-	SCK7_B	-	-	-	-	-	-	-	-	-	-	-	-

Table 1.17 Pin list (9/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
J5	-	-	-	-	-		PA03	-	-	-	-	-	-	-	-	RXD7_B/MISO7_B/SCL7_B	-	-	-	-	-	-	-	-	-	-	IRQ9	-
H6	-	-	-	-	-		PA02	-	-	-	-	-	-	-	-	TXD7_B/MOSI7_B/SDA7_B	-	-	-	-	-	-	-	-	-	-	IRQ10	-
J6	H2	113	-	-	-		PA01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_B
J7	H4	114	-	-	-		PA00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_B
K5	J4	115	-	-	-		P607	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_B
K6	J1	116	-	-	-		P606	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_B
K1	J2	117	H2	93	-		P605	D11	DQ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K2	J3	118	G4	94	-		P604	D12	DQ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	K3	119	H3	95	-		P603	D13	DQ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L1	K1	120	J1	96	65		P602	EBCLK	SDCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_A
L2	K2	121	J2	97	66	-	P601	WR/WR0	DQM0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_A
L3	L1	122	H4	98	67	-	P600	RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA02_A
M2	K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M1	L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K4	L2	125	J3	101	68	-	P107	D07	DQ07	-	-	GTIOC8A_A	-	-	CTS8_RTS8_A/SS8_A	-	-	-	-	-	-	-	-	-	-	-	KR07	LCD_DATA01_A
L4	M1	126	K3	102	69	-	P106	D06	DQ06	-	-	GTIOC8B_A	-	-	SCK8_A	-	-	SSLA3_A	-	-	-	-	-	-	-	-	KR06	LCD_DATA00_A
M3	L3	127	J4	103	70	-	P105	D05	DQ05	-	GTETRGA_C	-	-	-	TXD8_A/MOSI8_A/SDA8_A	-	-	SSLA2_A	-	-	-	-	-	-	-	-	IRQ0/KR05	LCD_TCON3_A
N3	M2	128	L3	104	71	-	P104	D04	DQ04	-	GTETRGB_B	-	-	-	RXD8_A/MISO8_A/SCL8_A	-	-	SSLA1_A	-	-	-	-	-	-	-	-	IRQ1/KR04	LCD_TCON2_A

Table 1.17 Pin list (10/12)

Pin number						Power, System, Clock, Debug,	I/O port	Extbus		Timers				Communication interfaces											Analog		HMI		
BGA224	BGA176	LQFP176	LGA145	LQFP144	LQFP100			External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSI	MII (25 MHz)	RMII (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	Interrupt	GLCDC, PDC
N2	N1	129	L1	105	72	-	P103	D03	DQ03	-	GTOWUP_A	GTIOC2A_A	-	-	CTS0_RTS0_A/SS0_A	-	-	SSLA0_A	-	-	-	-	-	-	-	-	KR03	LCD_TCON1_A
N1	M3	130	M1	106	73	-	P102	D02	DQ02	AGTO0	GTOWLO_A	GTIOC2B_A	-	-	SCK0_A	-	-	RSPCKA_A	-	-	-	-	-	ADTRG0_A	-	-	KR02	LCD_TCON0_A
P1	N2	131	M2	107	74	-	P101	D01	DQ01	AGTEE0	GTETRGB_A	-	-	-	TXD0_A/MOSI_A/SDA0_A	CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	-	-	-	-	-	-	-	-	IRQ1/KR01	LCD_CLK_A
R1	P1	132	N1	108	75	-	P100	D00	DQ00	AGTIO0_A	GTETRGA_A	-	-	-	RXD0_A/MISO0_A/SLC0_A	SCK1_A	SCL1_B	MISOA_A	-	-	-	-	-	-	-	-	IRQ2/KR00	LCD_EXTCLK_A
P2	N3	133	L2	109	-	-	P800	D14	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R2	R1	134	N2	110	-	-	P801	D15	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT4	-	-	-	-	-
K7	-	-	-	-	-	-	P808	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K8	-	-	-	-	-	-	P809	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P3	-	-	-	-	-	-	P810	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	P2	135	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT5	-	-	-	-	LCD_DATA02_B
P4	R2	136	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT6	-	-	-	-	LCD_DATA01_B
M4	P3	137	-	-	-		P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT7	-	-	-	-	LCD_DATA00_B
L5	-	-	-	-	-		P811	-	-	-	-	-	-	CTX0_C	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L6	-	-	-	-	-		P812	-	-	-	-	-	-	CRX0_C	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L7	N4	138	N3	111	-	VCC		-	-	-	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-
L8	M4	139	M3	112	-	VSS		-	-	-	-	-	-		-	-	-	-	-	-	-	-	-	-	-	-	-	-
R4	R3	140	K4	113	76	-	P500	-	-	AGTOA0	GTIU_B	GTIOC11A_A	-	USB_VBUSEN_B	-	-	-	QSPCLK	-	-	-	-	SD1CLK	AN016	IVREF0	-	-	-
N4	P4	141	M4	114	77	-	P501	-	-	AGTOB0	GTIV_B	GTIOC11B_A	-	USB_OVRCURA_B	-	TXD5_A/MOSI5_A/SDA5_A	-	QSSL	-	-	-	-	SD1CMD	AN116	IVREF1	-	IRQ11	-
N5	R4	142	L4	115	78	-	P502	-	-	-	GTIW_B	GTIOC12A	-	USB_OVRCURB_B	-	RXD5_A/MISO5_A/SCL5_A	-	QIO0	-	-	-	-	SD1DAT0	AN017	IVCMP0	-	IRQ12	-

Derating is the systematic reduction of load for improved reliability.

Table 2.2 Recommended operating conditions

Item	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
Switching regulator power supply voltage	VCC_DCDC	When switching regulator is used	-	VCC	-	V
		When switching regulator is not used	-	0	-	V
VBATT power supply voltage	VBATT		2.0		3.6	V
Analog power supply voltages	AVCC0		-	VCC	-	V
	AVSS0		-	0	-	V

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) –40 to +105°C

Item	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1/2)

Item			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI	V_{IH}	VCC × 0.8	-	VCC + 0.3	V
			V_{IL}	–0.3	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15	V_{IH}	VCC × 0.7	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.3	
		ETHERC	V_{IH}	2.3	-	VCC + 0.3	
			V_{IL}	–0.3	-	VCC × 0.2	
		IIC (SMBus)*1	V_{IH}	2.1	-	VCC + 0.3	
			V_{IL}	–0.3	-	0.8	
		IIC (SMBus)*2	V_{IH}	2.1	-	5.8	
			V_{IL}	–0.3	-	0.8	

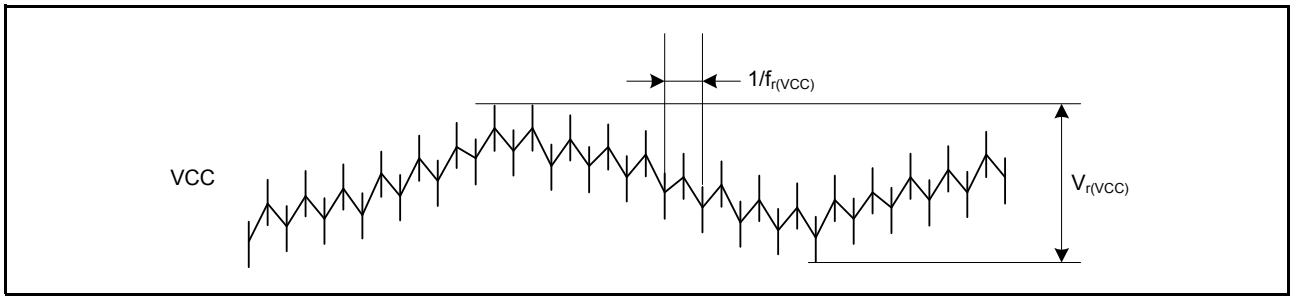


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

Item			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)		f	-	-	240	MHz
	Peripheral module clock (PCLKA)*2			-	-	120	
	Peripheral module clock (PCLKB)*2			-	-	60	
	Peripheral module clock (PCLKC)*2			-*3	-	60	
	Peripheral module clock (PCLKD)*2			-	-	120	
	Flash interface clock (FCLK)*2			-*1	-	60	
	External bus clock (BCLK)*2			-	-	120	
	EBCLK pin output			-	-	60	
	SDCLK pin output	VCC ≥ 3.0 V		-	-	120	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

Item		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2,*3		-*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	
	External bus clock (BCLK)		-	-	1	
	EBCLK pin output		-	-	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.13 Clock timing except for sub-clock oscillator (2/2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.61	16	16.39	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.56	18	18.44		
		f_{HOCO20}	19.52	20	20.48		
		f_{HOCO16}	15.52	16	16.48		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.46	18	18.54		
		f_{HOCO20}	19.40	20	20.60		
	With FLL	f_{HOCO16}	15.91	16	16.09		SOSC frequency is 32.768kHz ± 50ppm
		f_{HOCO18}	17.90	18	18.10		
		f_{HOCO20}	19.89	20	20.11		
HOCO clock oscillation stabilization wait time *2		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	3	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 2.7

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*1	s	-

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the value shown is recommended.

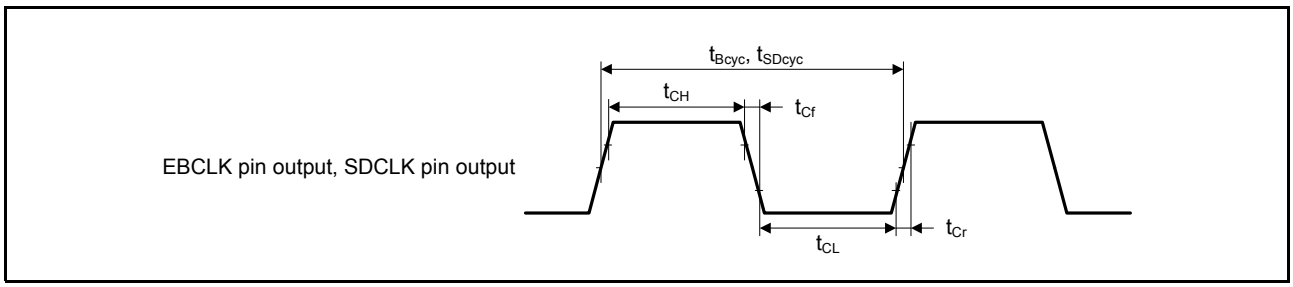
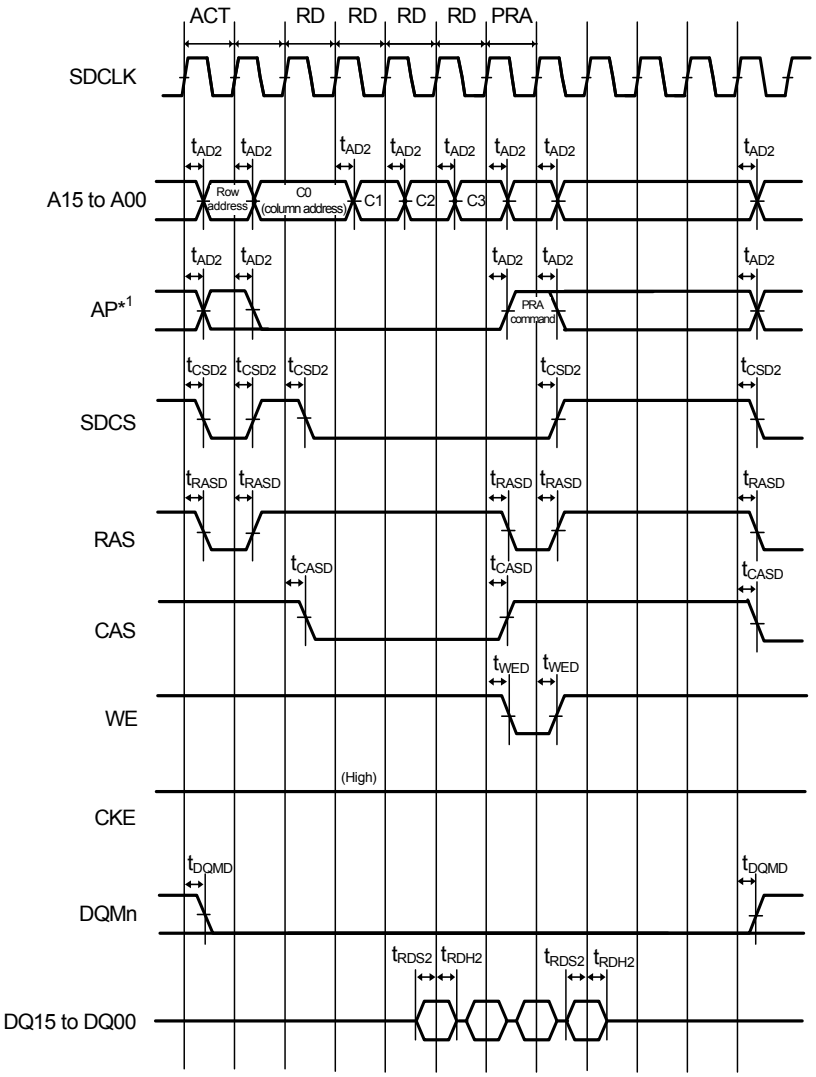


Figure 2.3 EBCLK and SDCLK output timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.21 SDRAM multiple read timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2/2)

GPT32 Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: GTIOC6A_A, GTIOC6B_A, GTIOC3A_B, GTIOC3B_B, GTIOC0A_B, GTIOC0B_B, GTIOC9A_B, GTIOC9B_B.
High drive output is selected in the port drive capability bit in the PmnPFS register for all other pins.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.28
		Dual edge		2.5	-		
	GTIOCxY_Z output skew (x = 0 to 7, Y= A or B , Z = A or B)	Middle drive buffer	t_{GTISK}*2	-	4	ns	Figure 2.29
		High drive buffer		-	4		
	GTIOCxY_Z output skew (x = 8 to 13, Y = A or B, Z = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY_Z output skew (x = 0 to 13, Y = A or B, Z = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP_x, GTOULO_x, GTOVUP_x, GTOVLO_x, GTOWUP_x, GTOWLO_x (x = A or B)		t_{GTOSK} *2	-	5	ns	Figure 2.30
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*3	-	2.0	ns	Figure 2.31
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*1	100	-	ns	Figure 2.32
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.33
KINT	Key interrupt input low width		t_{KR}	250	-	ns	Figure 2.34

Note 1. t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 3. The load is 30 pF.
Note 4. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

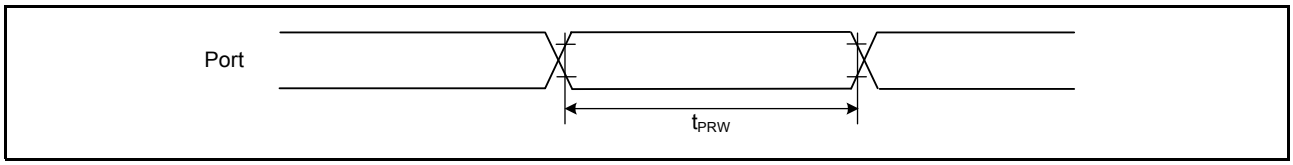


Figure 2.26 I/O ports input timing

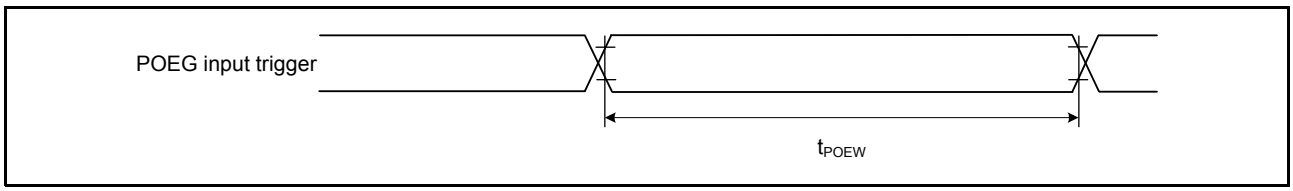


Figure 2.27 POEG input trigger timing

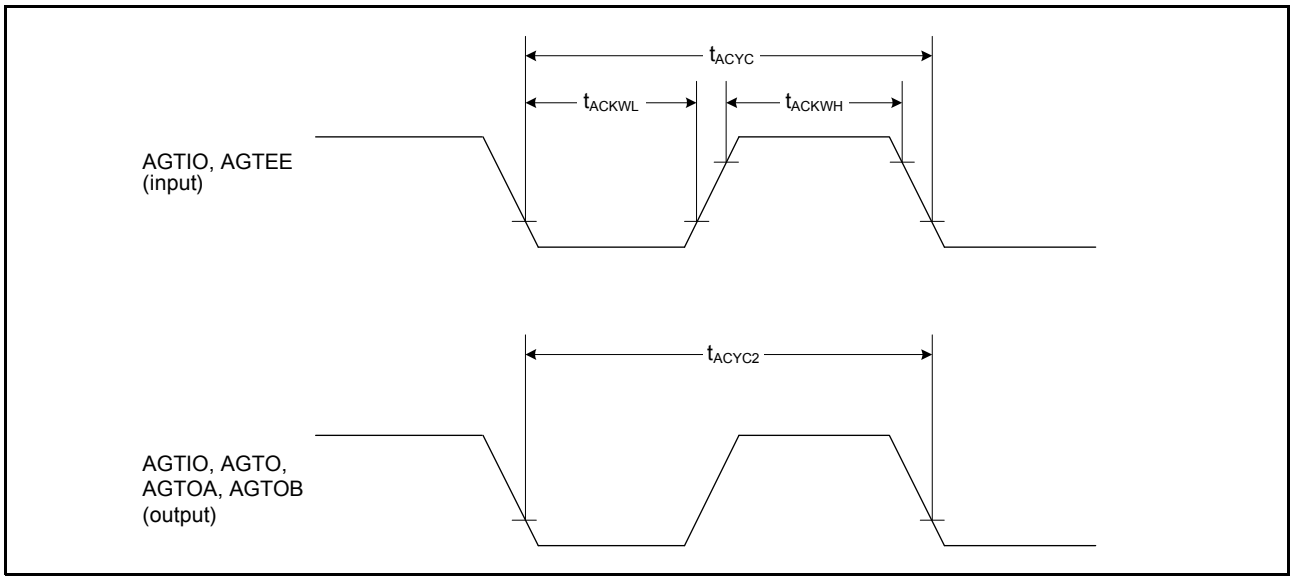


Figure 2.32 AGT input/output timing

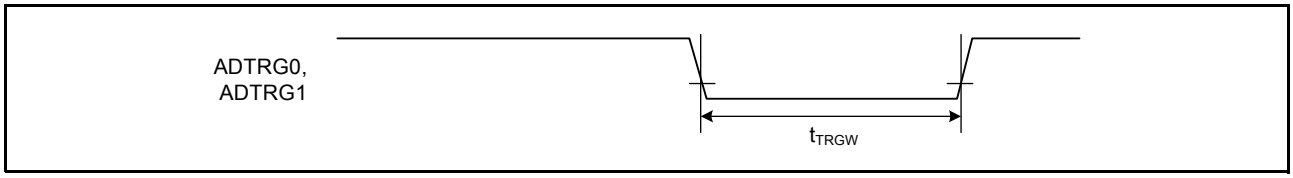


Figure 2.33 ADC12 trigger input timing

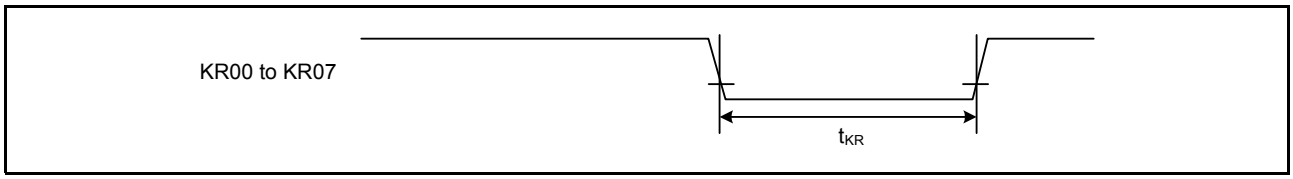


Figure 2.34 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

Item			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

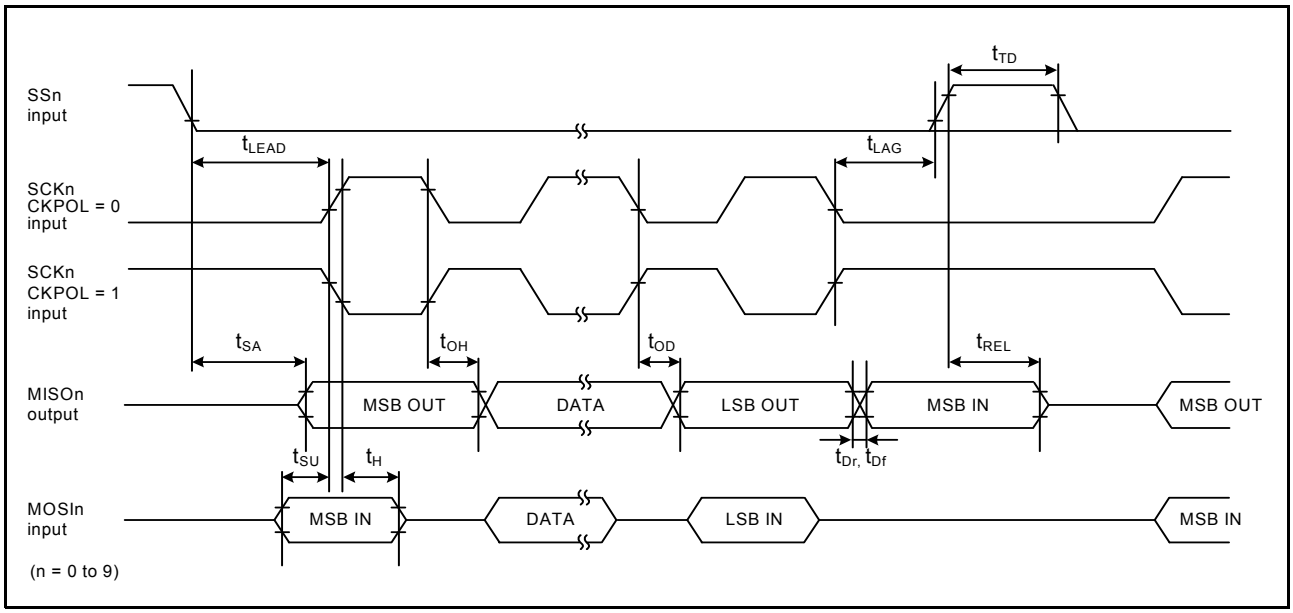


Figure 2.40 SCI simple SPI mode timing for slave when CKPH = 1

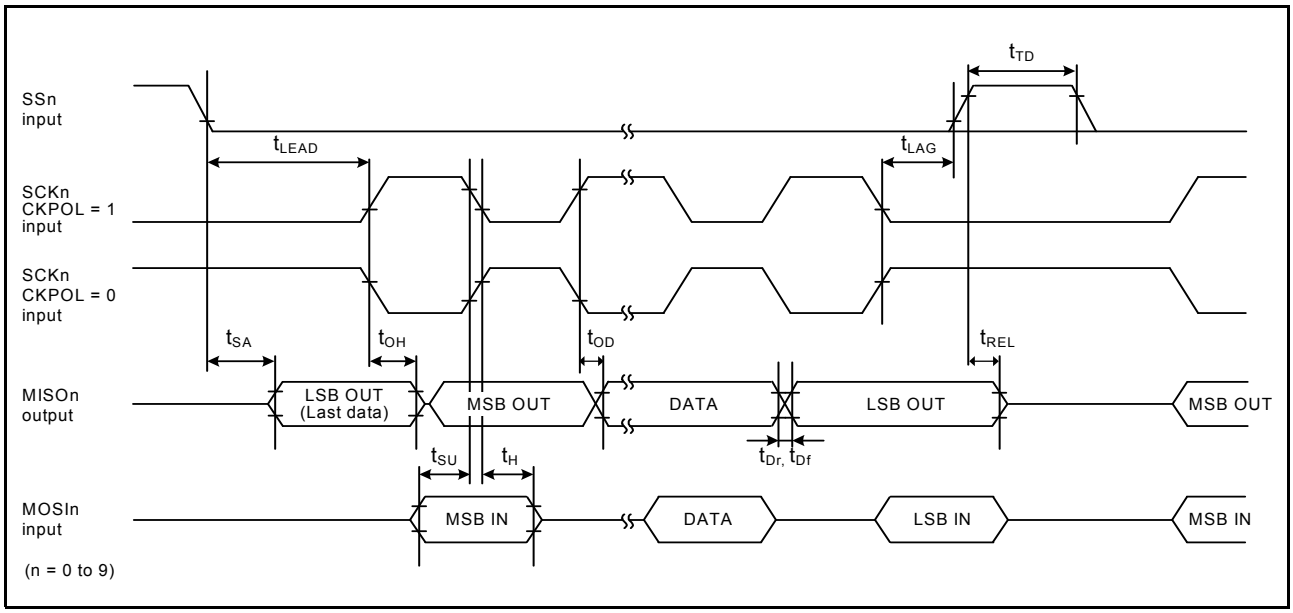


Figure 2.41 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1/2)

Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.42
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Table 2.24 SCI timing (3) (2/2)
Conditions: For the SCL1_A pins, low drive output is selected in the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	-	300	ns	Figure 2.42
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Note: SCL1_A output is not supported in these specifications.
t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKA cycle.
Note 1. Cb indicates the total capacity of the bus line.

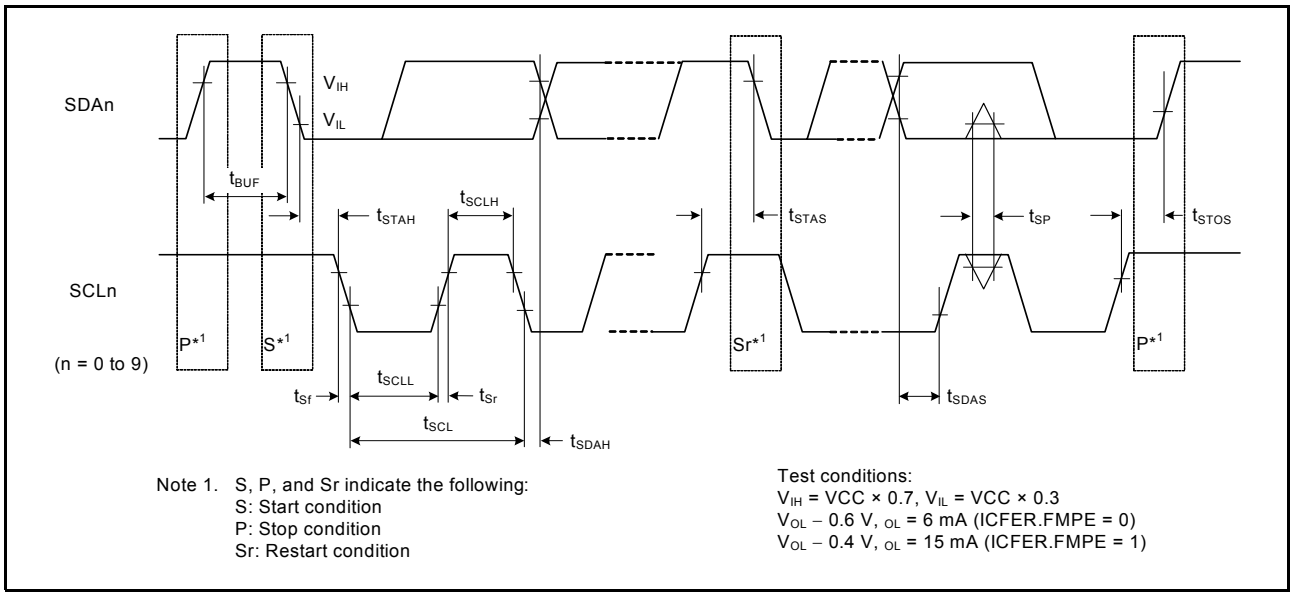


Figure 2.42 SCI simple IIC mode timing

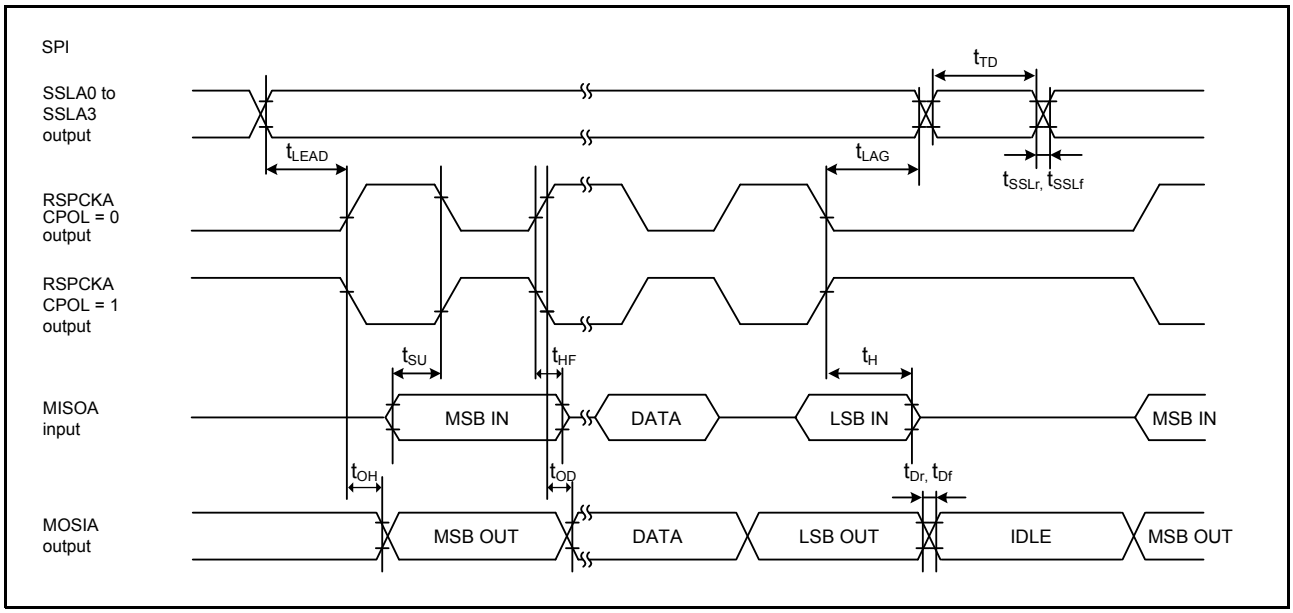


Figure 2.47 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

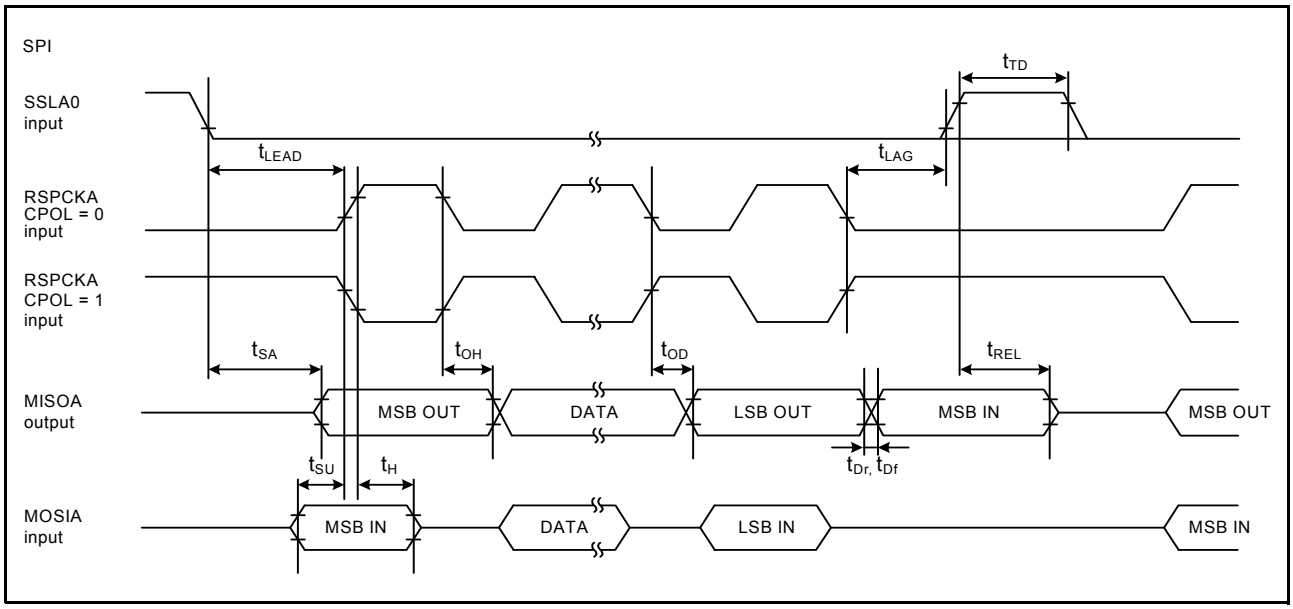


Figure 2.48 SPI timing for slave when CPHA = 0

Table 2.28 IIC timing (2)

(1) Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 2.52
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3(6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

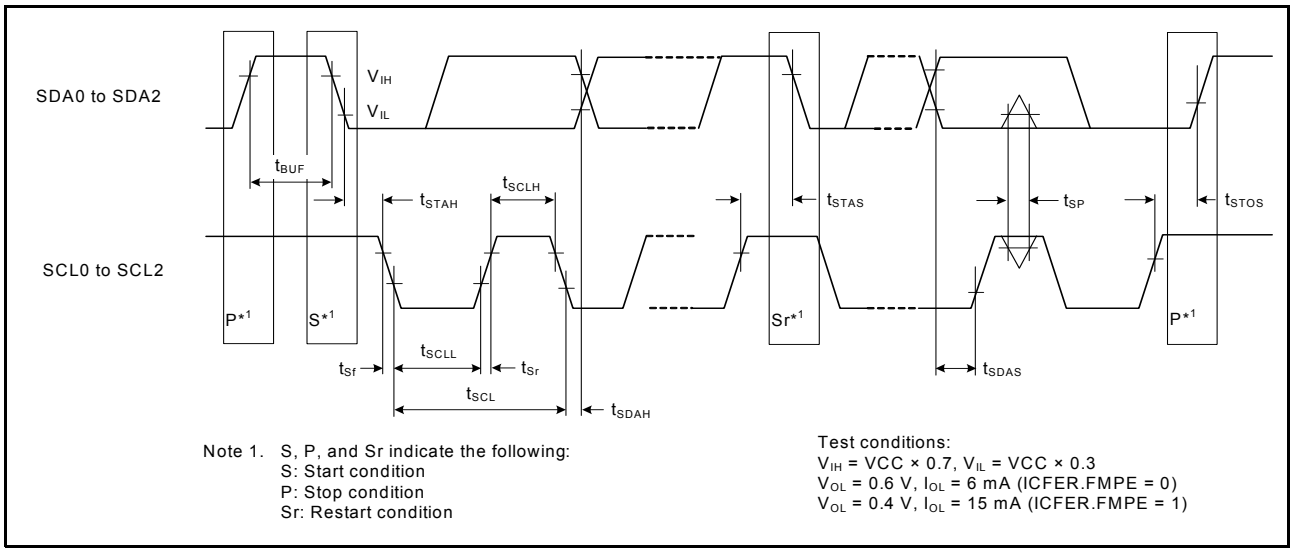


Figure 2.52 I²C bus interface input/output timing

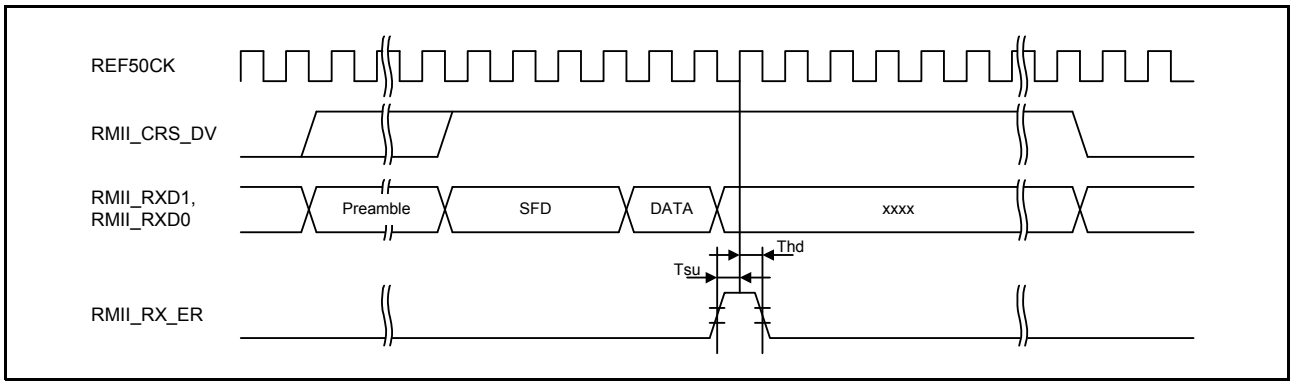


Figure 2.61 RMII reception timing when an error occurs

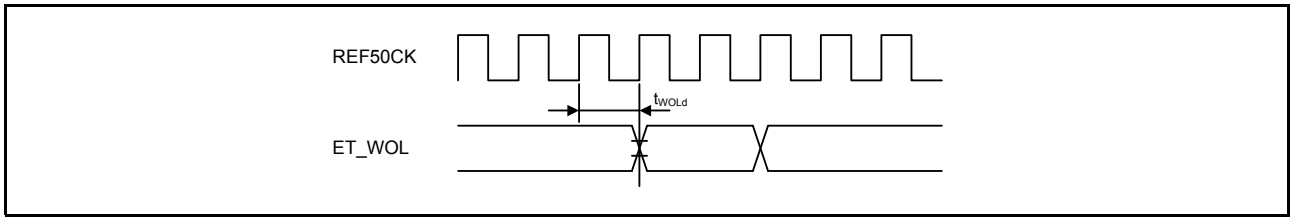


Figure 2.62 WOL output timing for RMII

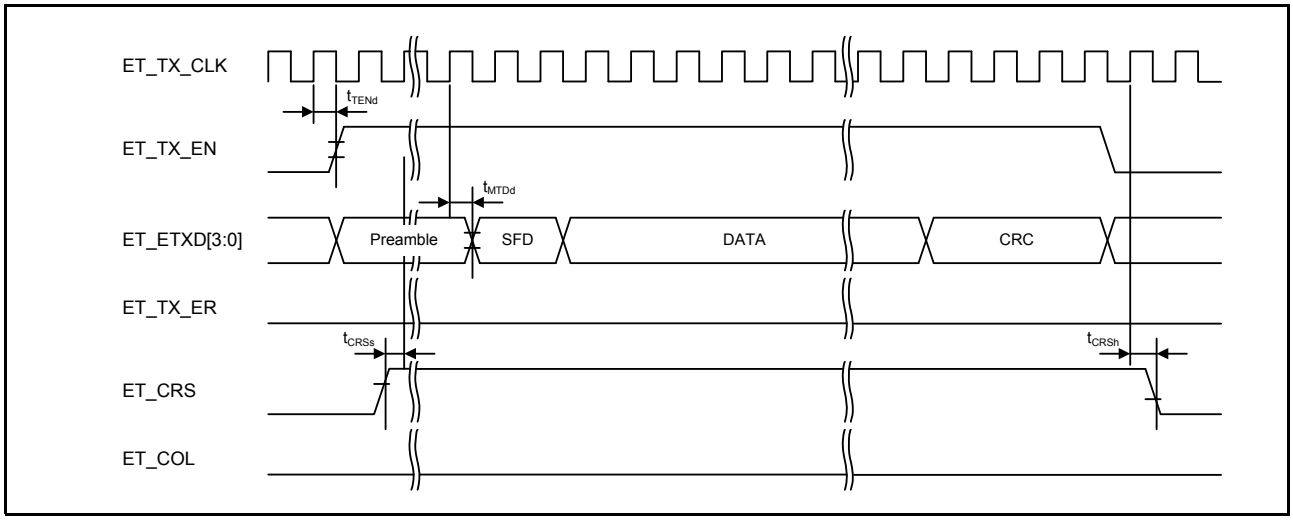


Figure 2.63 MII transmission timing in normal operation

Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics) (2/2)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
AC characteristics	Rise time	t_{HSR}	500	-	-	ps	Figure 2.81
	Fall time	t_{HSF}	500	-	-	ps	
	Output resistance	Z_{HSDRV}	40.5	-	49.5	Ω	-

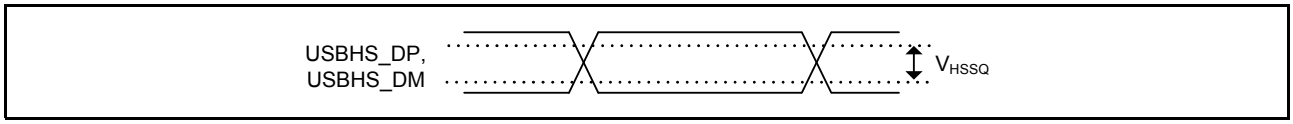


Figure 2.79 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode

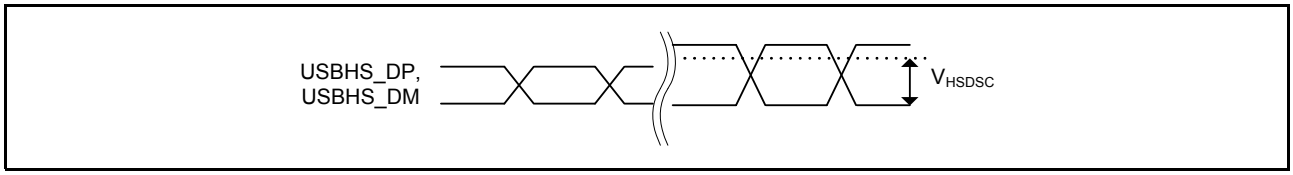


Figure 2.80 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode

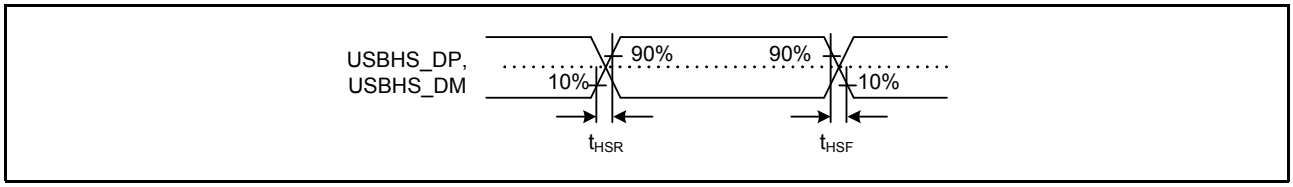


Figure 2.81 USBHS_DP and USBHS_DM output timing in high-speed mode

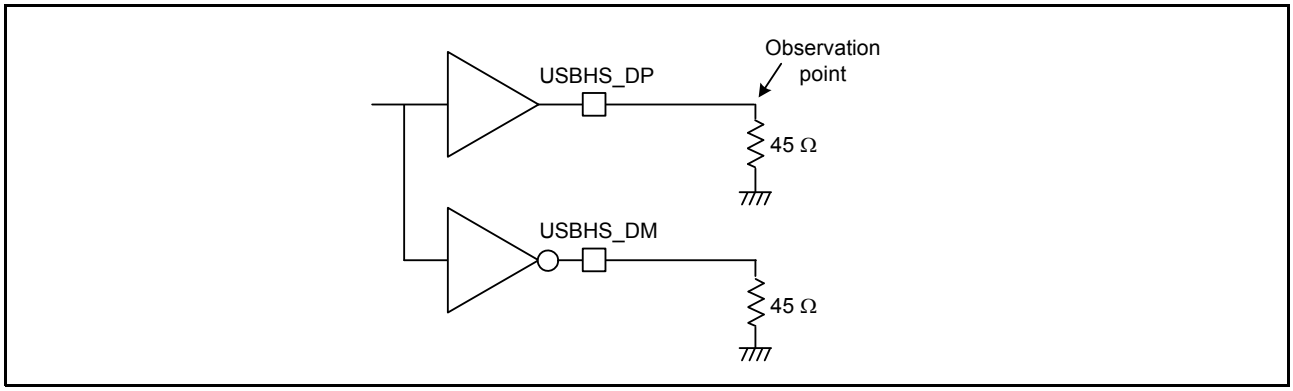
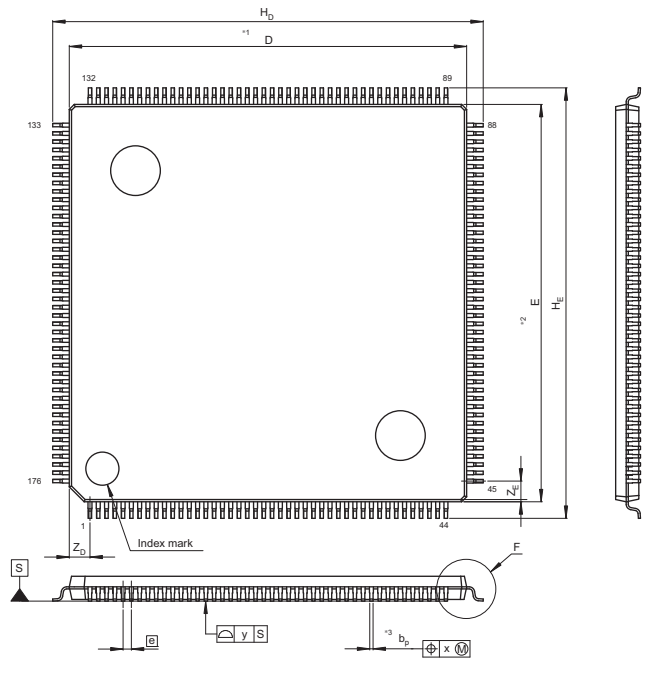


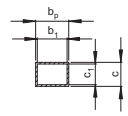
Figure 2.82 Test circuit in high-speed mode

Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 20/24 MHz

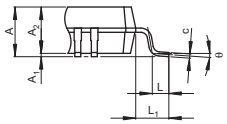
Item		Symbol	Min	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	175	μA	-
	D– sink current	I_{DM_SINK}	25	175	μA	-
	DCD source current	I_{DP_SRC}	7	13	μA	-
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
	D– source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





Terminal cross section



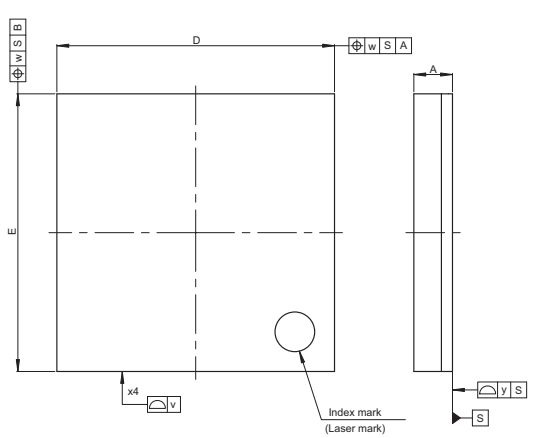
Detail F

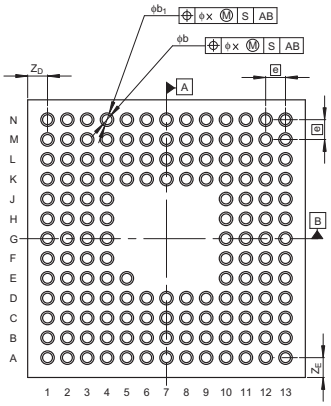
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 1.3 176-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.4 145-pin LGA

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.