Renesas Electronics America Inc - R5F521A6BDFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x24b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdfm-30

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating temperature
RX21A	R5F521A8BDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F521A8BDFN	PLQP0080KB-A					
	R5F521A8BDFM	PLQP0064KB-A					
	R5F521A8BDLJ	PTLG0100JA-A					
	R5F521A7BDFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BDFN	PLQP0080KB-A					
	R5F521A7BDFM	PLQP0064KB-A					
	R5F521A7BDLJ	PTLG0100JA-A					
	R5F521A6BDFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BDFN	PLQP0080KB-A					
	R5F521A6BDFM	PLQP0064KB-A					
	R5F521A6BDLJ	PTLG0100JA-A					
	R5F521A8BGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +105°C *1, *2
	R5F521A8BGFN	PLQP0080KB-A					
	R5F521A8BGFM	PLQP0064KB-A					
	R5F521A7BGFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BGFN	PLQP0080KB-A					
	R5F521A7BGFM	PLQP0064KB-A					
	R5F521A6BGFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BGFN	PLQP0080KB-A					
	R5F521A6BGFM	PLQP0064KB-A					

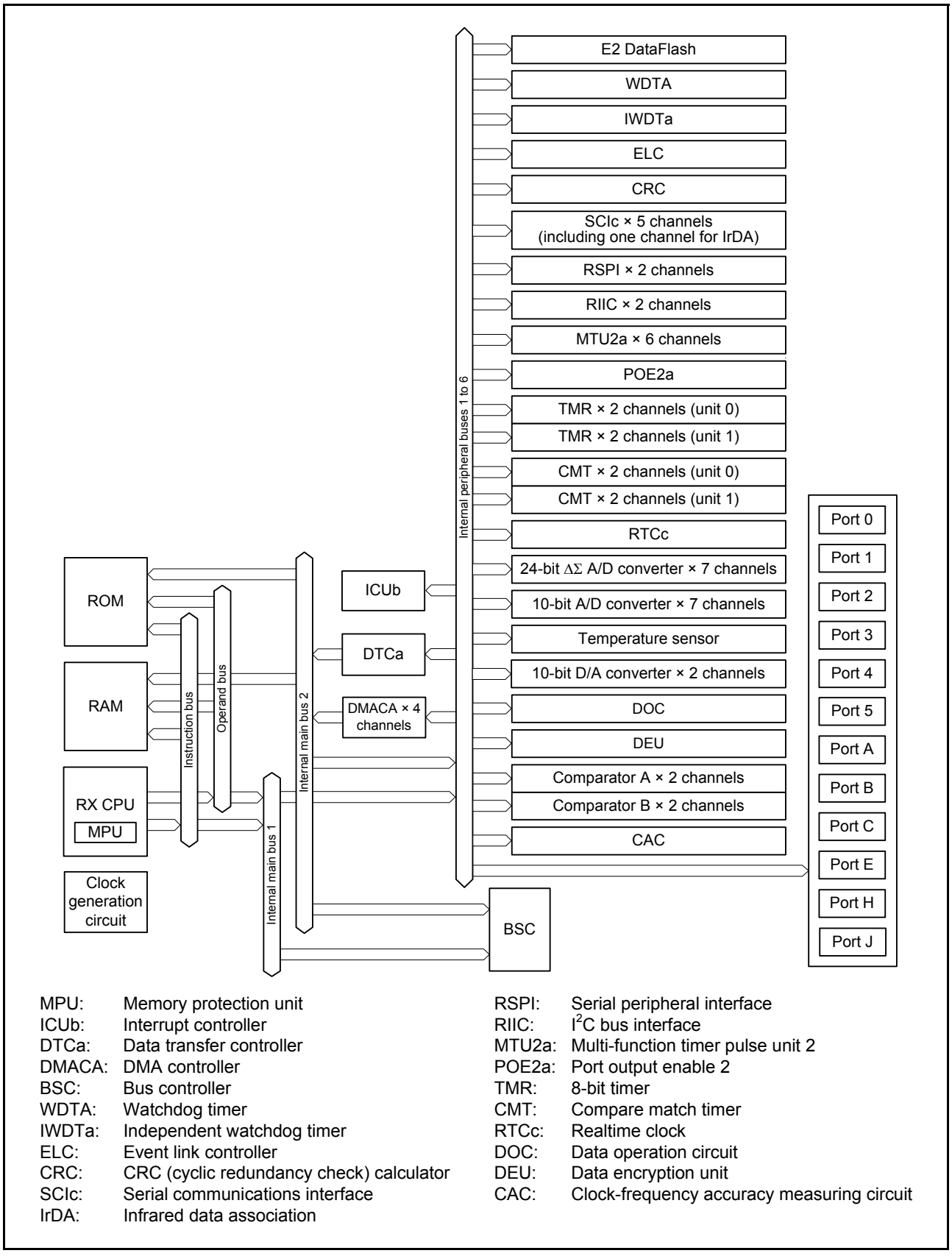
Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 2. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
section 37.3, Using the Temperature Sensor
section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

1.3 Block Diagram

Figure 1.2 shows a block diagram (100-pin package).



MPU: Memory protection unit
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIc: Serial communications interface
IrDA: Infrared data association

RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
DEU: Data encryption unit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram (100-Pin Package)

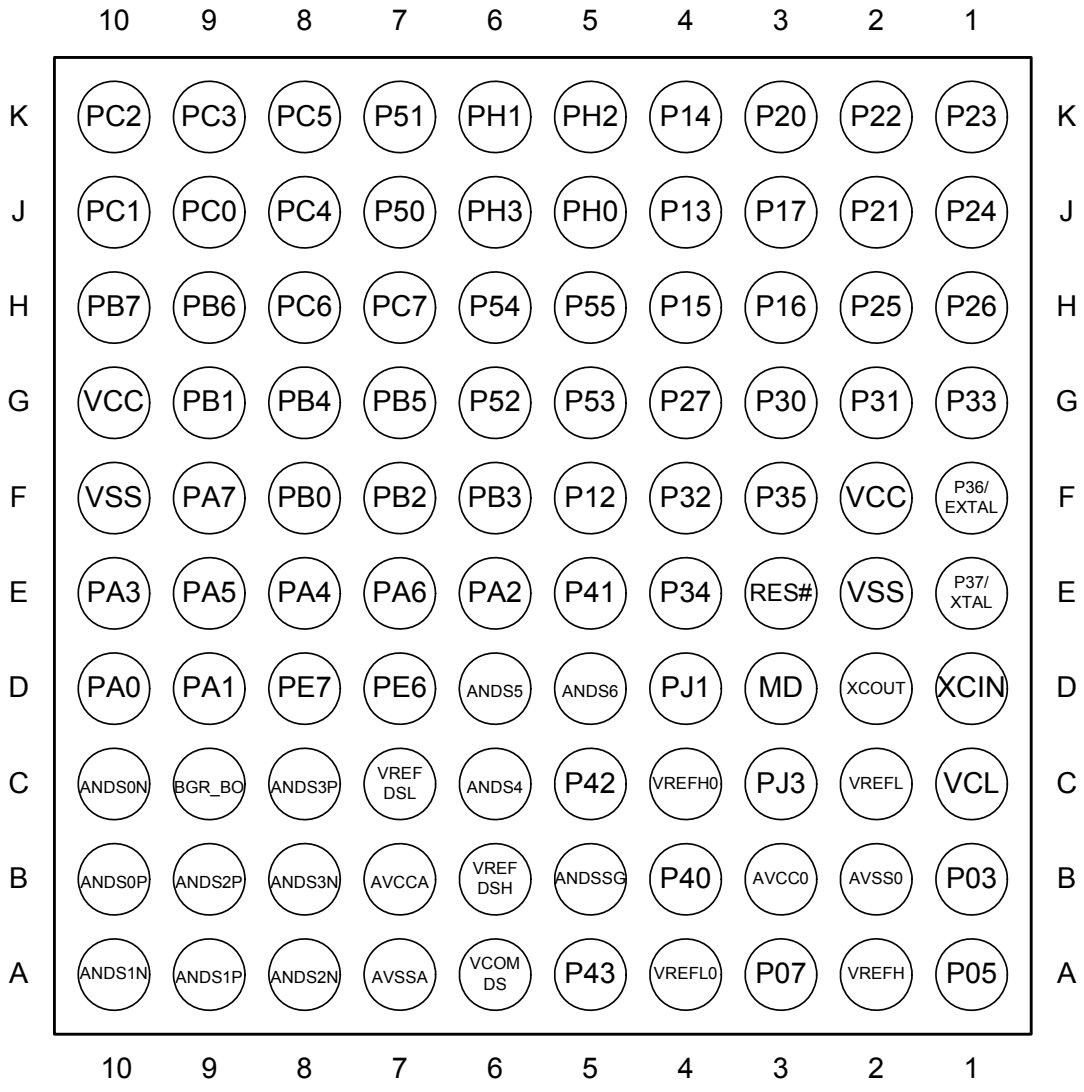
Table 1.4 Pin Functions (2 / 3)

Classifications	Pin Name	I/O	Description
Serial communications interface	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data
	TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmission of data
	SS1#, SS5#, SS6#, SS8#, SS9#	Input	Chip-select input pins
	• IrDA Interface		
	IRTXD5	Output	Data output pin in the IrDA format
	IRRXD5	Input	Data input pin in the IrDA format
I^2C bus interface	SCL0, SCL1	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open-drain output.
	SDA0, SDA1	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open-drain output.
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pin for the RSPI.
	MOSIA, MOSIB	I/O	Input or output data output from the master for the RSPI.
	MISOA, MISOB	I/O	Input or output data output from the slave for the RSPI.
	SSLA0, SSLB0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins to select the slave for the RSPI.
24-bit ΔΣ A/D converter	ANDS0N to ANDS3N, ANDS0P to ANDS3P	Input	Analog differential input pins for the ΔΣ A/D converter
	ANDS4 to ANDS6	Input	Analog single-ended input pins for the ΔΣ A/D converter
	ANDSSG	Input	Common signal ground pin for the analog single-ended inputs (ANDS4 to ANDS6) for the ΔΣ A/D converter
10-bit A/D converter	AN0 to AN6	Input	Input pin for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signals that start the A/D conversion.
D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter.

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

RX21A Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DMAC or DTC).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 001Ch	SYSTEM	Module stop control register D	MSTPCRD	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8		2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32		1 ICLK
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32		1 ICLK
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32		1 ICLK
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32		1 ICLK
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32		1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32		1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32		1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32		1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32		1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32		1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32		1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16		1 ICLK
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16		1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32		1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32		1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8		2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8		2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8		2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8		2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8		2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8		2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8		2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8		2 ICLK
0008 7020h	ICU	Interrupt request register 032	IR032	8	8		2 ICLK
0008 7021h	ICU	Interrupt request register 033	IR033	8	8		2 ICLK
0008 7022h	ICU	Interrupt request register 034	IR034	8	8		2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8		2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8		2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8		2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8		2 ICLK
0008 7030h	ICU	Interrupt request register 048	IR048	8	8		2 ICLK
0008 7031h	ICU	Interrupt request register 049	IR049	8	8		2 ICLK
0008 7032h	ICU	Interrupt request register 050	IR050	8	8		2 ICLK
0008 7033h	ICU	Interrupt request register 051	IR051	8	8		2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8		2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8		2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8		2 ICLK
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8		2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8		2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8		2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8		2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8		2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8		2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8		2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8		2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8		2 ICLK
0008 7058h	ICU	Interrupt request register 088	IR088	8	8		2 ICLK
0008 7059h	ICU	Interrupt request register 089	IR089	8	8		2 ICLK
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8		2 ICLK
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8		2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 70CFh	ICU	Interrupt request register 207	IR207	8	8		2 ICLK
0008 70D0h	ICU	Interrupt request register 208	IR208	8	8		2 ICLK
0008 70D1h	ICU	Interrupt request register 209	IR209	8	8		2 ICLK
0008 70D2h	ICU	Interrupt request register 210	IR210	8	8		2 ICLK
0008 70D3h	ICU	Interrupt request register 211	IR211	8	8		2 ICLK
0008 70D4h	ICU	Interrupt request register 212	IR212	8	8		2 ICLK
0008 70D5h	ICU	Interrupt request register 213	IR213	8	8		2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8		2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8		2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8		2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8		2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8		2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8		2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8		2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8		2 ICLK
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8		2 ICLK
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8		2 ICLK
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8		2 ICLK
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8		2 ICLK
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8		2 ICLK
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8		2 ICLK
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8		2 ICLK
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8		2 ICLK
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8		2 ICLK
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8		2 ICLK
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8		2 ICLK
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8		2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8		2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8		2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8		2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8		2 ICLK
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8		2 ICLK
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8		2 ICLK
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8		2 ICLK
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8		2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8		2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8		2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8		2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8		2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8		2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8		2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8		2 ICLK
0008 7131h	ICU	DTC activation enable register 049	DTCER049	8	8		2 ICLK
0008 7132h	ICU	DTC activation enable register 050	DTCER050	8	8		2 ICLK
0008 713Ah	ICU	DTC activation enable register 058	DTCER058	8	8		2 ICLK
0008 713Bh	ICU	DTC activation enable register 059	DTCER059	8	8		2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8		2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8		2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8		2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8		2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8		2 ICLK

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	20	µA	
			T_a = 55°C		12	41		
			T_a = 85°C		18	113		
			T_a = 105°C		29	233		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.7	7.9		
			T_a = 55°C		2.7	25		
			T_a = 85°C		7.0	86		
			T_a = 105°C		16	189		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled	T_a = 25°C		0.3	0.8		
			T_a = 55°C		0.4	1.1		
			T_a = 85°C		0.8	2.2		
			T_a = 105°C		1.3	4.7		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.2	—		
	Increment for RTC operation (low CL)				0.6	—		
	Increment for RTC operation (standard CL)				1.4	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

Table 5.22 Operation Frequency Value (Medium-Speed Operating Mode 2A)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	12.5	25	MHz
	FlashIF clock (FCLK)*1		12.5	25	
	Peripheral module clock (PCLKA)		12.5	25	
	Peripheral module clock (PCLKB)		12.5	25	
	Peripheral module clock (PCLKC)*2		12.5	25	
	Peripheral module clock (PCLKD)*3		12.5	25	

Note 1. The VCC is 2.7 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.23 Operation Frequency Value (Medium-Speed Operating Mode 2B)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	12.5	25	MHz
	FlashIF clock (FCLK)*1		12.5	25	
	Peripheral module clock (PCLKA)		12.5	25	
	Peripheral module clock (PCLKB)		12.5	25	
	Peripheral module clock (PCLKC)*2		12.5	25	
	Peripheral module clock (PCLKD)*3		12.5	25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.24 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	4	8	MHz
	FlashIF clock (FCLK)*1		4	8	
	Peripheral module clock (PCLKA)		4	8	
	Peripheral module clock (PCLKB)		4	8	
	Peripheral module clock (PCLKC)*2		4	8	
	Peripheral module clock (PCLKD)*3		4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.25 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	
	Peripheral module clock (PCLKA)		32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	
	Peripheral module clock (PCLKC)*2		32.768	32.768	
	Peripheral module clock (PCLKD)*3		32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The A/D converter cannot be used.

5.4.2 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.38
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.

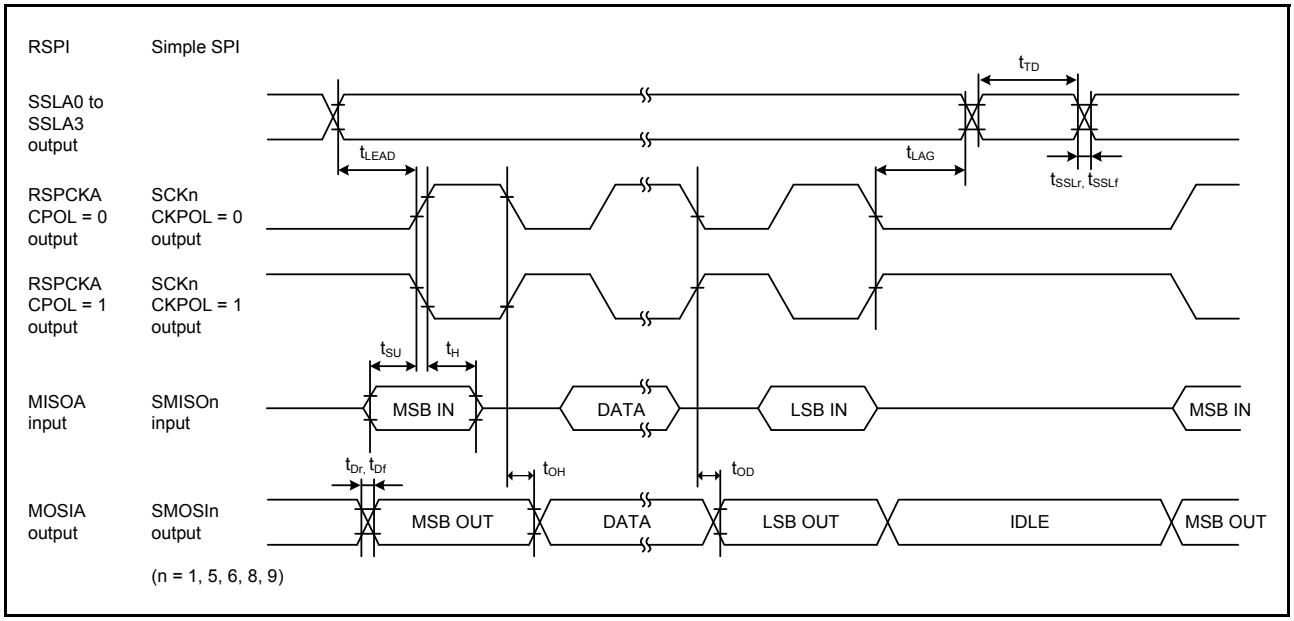


Figure 5.50 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

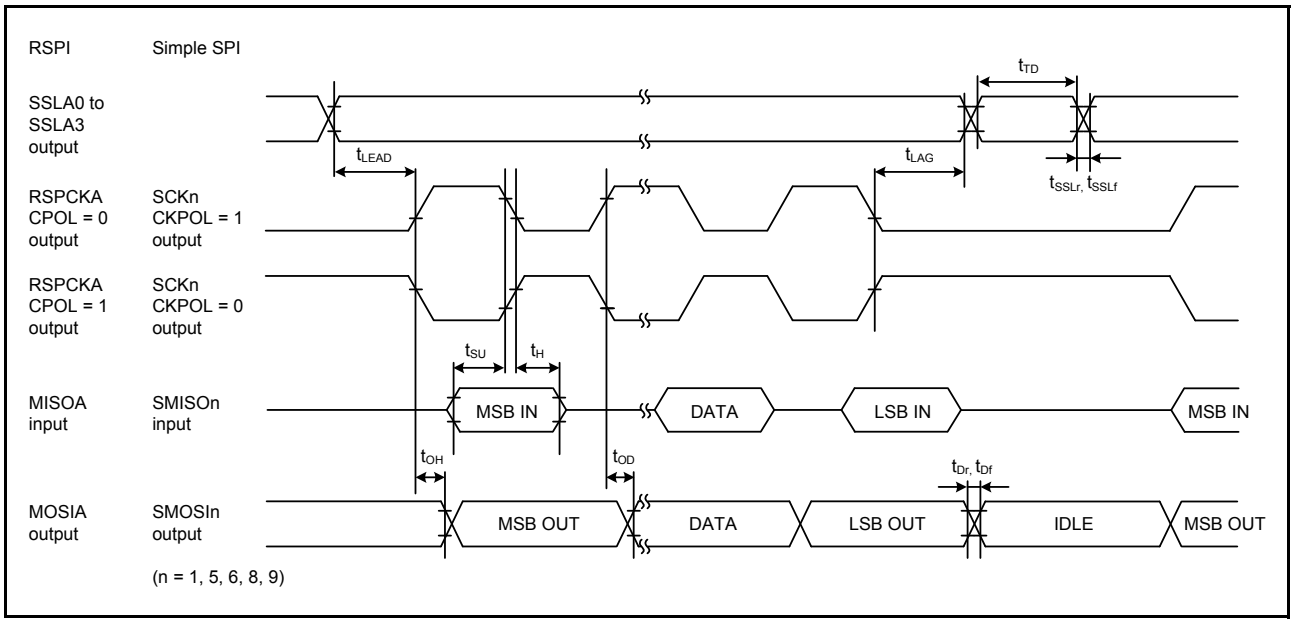


Figure 5.51 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

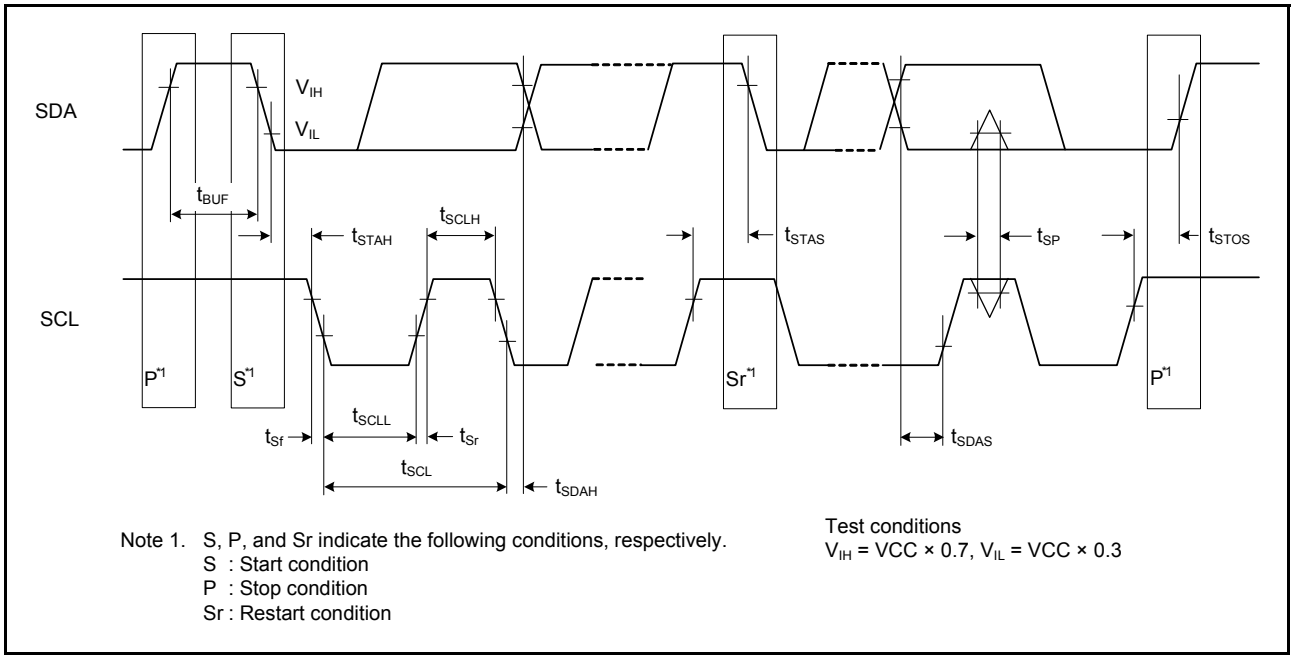


Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

5.8 Temperature Sensor Characteristics

Table 5.42 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCCA = VREFH0 = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	AVCC0 = 3.6		—	13.98	—		PGAGAIN = 10b
Output voltage (@25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.63
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	

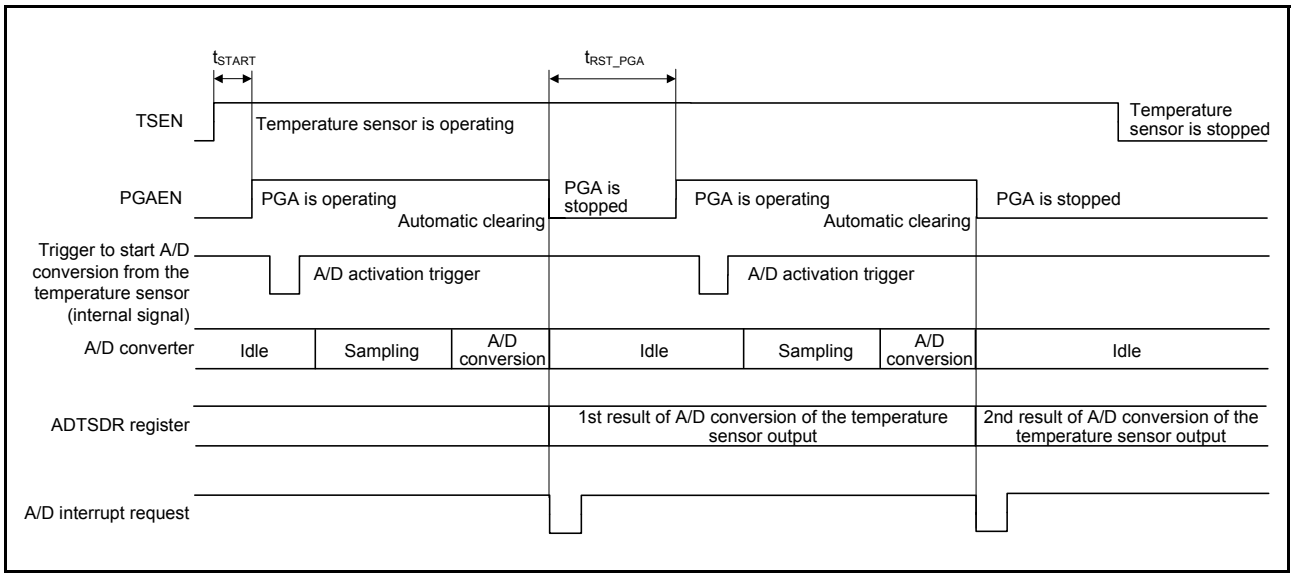


Figure 5.63 A/D Conversion Timing Example of the Temperature Sensor (Two Conversions Performed)

Table 5.52 E2 DataFlash Characteristics (3)
: medium-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

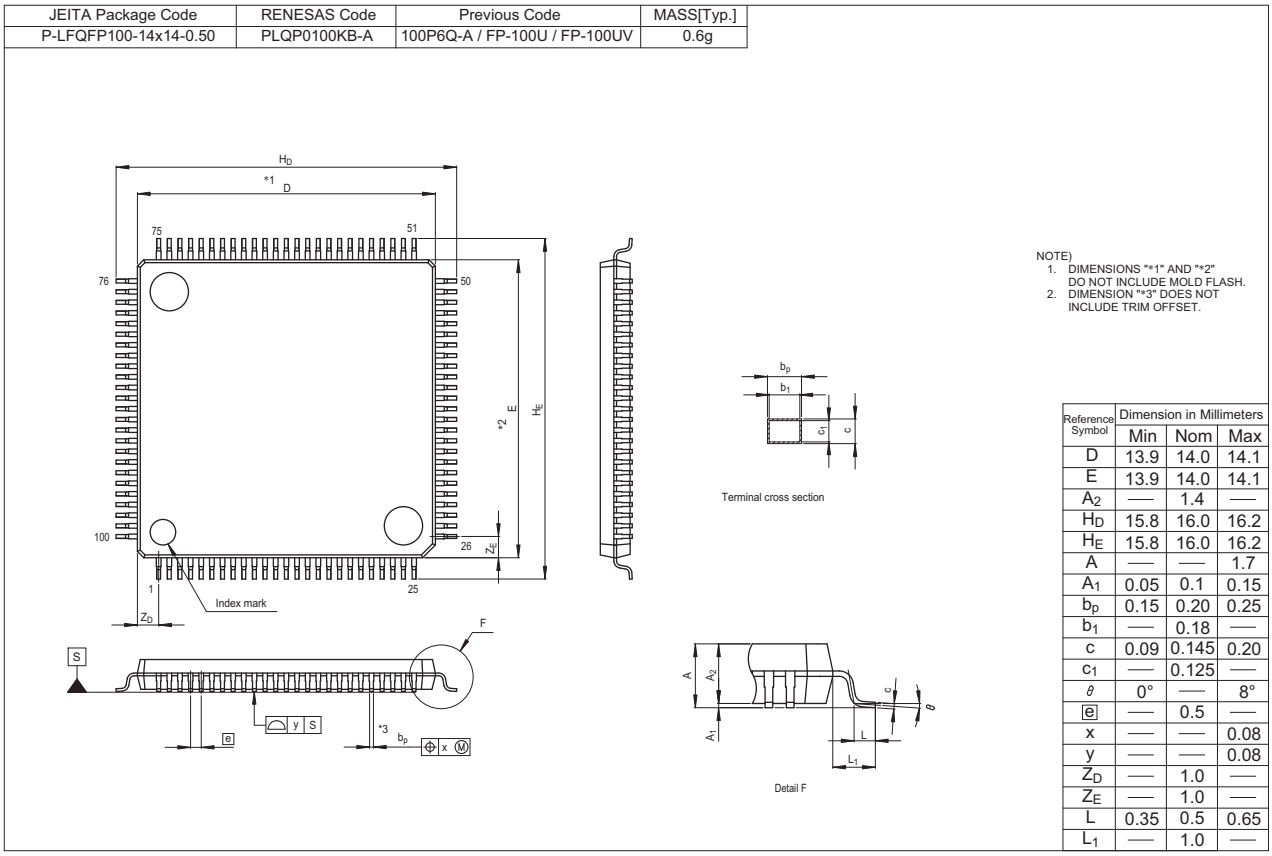
Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.28	5.1	—	0.20	2.9	ms
	8 bytes	t_{DP8}	—	0.32	5.9	—	0.23	3.3	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.36	7.6	—	0.26	4.3	ms
	8 bytes	t_{DP8}	—	0.40	8.8	—	0.28	4.7	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	4.8	32.3	—	4.1	12.8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	5.8	51.4	—	5.0	18.4	ms
Blank check time	2 bytes	t_{DBC2}	—	—	110	—	—	43	µs
	2 Kbytes	t_{DBC2K}	—	—	16.3	—	—	3.1	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	1.7	—	—	1.604	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	1.7	—	—	1.604	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	1.7	—	—	1.604	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	1.7	—	—	1.604	ms

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

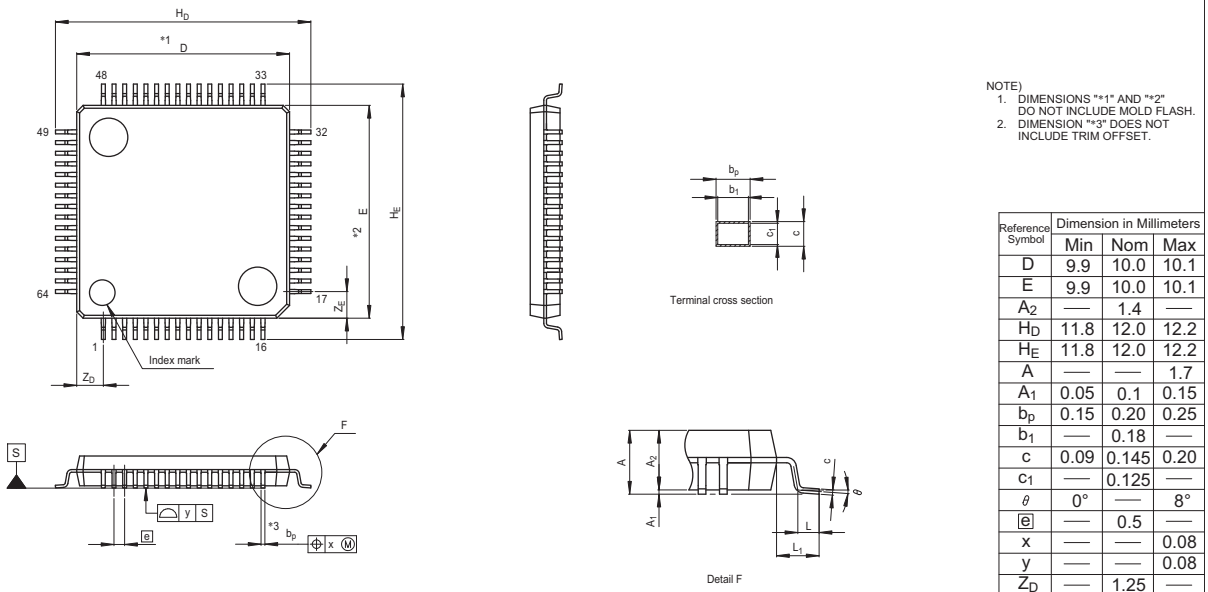
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

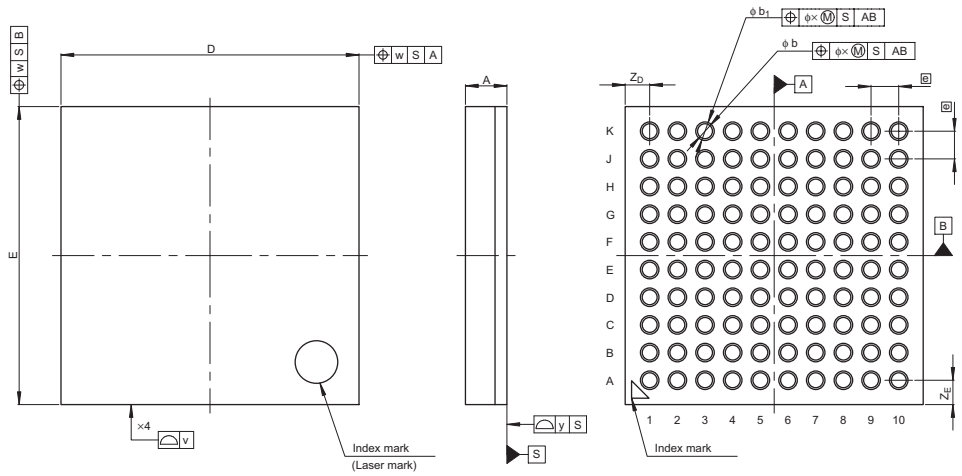


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 64-Pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure D 100-Pin TFLGA (PTLG0100JA-A)