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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

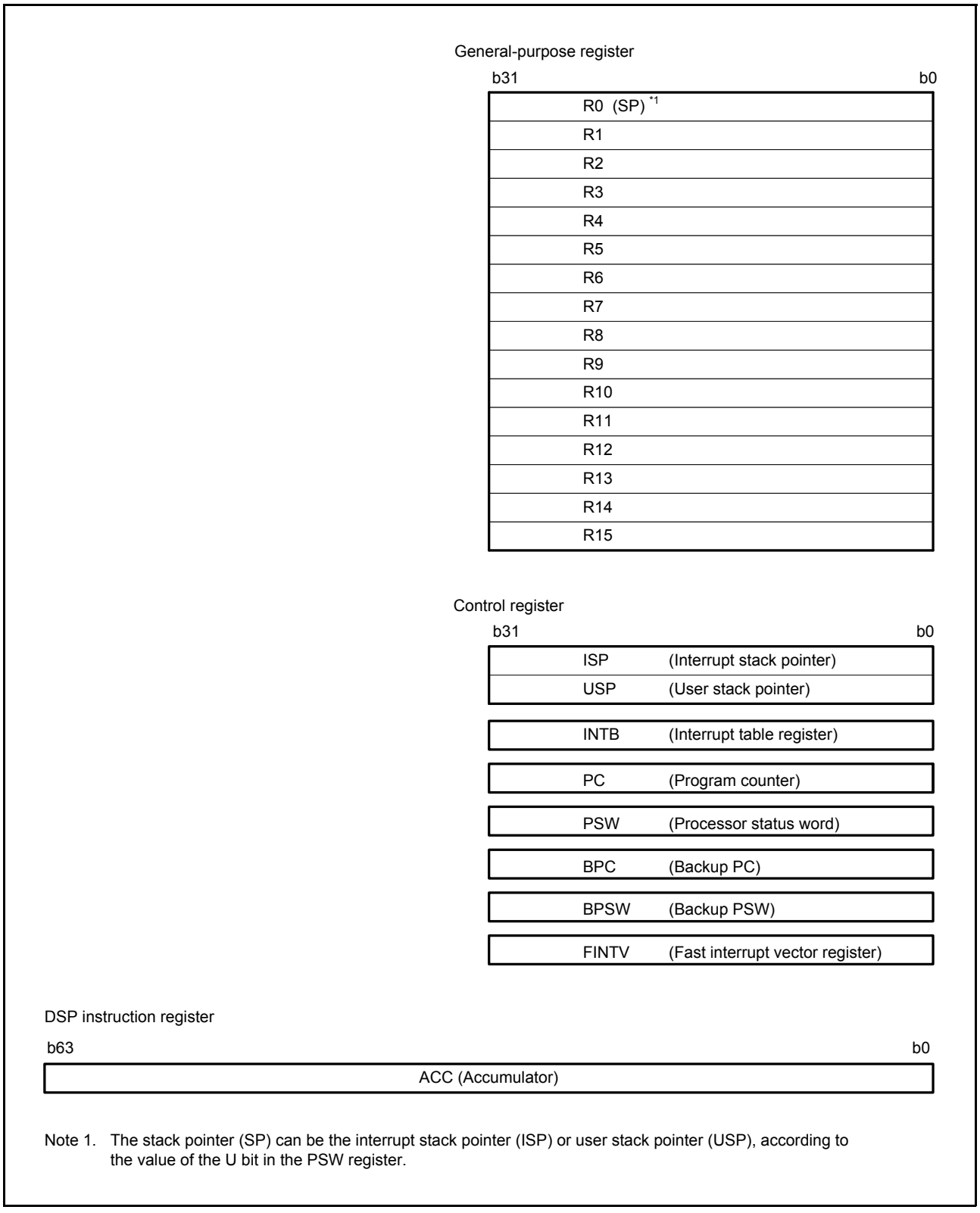
Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x24b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdfm-v0

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
E6		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
E7		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
E8		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
E9		PA5		RSPCKA	
E10		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
F1	EXTAL	P36			
F2	VCC				
F3		P35			NMI
F4		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
F5		P12	TMCI1	SCL0	IRQ2
F6		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
F7		PB2		CTS6#/RTS6#/SS6#	
F8		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
F9		PA7		MISOA	
F10	VSS				
G1		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
G2		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
G3		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS/RTCIC0
G4		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
G5		P53			
G6		P52		SSLB3	
G7		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
G8		PB4		CTS9#/RTS9#/SS9#	
G9		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
G10	VCC				
H1		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB	
H2		P25	MTIOC4C/MTCLKB		ADTRG0#
H3		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
H4		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
H5		P55	MTIOC4D/TMO3		
H6		P54	MTIOC4B/TMCI1		
H7		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
H8		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
J1		P24	MTIOC4A/MTCLKA/TMRI1		

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (3 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32		1 ICLK
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32		1 ICLK
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32		1 ICLK
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32		1 ICLK
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32		1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32		1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32		1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32		1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32		1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32		1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32		1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16		1 ICLK
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16		1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32		1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32		1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8		2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8		2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8		2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8		2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8		2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8		2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8		2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8		2 ICLK
0008 7020h	ICU	Interrupt request register 032	IR032	8	8		2 ICLK
0008 7021h	ICU	Interrupt request register 033	IR033	8	8		2 ICLK
0008 7022h	ICU	Interrupt request register 034	IR034	8	8		2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8		2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8		2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8		2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8		2 ICLK
0008 7030h	ICU	Interrupt request register 048	IR048	8	8		2 ICLK
0008 7031h	ICU	Interrupt request register 049	IR049	8	8		2 ICLK
0008 7032h	ICU	Interrupt request register 050	IR050	8	8		2 ICLK
0008 7033h	ICU	Interrupt request register 051	IR051	8	8		2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8		2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8		2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8		2 ICLK
0008 703Fh	ICU	Interrupt request register 063	IR063	8	8		2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8		2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8		2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8		2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8		2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8		2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8		2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8		2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8		2 ICLK
0008 7058h	ICU	Interrupt request register 088	IR088	8	8		2 ICLK
0008 7059h	ICU	Interrupt request register 089	IR089	8	8		2 ICLK
0008 705Ch	ICU	Interrupt request register 092	IR092	8	8		2 ICLK
0008 705Dh	ICU	Interrupt request register 093	IR093	8	8		2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8320h	RIIC1	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8321h	RIIC1	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8322h	RIIC1	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8323h	RIIC1	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8324h	RIIC1	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8325h	RIIC1	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8326h	RIIC1	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8327h	RIIC1	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8328h	RIIC1	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8329h	RIIC1	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8330h	RIIC1	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8331h	RIIC1	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8332h	RIIC1	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8333h	RIIC1	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK
0008 8724h	MTU0	Timer interrupt enable register 2	TIER2	8	8	2, 3 PCLKB	2 ICLK
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (17 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B11Bh	ELC	Event link setting register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ch	ELC	Event link setting register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK
0008 B11Dh	ELC	Event link setting register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK
0008 B11Eh	ELC	Event link setting register 29	ELSR29	8	8	2, 3 PCLKB	2 ICLK
0008 B11Fh	ELC	Event link option setting register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK
0008 B120h	ELC	Event link option setting register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK
0008 B121h	ELC	Event link option setting register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK
0008 B122h	ELC	Event link option setting register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK
0008 B123h	ELC	Port group setting register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK
0008 B124h	ELC	Port group setting register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK
0008 B125h	ELC	Port group control register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK
0008 B126h	ELC	Port group control register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK
0008 B127h	ELC	Port buffer register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK
0008 B128h	ELC	Port buffer register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK
0008 B129h	ELC	Event link port setting register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ah	ELC	Event link port setting register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK
0008 B12Bh	ELC	Event link port setting register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK
0008 B12Ch	ELC	Event link port setting register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK
0008 B12Dh	ELC	Event link software event generation register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK
0008 B130h	ELC	Event link port setting register 30	ELSR30	8	8	2, 3 PCLKB	2 ICLK
0008 B131h	ELC	Event link port setting register 31	ELSR31	8	8	2, 3 PCLKB	2 ICLK
0008 B132h	ELC	Event link port setting register 32	ELSR32	8	8	2, 3 PCLKB	2 ICLK
0008 B133h	ELC	Event link port setting register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK
0008 B134h	ELC	Event link port setting register 34	ELSR34	8	8	2, 3 PCLKB	2 ICLK
0008 B135h	ELC	Event link port setting register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK
0008 B136h	ELC	Event link port setting register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK
0008 B401h	DSAD	ΔΣ A/D reset register	DSADRSTR	8	8	2, 3 PCLKB	2 ICLK
0008 B402h	DSAD	ΔΣ A/D reference control register	DSADRCR	8	8	2, 3 PCLKB	2 ICLK
0008 B403h	DSAD	ΔΣ A/D control expansion register	DSADCER	8	8	2, 3 PCLKB	2 ICLK
0008 B410h	DSAD	ΔΣ A/D control register 0	DSADCR0	8	8	2, 3 PCLKB	2 ICLK
0008 B411h	DSAD	ΔΣ A/D control/status register 0	DSADCSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B412h	DSAD	ΔΣ A/D gain select register 0	DSADGSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B413h	DSAD	ΔΣ A/D overwrite flag register 0	DSADFR0	8	8	2, 3 PCLKB	2 ICLK
0008 B414h	DSAD	ΔΣ A/D data register 0	DSADDR0	32	32	2, 3 PCLKB	2 ICLK
0008 B418h	DSAD	ΔΣ A/D input select register 0	DSADISR0	8	8	2, 3 PCLKB	2 ICLK
0008 B420h	DSAD	ΔΣ A/D control register 1	DSADCR1	8	8	2, 3 PCLKB	2 ICLK
0008 B421h	DSAD	ΔΣ A/D control/status register 1	DSADCSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B422h	DSAD	ΔΣ A/D gain select register 1	DSADGSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B423h	DSAD	ΔΣ A/D overwrite flag register 1	DSADFR1	8	8	2, 3 PCLKB	2 ICLK
0008 B424h	DSAD	ΔΣ A/D data register 1	DSADDR1	32	32	2, 3 PCLKB	2 ICLK
0008 B428h	DSAD	ΔΣ A/D input select register 1	DSADISR1	8	8	2, 3 PCLKB	2 ICLK
0008 B430h	DSAD	ΔΣ A/D control register 2	DSADCR2	8	8	2, 3 PCLKB	2 ICLK
0008 B431h	DSAD	ΔΣ A/D control/status register 2	DSADCSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B432h	DSAD	ΔΣ A/D gain select register 2	DSADGSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B433h	DSAD	ΔΣ A/D overwrite flag register 2	DSADFR2	8	8	2, 3 PCLKB	2 ICLK
0008 B434h	DSAD	ΔΣ A/D data register 2	DSADDR2	32	32	2, 3 PCLKB	2 ICLK
0008 B438h	DSAD	ΔΣ A/D input select register 2	DSADISR2	8	8	2, 3 PCLKB	2 ICLK
0008 B440h	DSAD	ΔΣ A/D control register 3	DSADCR3	8	8	2, 3 PCLKB	2 ICLK
0008 B441h	DSAD	ΔΣ A/D control/status register 3	DSADCSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B442h	DSAD	ΔΣ A/D gain select register 3	DSADGSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B443h	DSAD	ΔΣ A/D overwrite flag register 3	DSADFR3	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
0008 C121h	PORT	Port switching register A	PSRA	8	8	2, 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Input voltage (except for ports for 5 V tolerant*1)	V_{in}	–0.3 to VCC + 0.3*3	V
Input voltage (ports for 5 V tolerant*1)	V_{in}	–0.3 to +6.5	V
Reference power supply voltage	VREFH, VREFH0	–0.3 to VCC + 0.3*3	V
Analog power supply voltage	AVCC0, AVCCA, BGR_BO*2	–0.3 to +6.5	V
A/D converter analog input voltage	V_{AN}	–0.3 to VCC + 0.3*3	V
ΔΣ A/D converter analog input voltage	V_{ANDS}	–0.6 to VCC + 0.3*3	V
Operating temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, the AVCCA and AVSSA pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 0.1 µF (±20% accuracy) capacitor. The capacitor must be placed as close to the pin as possible.

Note 1. Ports 12, 13, 16, 17, 20, and 21 are 5 V tolerant.

Note 2. Set AVCC0 and AVCCA to the same potential as VCC. When neither the A/D converter, the D/A converter, nor ΔΣ A/D converter is in use, do not leave the AVCC0, VREFH, AVCCA, VREFH0, AVSS0, VREFL, AVSSA, and VREFL0 pins open. Connect the AVCC0, VREFH, AVCCA, and VREFH0 pins to VCC, and the AVSS0, VREFL, AVSSA, and VREFL0 pins to VSS, respectively.

Note 3. The maximum value is 6.5 V.

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*6	ICLK = 8 MHz	I_{CC}	1.9	—	mA	
				ICLK = 4 MHz		1.2	—		
			All peripheral operation: Normal*7	ICLK = 8 MHz		2.5	—		
				ICLK = 4 MHz		1.7	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.3	—		
				ICLK = 4 MHz		0.9	—		
			All peripheral operation: Normal	ICLK = 8 MHz		1.9	—		
				ICLK = 4 MHz		1.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.1	—		
				ICLK = 4 MHz		0.9	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.027	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.030	—		
			All peripheral operation: Max.*11	ICLK = 32 kHz		—	1.0		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.025	—		
		All-module clock stop mode		ICLK = 32 kHz		0.022	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are ICLK divided by 1.
Note 6. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are ICLK divided by 1.

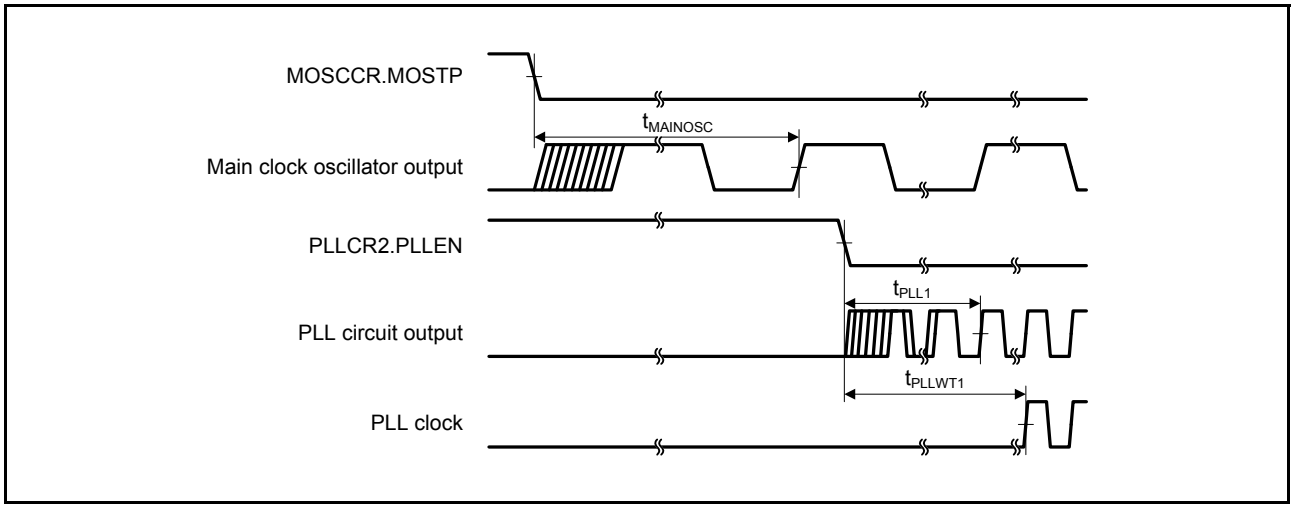


Figure 5.31 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

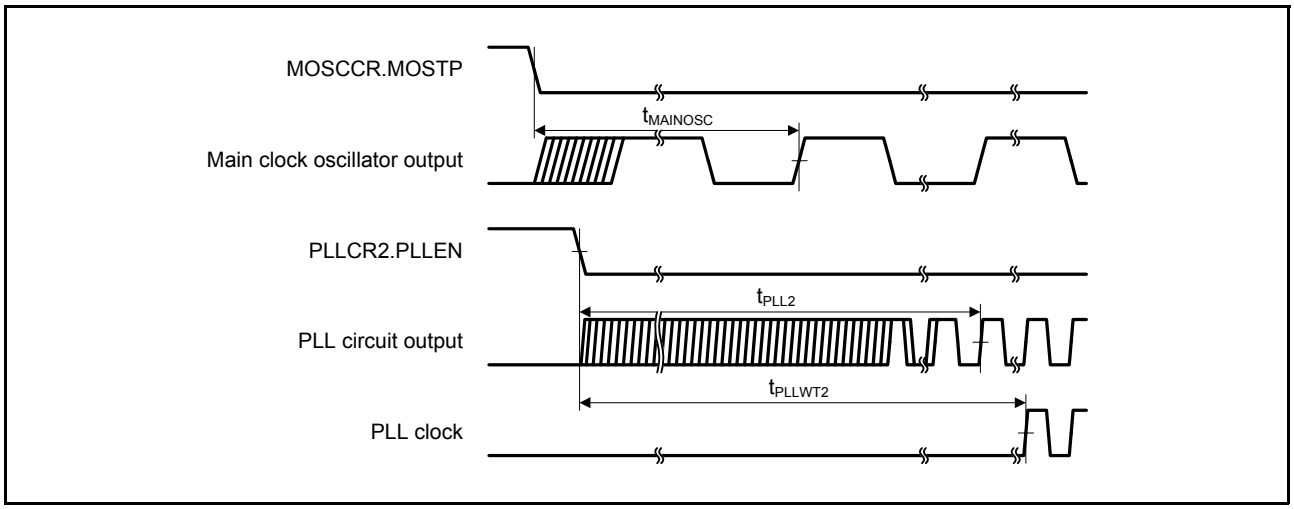


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

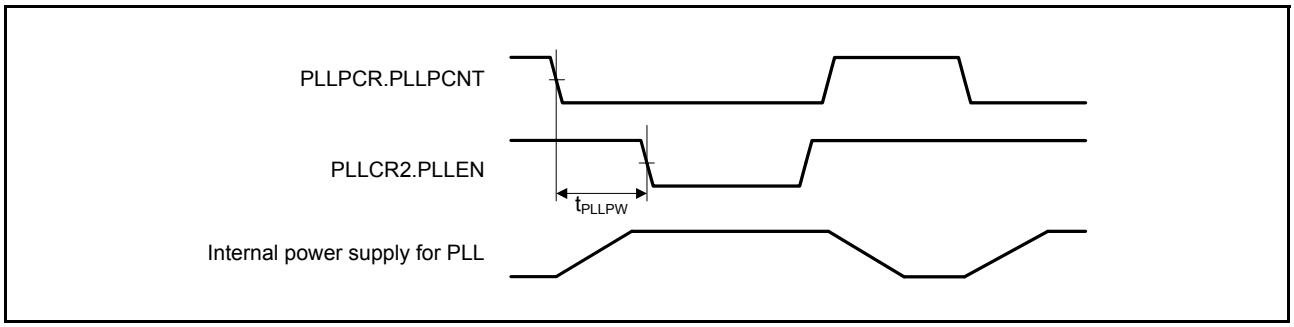


Figure 5.33 PLL Power Control Timing

Table 5.35 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.54
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	Figure 5.54
	SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

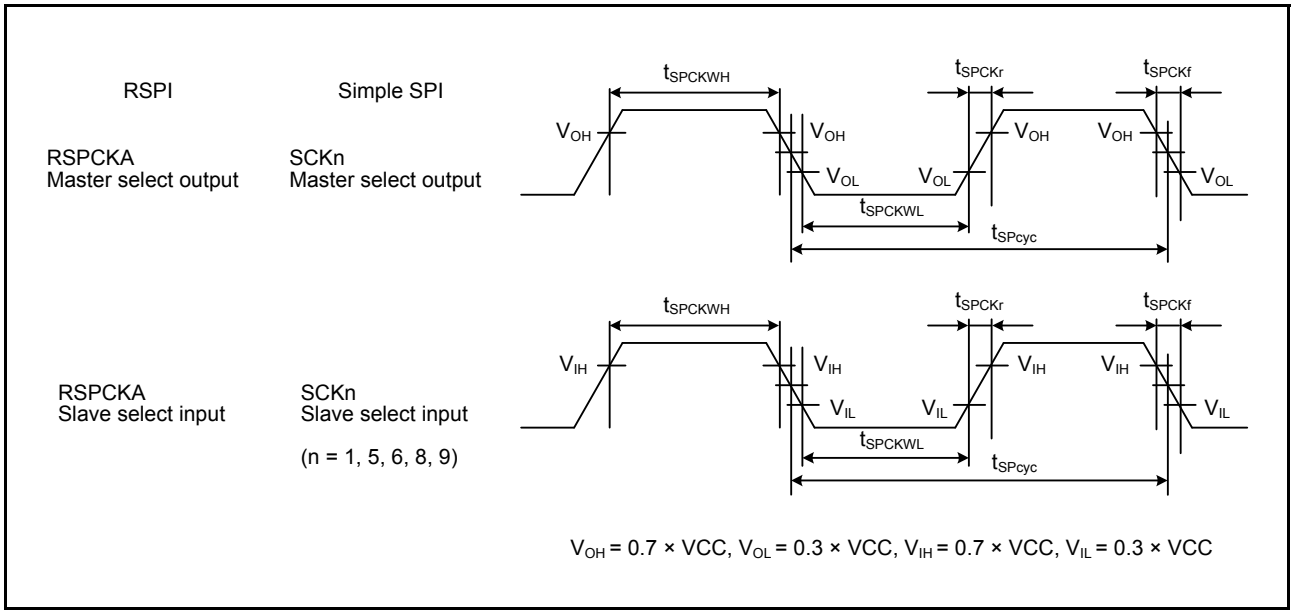


Figure 5.49 RSPI Clock Timing and Simple SPI Clock Timing

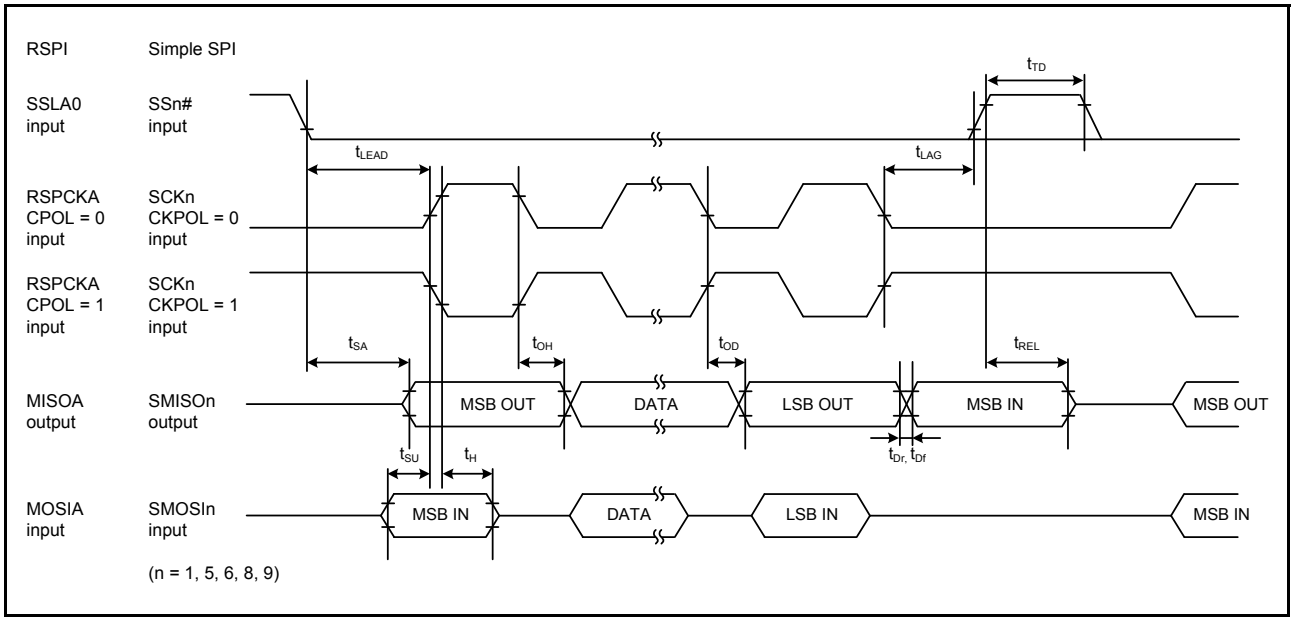


Figure 5.52 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

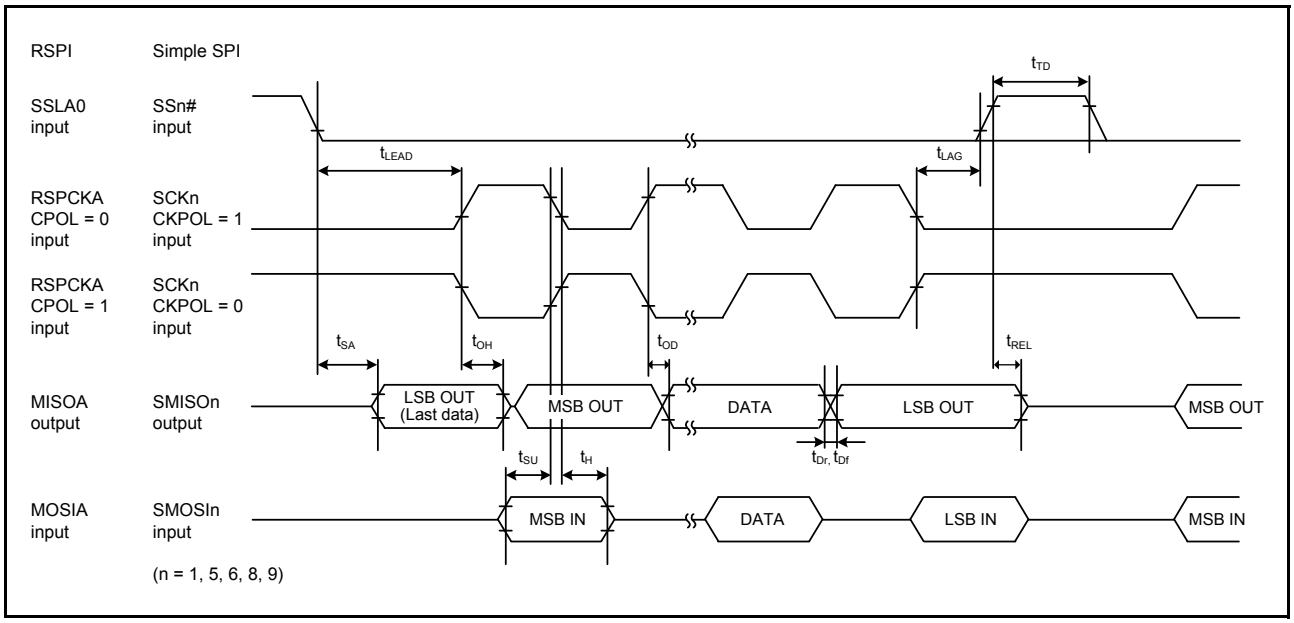


Figure 5.53 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

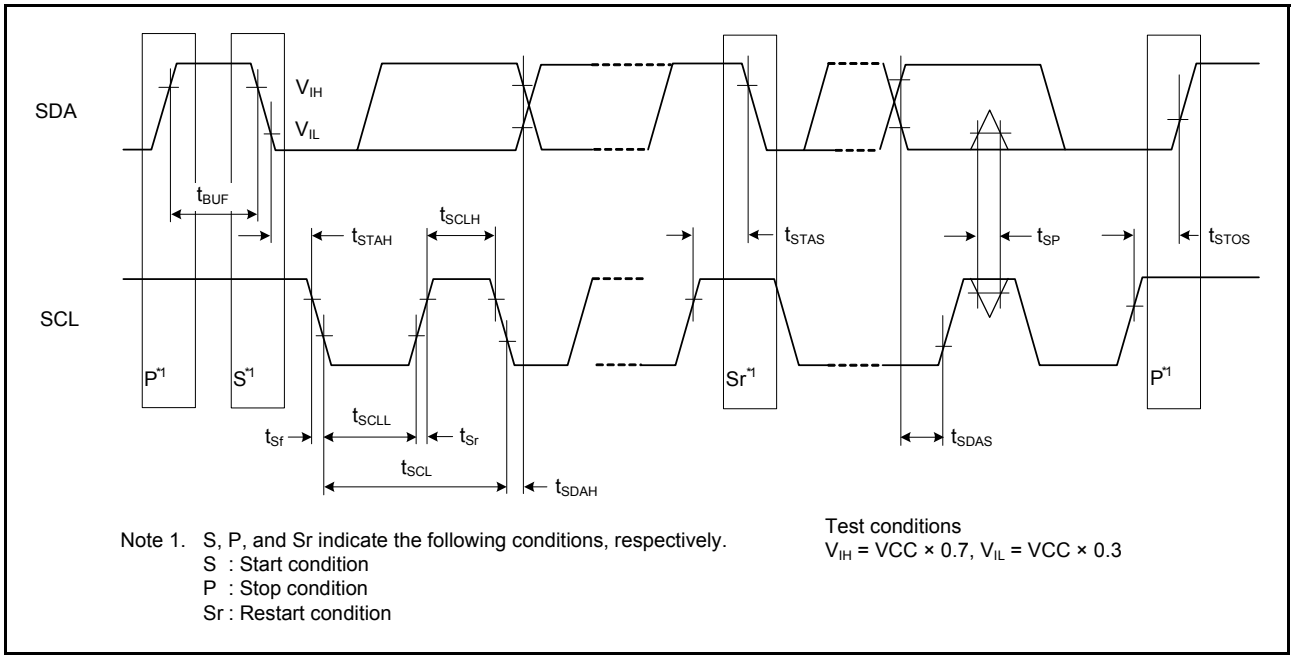


Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.45 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_7}	2.95	3.10	3.25	V	Figure 5.68
		V_{det2_8}	2.85	2.95	3.05		At falling edge VCC
		V_{det2_9}	2.70	2.80	2.90		
		V_{det2_A}	2.55	2.65	2.75		
		V_{det2_B}	2.40	2.50	2.60		
		V_{det2_C}	2.25	2.35	2.45		
		V_{det2_D}	2.10	2.20	2.30		
		V_{det2_E}	1.95	2.05	2.15		
		V_{det2_F}	1.80	1.90	2.00		
		V_{CMPA2}	1.18	1.33	1.48		EXVCCINP2 = 1
Internal reset time	Power-on reset time	t_{POR}	—	9	—	ms	Figure 5.65
	Voltage monitoring 0 reset time	t_{LVD0}	—	9	—		Figure 5.66
	Voltage monitoring 1 reset time	t_{LVD1}	—	1.4	—		Figure 5.67
	Voltage monitoring 2 reset time	t_{LVD2}	—	1.4	—		Figure 5.68
Minimum VCC down time*2		t_{VOFF}	200	—	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	200	µs	Figure 5.65
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	15	µs	Figure 5.67 and Figure 5.68
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.65 VCC = 0.9 V or lower
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_7.
			—	50	—		When selection is from among VdetX_8 to F.

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/ LVD.

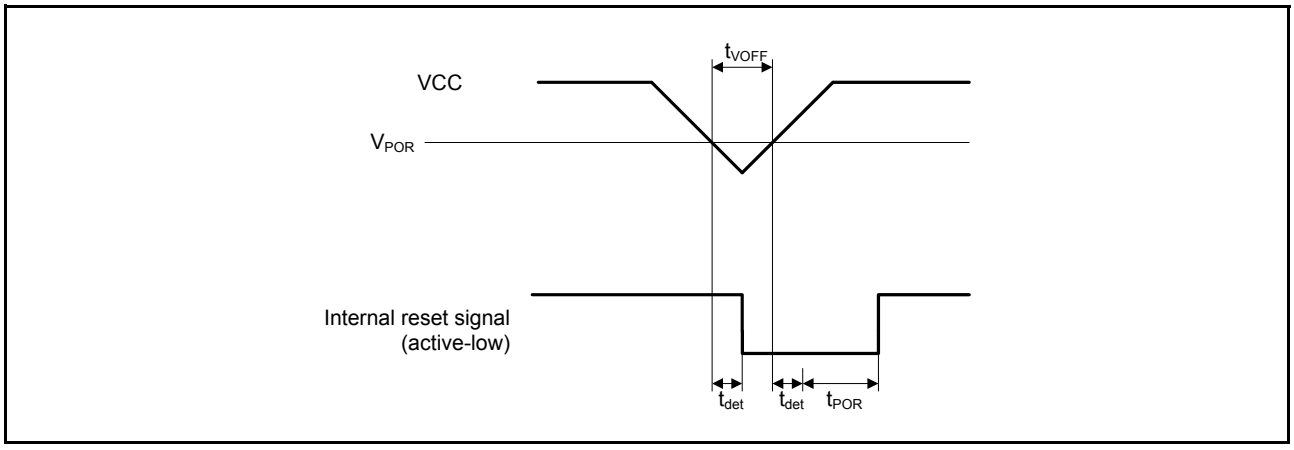


Figure 5.64 Voltage Detection Reset Timing

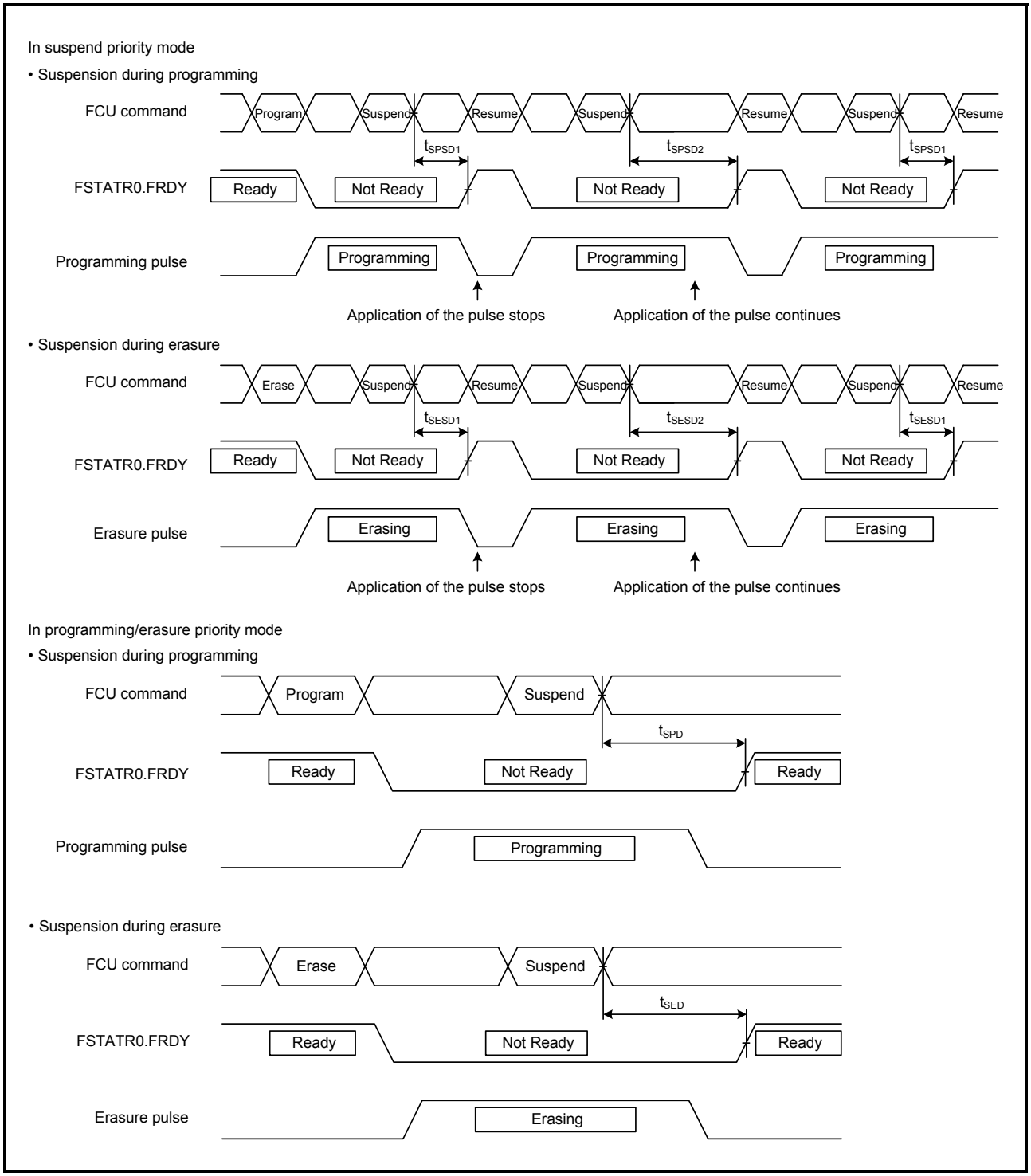
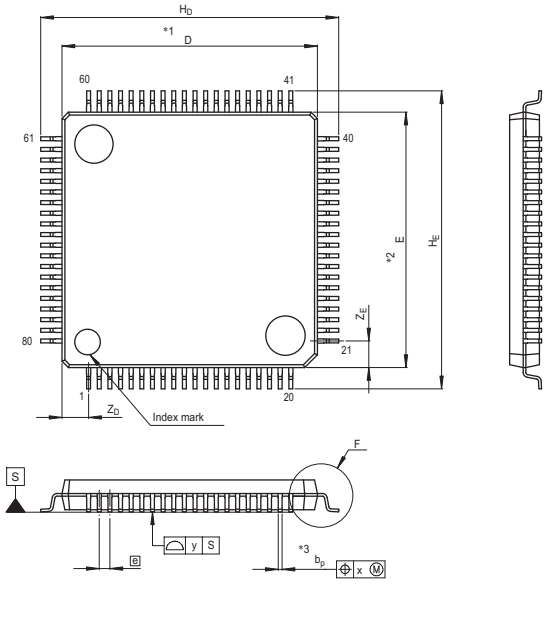


Figure 5.70 Flash Memory Program/Erase Suspend Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g

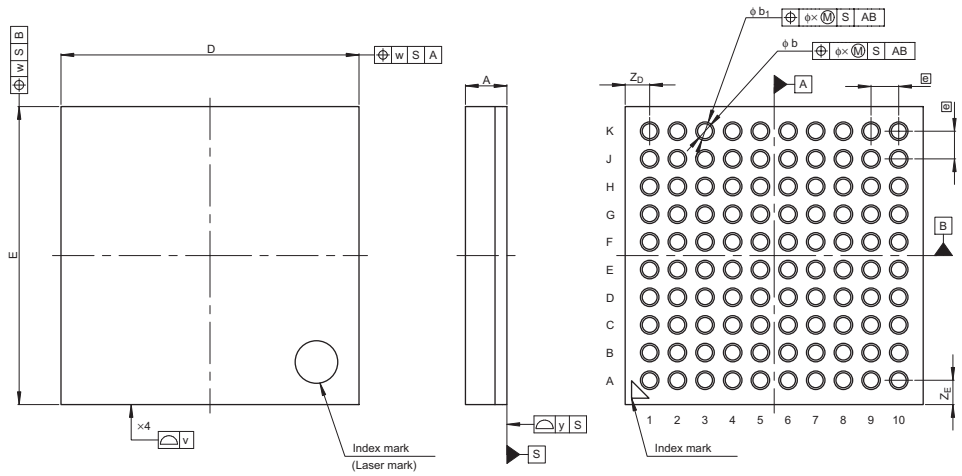


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 80-Pin LQFP (PLQP0080KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure D 100-Pin TFLGA (PTLG0100JA-A)

REVISION HISTORY	RX21A Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 24, 2012	—	First edition, issued