# Renesas Electronics America Inc - R5F521A6BDFN#V0 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 4x24b, 7x10b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdfn-v0 |

**Table 1.1 Outline of Specifications (2 / 4)**

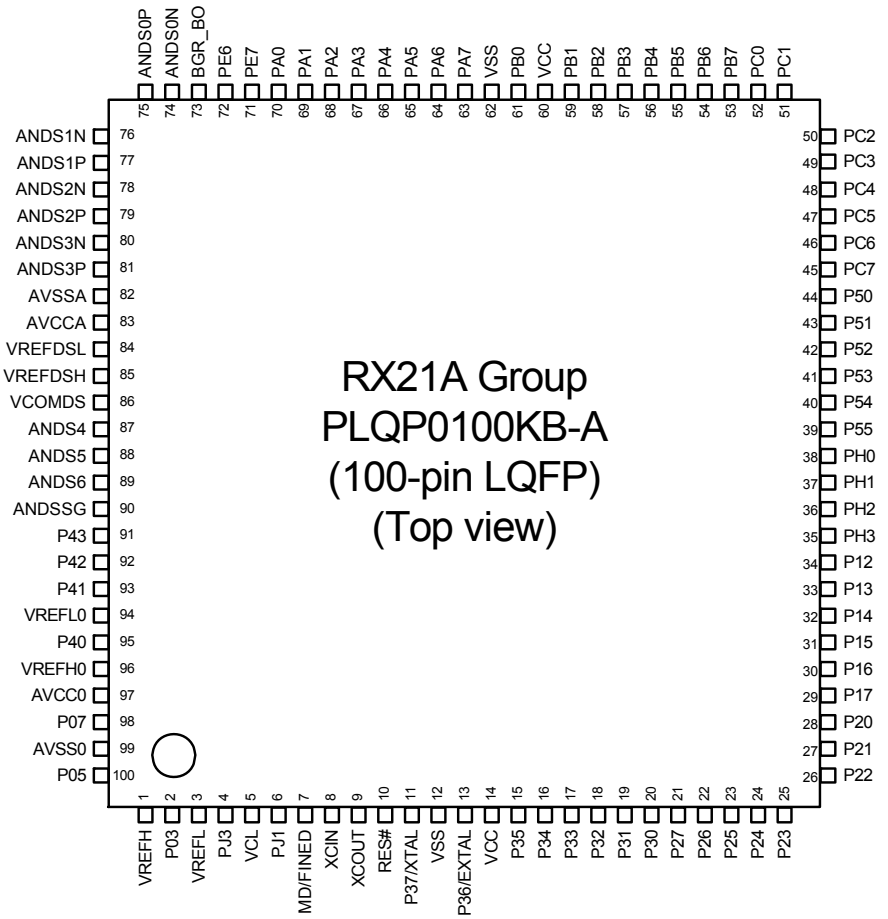
| Classification | Module/Function | Description |
|---|---|---|
| DMA | DMA controller (DMACA) | • 4 channels<br>• Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | Data transfer controller (DTCa) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Interrupts<br>• Chain transfer function |
| I/O ports | General I/O ports | 100-pin/80-pin/64-pin<br>• I/O pin: 66/51/38<br>• Input: 1/1/1<br>• Pull-up resistors: 66/51/38<br>• Open-drain outputs: 47/37/28<br>• 5-V tolerance: 6/6/2 |
| Event link controller (ELC) | | • Event signals of 69 types can be directly connected to the module<br>• Operations of timer modules are selectable at event input<br>• Capable of event link operation for ports B and E |
| Multi-function pin controller (MPC) | | • Capable of selecting input/output function from multiple pins |
| Timers | Multi-function timer pulse unit 2 (MTU2a) | • (16 bits x 6 channels) x 1 unit<br>• Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels.<br>• Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>• Input capture function<br>• 21 output compare/input capture registers<br>• Pulse output mode<br>• Complementary PWM output mode<br>• Reset synchronous PWM mode<br>• Phase-counting mode<br>• Generation of triggers for A/D converter conversion |
| | Port output enable2 (POE2a) | Controls the high-impedance state of the MTU's waveform output pins |
| | 8-bit timer (TMR) | • (8 bits x 2 channels) x 2 units<br>• Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal<br>• Capable of output of pulse trains with desired duty cycles or of PWM signals<br>• The 2 channels of each unit can be cascaded to create a 16-bit timer<br>• Capable of generating baud-rate clocks for SCI5 and SCI6 |
| | Compare match timer (CMT) | • (16 bits x 2 channels) x 2 units<br>• Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Watchdog timer (WDTA) | • 14 bits x 1 channel<br>• Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192) |
| | Independent watchdog timer (IWDTa) | • 14 bits x 1 channel<br>• Counter-input clock: IWDT-dedicated on-chip oscillator<br>Frequency divided by 1, 16, 32, 64, 128, or 256 |
| | Realtime clock (RTCc) | • Clock source: Sub-clock<br>• Time count or 32-bit binary count in second units basis selectable<br>• Time/calendar<br>• Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt<br>• Time-capture facility for three values |

**Table 1.1 Outline of Specifications (3 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Serial communications interfaces (SCIc) | • 5 channels (channel 1, 5, 6, 8, 9) (including one channel for IrDA)<br>• Serial communications modes:<br>Asynchronous, clock synchronous, and smart-card interface<br>• On-chip baud rate generator allows selection of the desired bit rate<br>• Choice of LSB-first or MSB-first transfer<br>• Average transfer rate clock can be input from TMR timers (SCI5 and SCI6)<br>• Simple IIC<br>• Simple SPI |
| | IrDA interface (IRDA) | • 1 channel (SCI5 is used)<br>• Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0 |
| | $I^2C$ bus interface (RIIC) | • 2 channels<br>• Communications formats:<br>$I^2C$ bus format/SMBus format<br>• Master/slave selectable<br>• Supports the fast mode |
| | Serial peripheral interface (RSPI) | • 2 channels<br>• Transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>• Capable of handling serial transfer as a master or slave<br>• Data formats<br>• Choice of LSB-first or MSB-first transfer<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Double buffers for both transmission and reception |
| 24-bit ΔΣ A/D converter (DSAD) | | • 7 channels: 4-channel differential input for current; 3-channel single-ended input for voltage<br>• x 1 to x 64 PGA for differential input side for current and x 1 to x 4 PGA for single-ended input side for voltage<br>• Minimum conversion time: 81.92 µs (A/D conversion clock: 25 MHz) |
| 10-bit A/D converter (AD) | | • 10 bits (7 channels x 1 unit)<br>• 10-bit resolution<br>• Conversion time: 2.0 µs per channel (A/D conversion clock: 25 MHz)<br>• Operating modes<br>Scan mode (single scan mode and continuous scan mode)<br>• Sample-and-hold function<br>• Self-diagnosis for the A/D converter<br>• Assistance in detecting disconnected analog inputs<br>• A/D conversion start conditions<br>Conversion can be started by software, a conversion start trigger from a timer (MTU), an external trigger signal, a temperature sensor or ELC. |
| Temperature sensor (TEMPSa) | | • Outputs the voltage that changes depending on the temperature<br>• PGA gain switchable: Three levels according to the voltage range |
| D/A converter (DA) | | • 2 channels<br>• 10-bit resolution<br>• Output voltage: 0 V to VREFH |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Data encryption unit (DEU)*1 | | • Encryption and decryption of AES<br>• 128-, 192-, or 256-bit key length<br>• ECB or CBC mode |
| Comparator A (CMPA) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Comparator B (CMPB) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Data operating circuit (DOC) | | Comparison, addition, and subtraction of 16-bit data |
| Power supply voltage/ Operating frequency | | VCC = 1.8 to 3.6 V: 25 MHz, VCC = 2.7 to 3.6 V: 50 MHz |
| Supply current | | 8.6mA@50MHz (typ) |
| Operating temperature | | D version: –40 to +85°C, G version: –40 to +105°C*2, *3 |

## 1.5 Pin Assignments

Figure 1.3 to Figure 1.5 show the pin assignments. Table 1.5 to Table 1.7 show the lists of pins and pin functions.




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LQFP)”.

**Figure 1.3 Pin Assignments of the 100-Pin LQFP**

**Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 1 | VREFH | | | | |
| 2 | | P03 | | | AN4/DA0 |
| 3 | VREFL | | | | |
| 4 | | PJ3 | MTIOC3C | CTS6#/RTS6#/SS6# | |
| 5 | VCL | | | | |
| 6 | | PJ1 | MTIOC3A | | |
| 7 | MD | | | | FINED |
| 8 | XCIN | | | | |
| 9 | XCOUT | | | | |
| 10 | RES# | | | | |
| 11 | XTAL | P37 | | | |
| 12 | VSS | | | | |
| 13 | EXTAL | P36 | | | |
| 14 | VCC | | | | |
| 15 | | P35 | | | NMI |
| 16 | | P34 | MTIOC0A/TMCI3/POE2# | SCK6 | IRQ4 |
| 17 | | P33 | MTIOC0D/TMRI3/POE3# | RXD6/SMISO6/SSCL6 | IRQ3-DS |
| 18 | | P32 | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| 19 | | P31 | MTIOC4D/TMCI2 | CTS1#/RTS1#/SS1#/SSLB0 | IRQ1-DS/RTCIC1 |
| 20 | | P30 | MTIOC4B/TMRI3/POE8# | RXD1/SMISO1/SSCL1/ MISOB | IRQ0-DS/RTCIC0 |
| 21 | | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB | |
| 22 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1/ MOSIB | |
| 23 | | P25 | MTIOC4C/MTCLKB | | ADTRG0# |
| 24 | | P24 | MTIOC4A/MTCLKA/TMRI1 | | |
| 25 | | P23 | MTIOC3D/MTCLKD | | |
| 26 | | P22 | MTIOC3B/MTCLKC/TMO0 | | |
| 27 | | P21 | MTIOC1B/TMCI0 | SCL1 | |
| 28 | | P20 | MTIOC1A/TMRI0 | SDA1 | |
| 29 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA0-DS | IRQ7 |
| 30 | | P16 | MTIOC3C/MTIOC3D/TMO2 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS | IRQ6/RTCOUT/ ADTRG0# |
| 31 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| 32 | | P14 | MTIOC3A/MTCLKA/TMRI2 | CTS1#/RTS1#/SS1# | IRQ4 |
| 33 | | P13 | MTIOC0B/TMO3 | SDA0 | IRQ3 |
| 34 | | P12 | TMCI1 | SCL0 | IRQ2 |
| 35 | | PH3 | TMCI0 | | |
| 36 | | PH2 | TMRI0 | | IRQ1 |
| 37 | | PH1 | TMO0 | | IRQ0 |
| 38 | | PH0 | | | CACREF |
| 39 | | P55 | MTIOC4D/TMO3 | | |
| 40 | | P54 | MTIOC4B/TMCI1 | | |
| 41 | | P53 | | | |

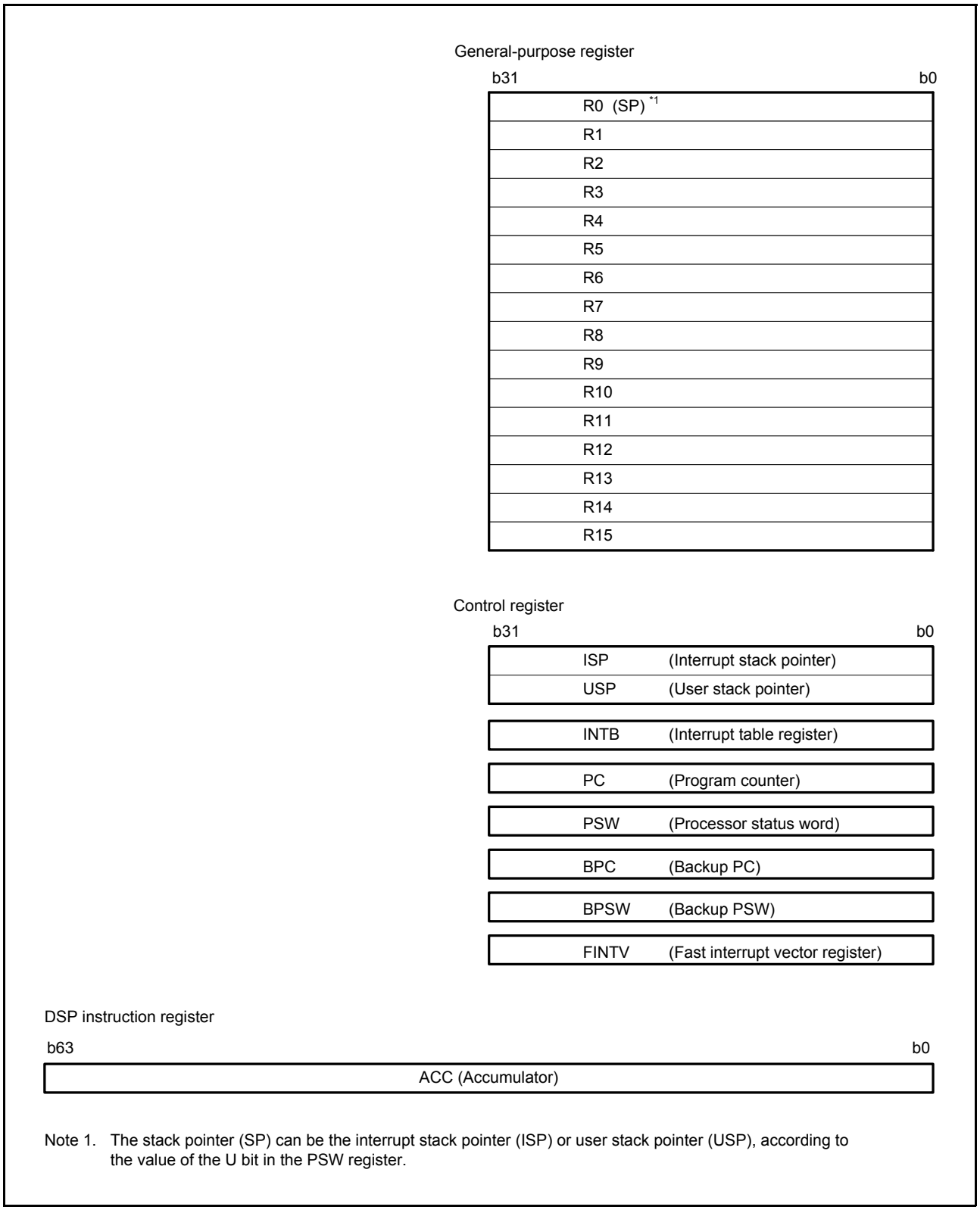
**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 42 | | PB6 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| 43 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| 44 | | PB4 | | CTS9#/RTS9#/SS9# | |
| 45 | | PB3 | MTIOC0A/MTIOC4A/TMO0/ POE3# | SCK6 | |
| 46 | | PB2 | | CTS6#/RTS6#/SS6# | |
| 47 | | PB1 | MTIOC0C/MTIOC4C/TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| 48 | VCC | | | | |
| 49 | | PB0 | MTIC5W | RXD6/SMISO6/SSCL6/RSPCKA | CMPB0 |
| 50 | VSS | | | | |
| 51 | | PA6 | MTIC5V/MTCLKB/TMCI3/ POE2# | CTS5#/RTS5#/SS5#/MOSIA | CVREFB0 |
| 52 | | PA5 | | RSPCKA | |
| 53 | | PA4 | MTIC5U/MTCLKA/TMRI0 | TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0 | IRQ5-DS/CVREFB1 |
| 54 | | PA3 | MTIOC0D/MTCLKD | RXD5/SMISO5/SSCL5/IRRXD5 | IRQ6-DS/CMPB1 |
| 55 | | PA2 | | RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3 | CMPA2 |
| 56 | | PA1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | CVREFA |
| 57 | | PA0 | MTIOC4A | SSLA1 | CACREF/CMPA1 |
| 58 | BGR_BO | | | | |
| 59 | | | | | ANDS0N |
| 60 | | | | | ANDS0P |
| 61 | | | | | ANDS1N |
| 62 | | | | | ANDS1P |
| 63 | AVSSA | | | | |
| 64 | AVCCA | | | | |
| 65 | VREFDSL | | | | |
| 66 | VREFDSH | | | | |
| 67 | VCOMDS | | | | |
| 68 | | | | | ANDS4 |
| 69 | | | | | ANDS5 |
| 70 | ANDSSG | | | | |
| 71 | | P43 | | | AN3 |
| 72 | | P42 | | | AN2 |
| 73 | | P41 | | | AN1 |
| 74 | VREFL0 | | | | |
| 75 | | P40 | | | AN0 |
| 76 | VREFH0 | | | | |
| 77 | AVCC0 | | | | |
| 78 | | P07 | | | AN6/ADTRG0# |
| 79 | AVSS0 | | | | |
| 80 | | P05 | | | AN5/DA1 |

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

# 2. CPU

Figure 2.1 shows the register set of the CPU.




Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

**Figure 2.1 Register Set of the CPU**

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory map.

## 4.1 I/O Register Addresses (Address Order)

**Table 4.1 List of I/O Registers (Address Order) (1 / 24)**

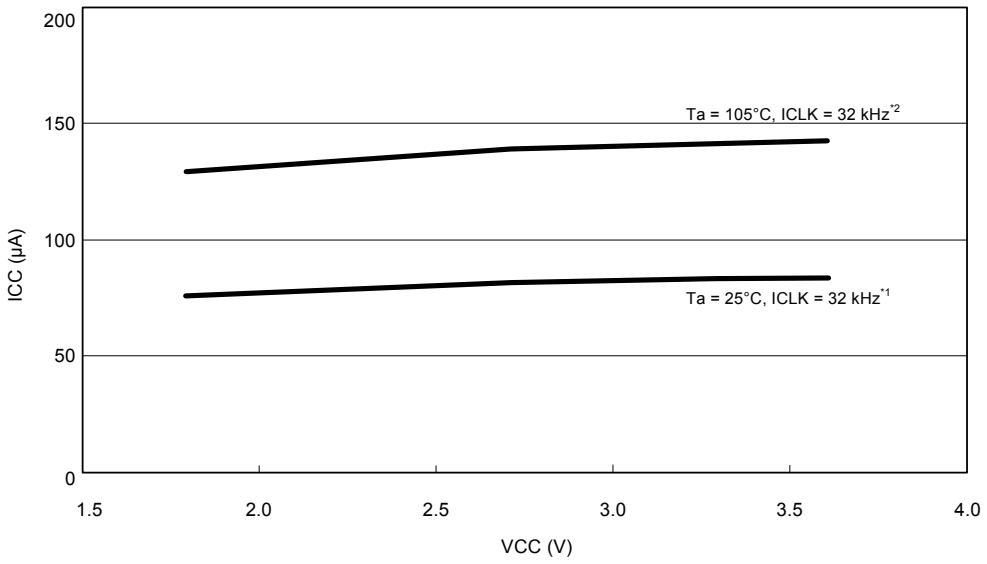
| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 0000h | SYSTEM | Mode monitor register | MDMONR | 16 | 16 | | 3 ICLK |
| 0008 0002h | SYSTEM | Mode status register | MDSR | 16 | 16 | | 3 ICLK |
| 0008 0008h | SYSTEM | System control register 1 | SYSCR1 | 16 | 16 | | 3 ICLK |
| 0008 000Ch | SYSTEM | Standby control register | SBYCR | 16 | 16 | | 3 ICLK |
| 0008 0010h | SYSTEM | Module stop control register A | MSTPCRA | 32 | 32 | | 3 ICLK |
| 0008 0014h | SYSTEM | Module stop control register B | MSTPCRB | 32 | 32 | | 3 ICLK |
| 0008 0018h | SYSTEM | Module stop control register C | MSTPCRC | 32 | 32 | | 3 ICLK |
| 0008 001Ch | SYSTEM | Module stop control register D | MSTPCRD | 32 | 32 | | 3 ICLK |
| 0008 0020h | SYSTEM | System clock control register | SCKCR | 32 | 32 | | 3 ICLK |
| 0008 0026h | SYSTEM | System clock control register 3 | SCKCR3 | 16 | 16 | | 3 ICLK |
| 0008 0028h | SYSTEM | PLL control register | PLLCR | 16 | 16 | | 3 ICLK |
| 0008 002Ah | SYSTEM | PLL control register 2 | PLLCR2 | 8 | 8 | | 3 ICLK |
| 0008 0032h | SYSTEM | Main clock oscillator control register | MOSCCR | 8 | 8 | | 3 ICLK |
| 0008 0033h | SYSTEM | Sub-clock oscillator control register | SOSCCR | 8 | 8 | | 3 ICLK |
| 0008 0034h | SYSTEM | Low-speed on-chip oscillator control register | LOCOCR | 8 | 8 | | 3 ICLK |
| 0008 0035h | SYSTEM | IWDT-dedicated on-chip oscillator control register | ILOCOCR | 8 | 8 | | 3 ICLK |
| 0008 0036h | SYSTEM | High-speed on-chip oscillator control register | HOCOCR | 8 | 8 | | 3 ICLK |
| 0008 0037h | SYSTEM | High-speed on-chip oscillator control register 2 | HOCOCR2 | 8 | 8 | | 3 ICLK |
| 0008 0040h | SYSTEM | Oscillation stop detection control register | OSTDCR | 8 | 8 | | 3 ICLK |
| 0008 0041h | SYSTEM | Oscillation stop detection status register | OSTDSR | 8 | 8 | | 3 ICLK |
| 0008 00A0h | SYSTEM | Operating power control register | OPCCR | 8 | 8 | | 3 ICLK |
| 0008 00A1h | SYSTEM | Sleep mode return clock source switching register | RSTCKCR | 8 | 8 | | 3 ICLK |
| 0008 00A2h | SYSTEM | Main clock oscillator wait control register | MOSCWTCR | 8 | 8 | | 3 ICLK |
| 0008 00A3h | SYSTEM | Sub-clock oscillator wait control register | SOSCWTCR | 8 | 8 | | 3 ICLK |
| 0008 00A6h | SYSTEM | PLL wait control register | PLLWTCR | 8 | 8 | | 3 ICLK |
| 0008 00A9h | SYSTEM | HOCO wait control register 2 | HOCOWTCR2 | 8 | 8 | | 3 ICLK |
| 0008 00C0h | SYSTEM | Reset status register 2 | RSTSR2 | 8 | 8 | | 3 ICLK |
| 0008 00C2h | SYSTEM | Software reset register | SWRR | 16 | 16 | | 3 ICLK |
| 0008 00E0h | SYSTEM | Voltage monitoring 1 circuit/comparator A1 control register 1 | LVD1CR1 | 8 | 8 | | 3 ICLK |
| 0008 00E1h | SYSTEM | Voltage monitoring 1 circuit/comparator A1 status register | LVD1SR | 8 | 8 | | 3 ICLK |
| 0008 00E2h | SYSTEM | Voltage monitoring 2 circuit/comparator A2 control register 1 | LVD2CR1 | 8 | 8 | | 3 ICLK |
| 0008 00E3h | SYSTEM | Voltage monitoring 2 circuit/comparator A2 status register | LVD2SR | 8 | 8 | | 3 ICLK |
| 0008 03FEh | SYSTEM | Protect register | PRCR | 16 | 16 | | 3 ICLK |
| 0008 1300h | BSC | Bus error status clear register | BERCLR | 8 | 8 | | 2 ICLK |
| 0008 1304h | BSC | Bus error monitoring enable register | BEREN | 8 | 8 | | 2 ICLK |
| 0008 1308h | BSC | Bus error status register 1 | BERSR1 | 8 | 8 | | 2 ICLK |
| 0008 130Ah | BSC | Bus error status register 2 | BERSR2 | 16 | 16 | | 2 ICLK |
| 0008 1310h | BSC | Bus priority control register | BUSPRI | 16 | 16 | | 2 ICLK |
| 0008 2000h | DMAC0 | DMA source address register | DMSAR | 32 | 32 | | 2 ICLK |
| 0008 2004h | DMAC0 | DMA destination address register | DMDAR | 32 | 32 | | 2 ICLK |
| 0008 2008h | DMAC0 | DMA transfer count register | DMCRA | 32 | 32 | | 2 ICLK |
| 0008 200Ch | DMAC0 | DMA block transfer count register | DMCRB | 16 | 16 | | 2 ICLK |
| 0008 2010h | DMAC0 | DMA transfer mode register | DMTMD | 16 | 16 | | 2 ICLK |
| 0008 2013h | DMAC0 | DMA interrupt setting register | DMINT | 8 | 8 | | 2 ICLK |
| 0008 2014h | DMAC0 | DMA address mode register | DMAMD | 16 | 16 | | 2 ICLK |
| 0008 2018h | DMAC0 | DMA offset register | DMOFR | 32 | 32 | | 2 ICLK |
| 0008 201Ch | DMAC0 | DMA transfer enable register | DMCNT | 8 | 8 | | 2 ICLK |
| 0008 201Dh | DMAC0 | DMA software start register | DMREQ | 8 | 8 | | 2 ICLK |
| 0008 201Eh | DMAC0 | DMA status register | DMSTS | 8 | 8 | | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (2 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 201Fh | DMAC0 | DMA activation source flag control register | DMCSL | 8 | 8 | | 2 ICLK |
| 0008 2040h | DMAC1 | DMA source address register | DMSAR | 32 | 32 | | 2 ICLK |
| 0008 2044h | DMAC1 | DMA destination address register | DMDAR | 32 | 32 | | 2 ICLK |
| 0008 2048h | DMAC1 | DMA transfer count register | DMCRA | 32 | 32 | | 2 ICLK |
| 0008 204Ch | DMAC1 | DMA block transfer count register | DMCRB | 16 | 16 | | 2 ICLK |
| 0008 2050h | DMAC1 | DMA transfer mode register | DMTMD | 16 | 16 | | 2 ICLK |
| 0008 2053h | DMAC1 | DMA interrupt setting register | DMINT | 8 | 8 | | 2 ICLK |
| 0008 2054h | DMAC1 | DMA address mode register | DMAMD | 16 | 16 | | 2 ICLK |
| 0008 205Ch | DMAC1 | DMA transfer enable register | DMCNT | 8 | 8 | | 2 ICLK |
| 0008 205Dh | DMAC1 | DMA software start register | DMREQ | 8 | 8 | | 2 ICLK |
| 0008 205Eh | DMAC1 | DMA status register | DMSTS | 8 | 8 | | 2 ICLK |
| 0008 205Fh | DMAC1 | DMA activation source flag control register | DMCSL | 8 | 8 | | 2 ICLK |
| 0008 2080h | DMAC2 | DMA source address register | DMSAR | 32 | 32 | | 2 ICLK |
| 0008 2084h | DMAC2 | DMA destination address register | DMDAR | 32 | 32 | | 2 ICLK |
| 0008 2088h | DMAC2 | DMA transfer count register | DMCRA | 32 | 32 | | 2 ICLK |
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | | 2 ICLK |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | | 2 ICLK |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | | 2 ICLK |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | | 2 ICLK |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | | 2 ICLK |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | | 2 ICLK |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | | 2 ICLK |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | | 2 ICLK |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | | 2 ICLK |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | | 2 ICLK |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | | 2 ICLK |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | | 2 ICLK |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | | 2 ICLK |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | | 2 ICLK |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | | 2 ICLK |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | | 2 ICLK |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | | 2 ICLK |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | | 2 ICLK |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | | 2 ICLK |
| 0008 2200h | DMAC | DMA module activation register | DMAST | 8 | 8 | | 2 ICLK |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | | 2 ICLK |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | | 2 ICLK |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | | 2 ICLK |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | | 2 ICLK |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | | 2 ICLK |
| 0008 6400h | MPU | Region-0 start page number register | RSPAGE0 | 32 | 32 | | 1 ICLK |
| 0008 6404h | MPU | Region-0 end page number register | REPAGE0 | 32 | 32 | | 1 ICLK |
| 0008 6408h | MPU | Region-1 start page number register | RSPAGE1 | 32 | 32 | | 1 ICLK |
| 0008 640Ch | MPU | Region-1 end page number register | REPAGE1 | 32 | 32 | | 1 ICLK |
| 0008 6410h | MPU | Region-2 start page number register | RSPAGE2 | 32 | 32 | | 1 ICLK |
| 0008 6414h | MPU | Region-2 end page number register | REPAGE2 | 32 | 32 | | 1 ICLK |
| 0008 6418h | MPU | Region-3 start page number register | RSPAGE3 | 32 | 32 | | 1 ICLK |
| 0008 641Ch | MPU | Region-3 end page number register | REPAGE3 | 32 | 32 | | 1 ICLK |
| 0008 6420h | MPU | Region-4 start page number register | RSPAGE4 | 32 | 32 | | 1 ICLK |
| 0008 6424h | MPU | Region-4 end page number register | REPAGE4 | 32 | 32 | | 1 ICLK |
| 0008 6428h | MPU | Region-5 start page number register | RSPAGE5 | 32 | 32 | | 1 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (10 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8036h | IWDT | IWDT reset control register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8038h | IWDT | IWDT count stop control register | IWDTCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C0h | DA | D/A data register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C2h | DA | D/A data register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C4h | DA | D/A control register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C5h | DA | DADRm format select register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8200h | TMR0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8201h | TMR1 | Timer counter control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8202h | TMR0 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8203h | TMR1 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8204h | TMR0 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8205h | TMR1 | Time constant register A | TCORA | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8206h | TMR0 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8207h | TMR1 | Time constant register B | TCORB | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8208h | TMR0 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8209h | TMR1 | Timer counter | TCNT | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Ah | TMR0 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Bh | TMR1 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Ch | TMR0 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8210h | TMR2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8211h | TMR3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8212h | TMR2 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8213h | TMR3 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8214h | TMR2 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8215h | TMR3 | Time constant register A | TCORA | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8216h | TMR2 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8217h | TMR3 | Time constant register B | TCORB | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8218h | TMR2 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8219h | TMR3 | Timer counter | TCNT | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ah | TMR2 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Bh | TMR3 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ch | TMR2 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8300h | RIIC0 | $I^2C$ bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8301h | RIIC0 | $I^2C$ bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8302h | RIIC0 | $I^2C$ bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8303h | RIIC0 | $I^2C$ bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8304h | RIIC0 | $I^2C$ bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8305h | RIIC0 | $I^2C$ bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8306h | RIIC0 | $I^2C$ bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8307h | RIIC0 | $I^2C$ bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8308h | RIIC0 | $I^2C$ bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8309h | RIIC0 | $I^2C$ bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Timeout internal counter U | TMOCNTU | 8 | 8*2 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |




Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

**Figure 5.5 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data)**

**Table 5.17 Output Values of Voltage (1)**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 2.7 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output mode | $V_{OL}$ | — | 0.4 | V | $I_{OL}$ = 0.5 mA |
| | | High-drive output mode | | — | 0.4 | | $I_{OL}$ = 1.0 mA |
| Output high | All output pins | Normal output mode | $V_{OH}$ | VCC – 0.4 | — | V | $I_{OL}$ = –0.5 mA |
| | | High-drive output mode | | VCC – 0.4 | — | | $I_{OL}$ = –1.0 mA |

**Table 5.18 Output Values of Voltage (2)**

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL =0 V,
$T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output mode | $V_{OL}$ | — | 1.0 | V | $I_{OL}$ = 3.0 mA |
| | | High-drive output mode | | — | 1.0 | | $I_{OL}$ = 5.0 mA |
| | RIIC pins | | | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| Output high | All output pins | Normal output mode | $V_{OH}$ | VCC – 1.0 | — | V | $I_{OL}$ = –3.0 mA |
| | | High-drive output mode | | VCC – 1.0 | — | | $I_{OL}$ = –5.0 mA |

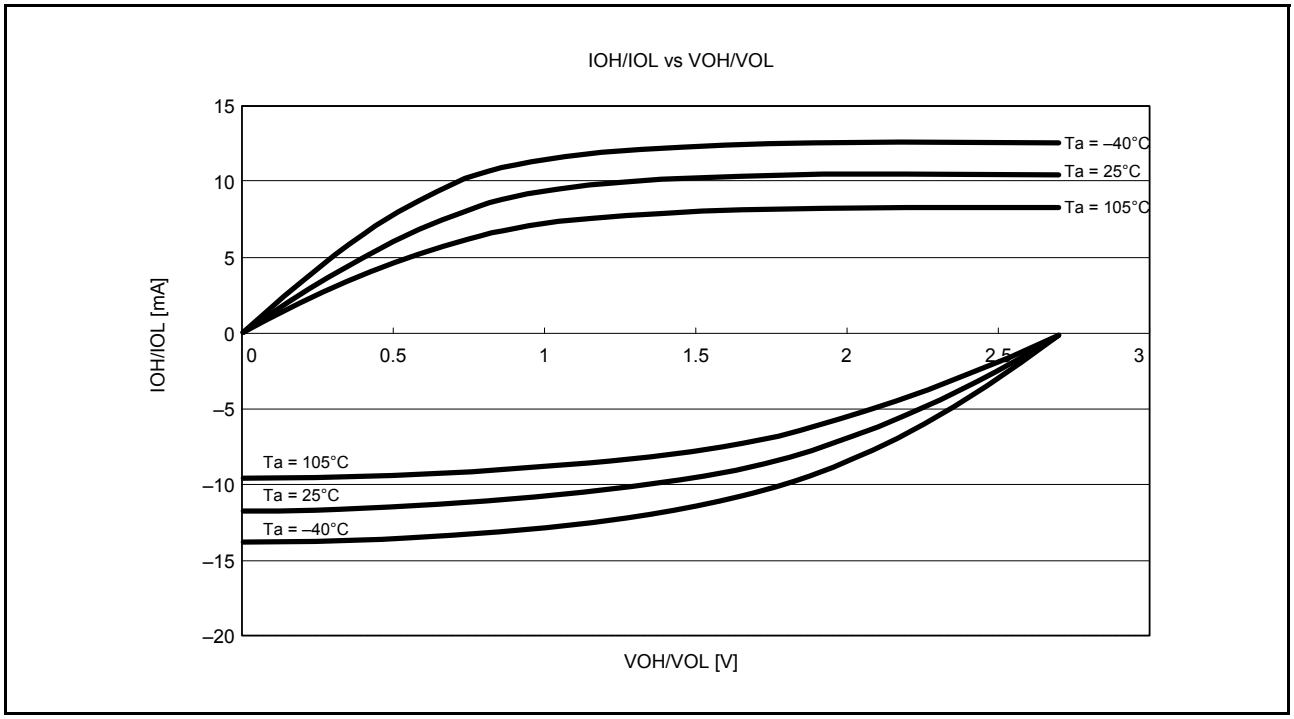



**Figure 5.13 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when Normal Output is Selected (Reference Data)**

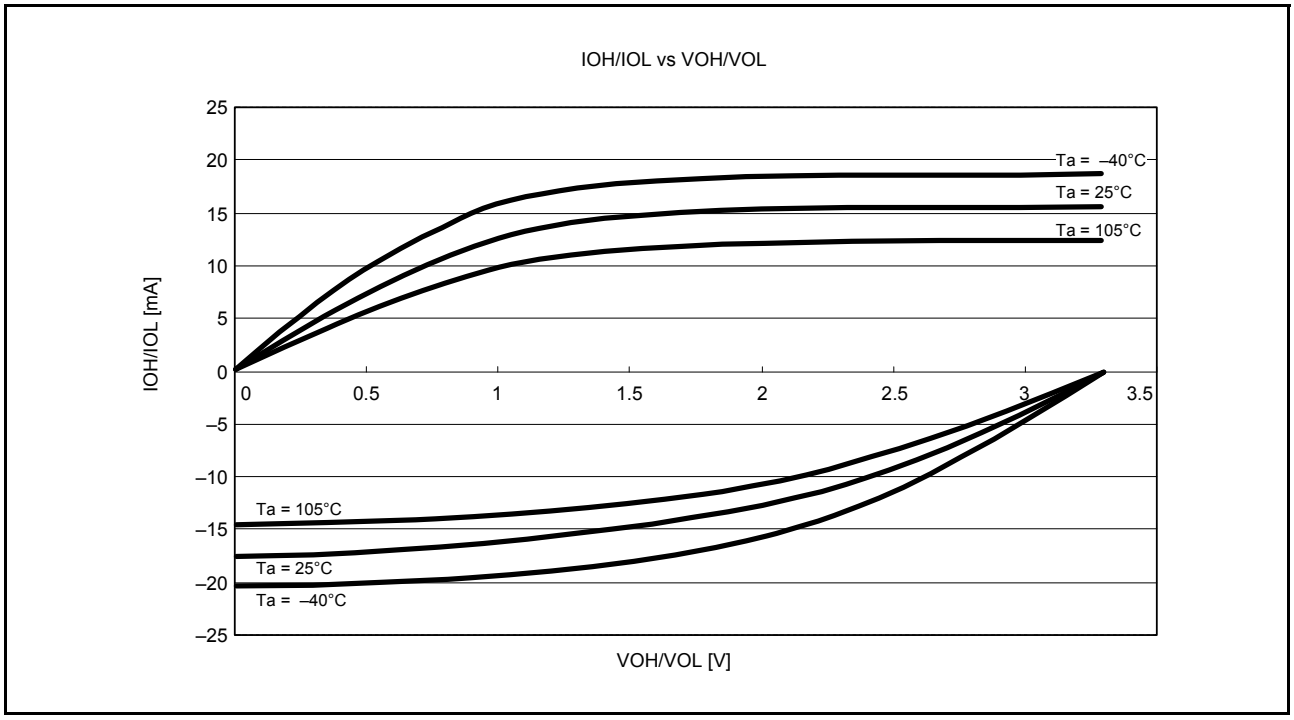



**Figure 5.14 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when Normal Output is Selected (Reference Data)**

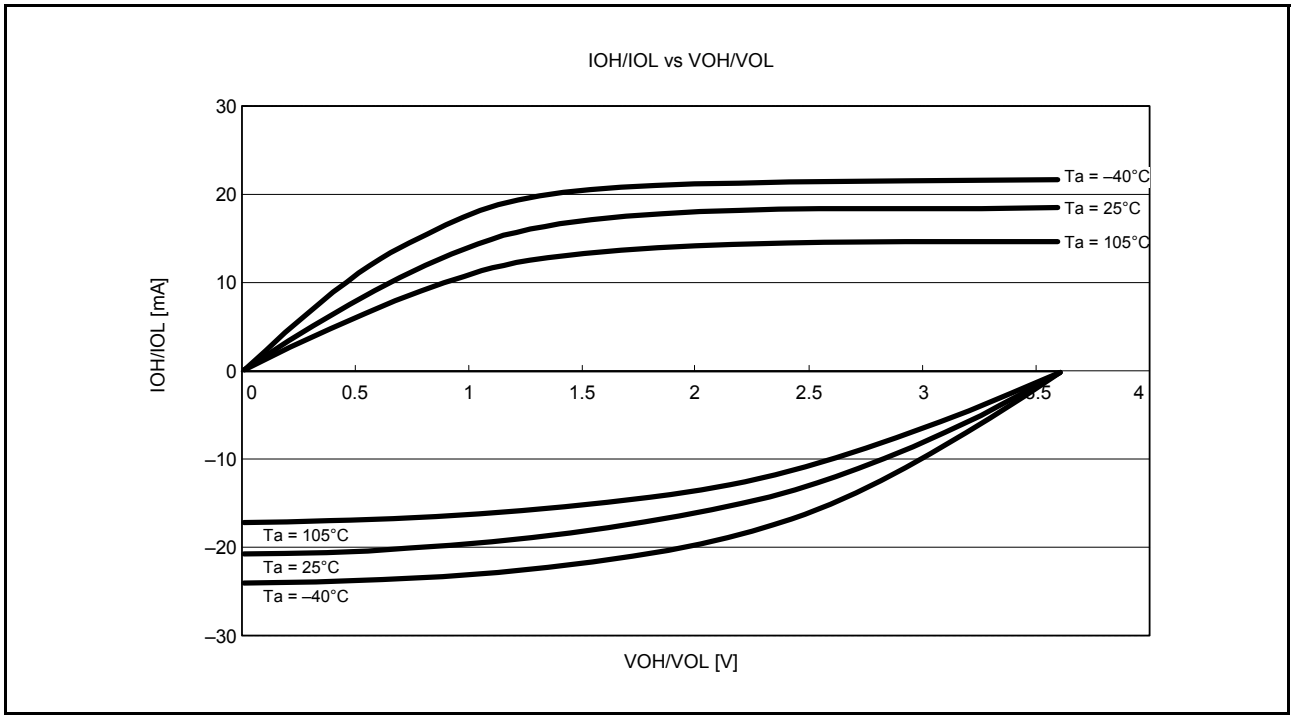



**Figure 5.15 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.6 V when Normal Output is Selected (Reference Data)**

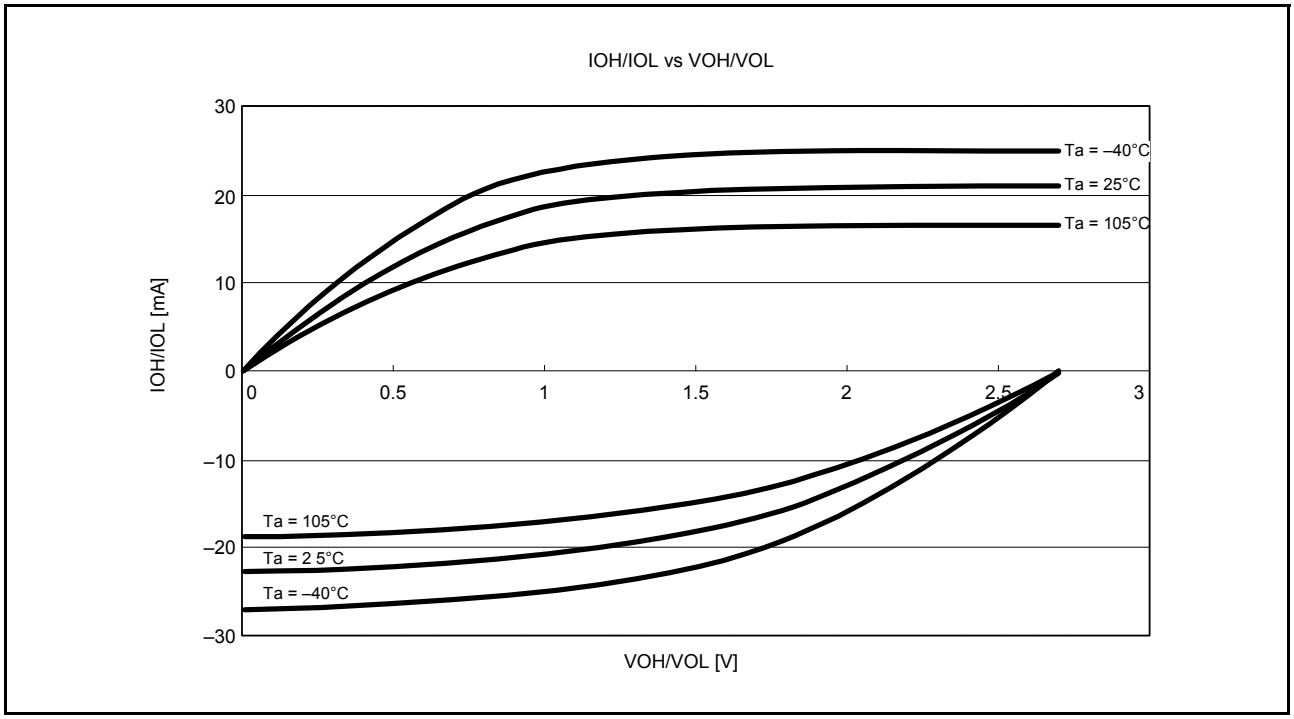



**Figure 5.18 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)**

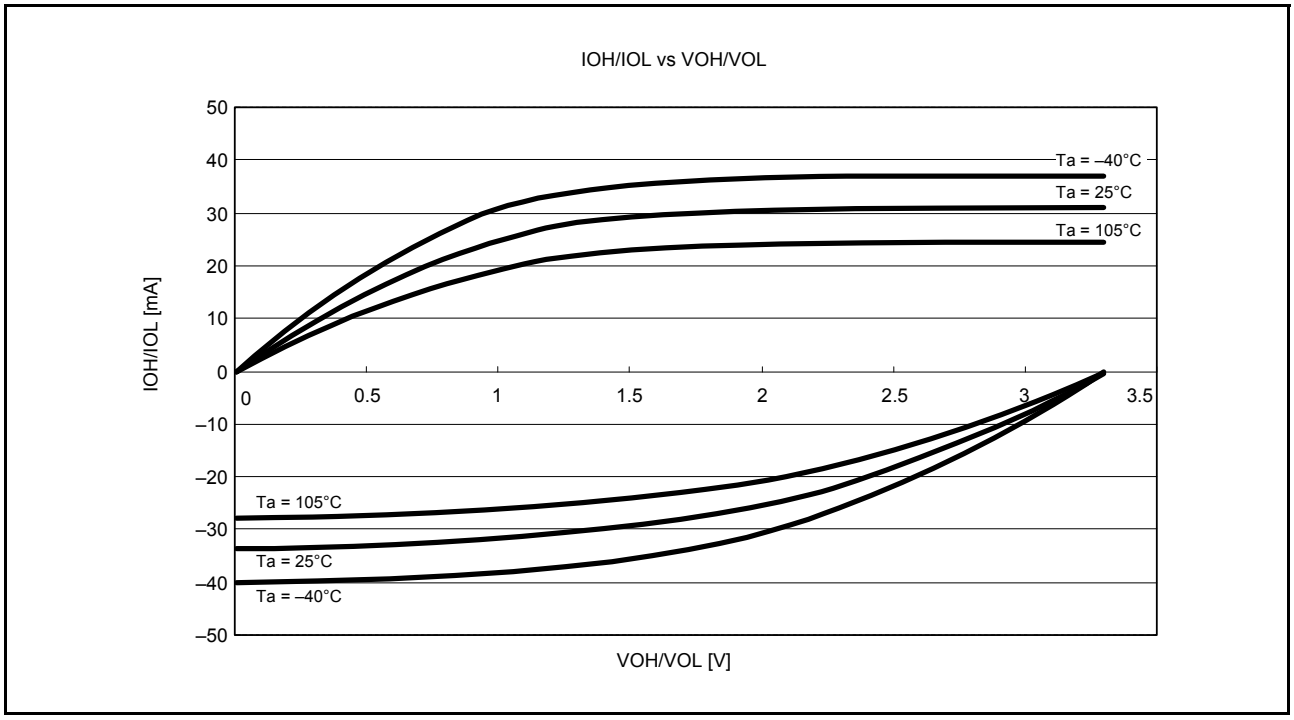



**Figure 5.19 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)**

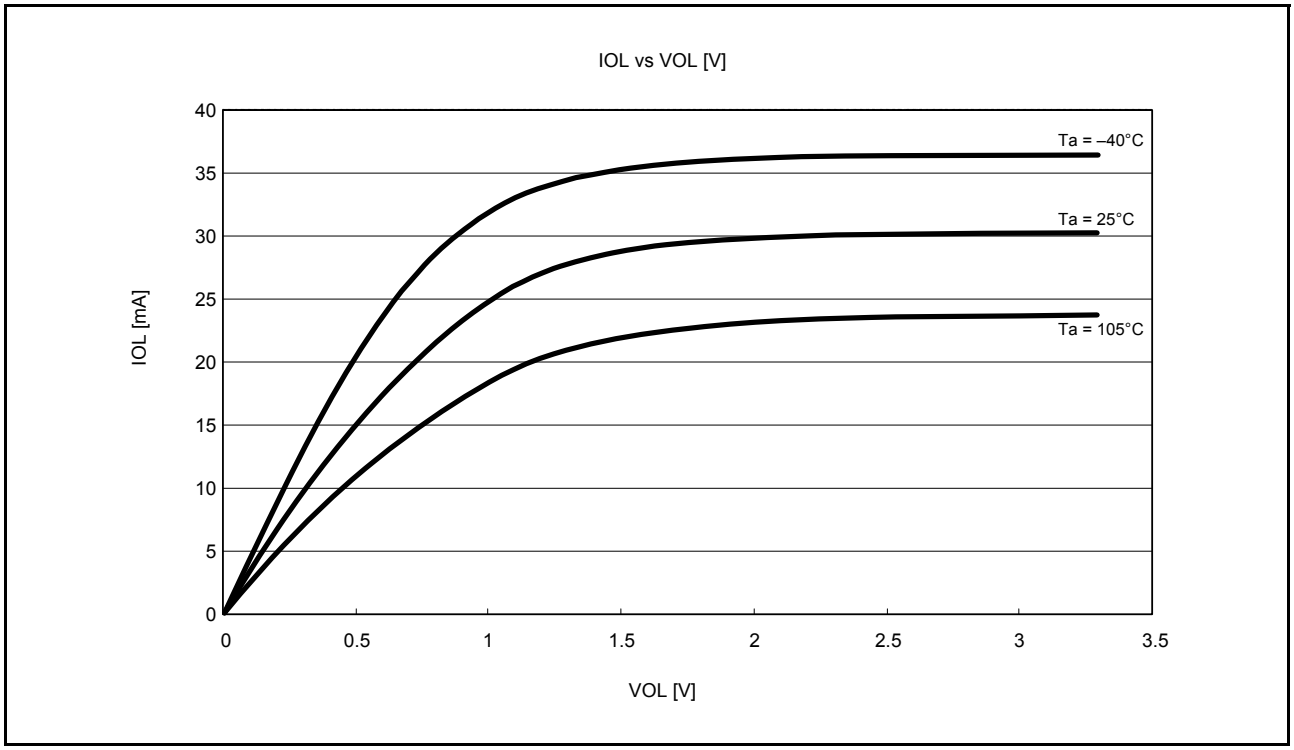



**Figure 5.23 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)**

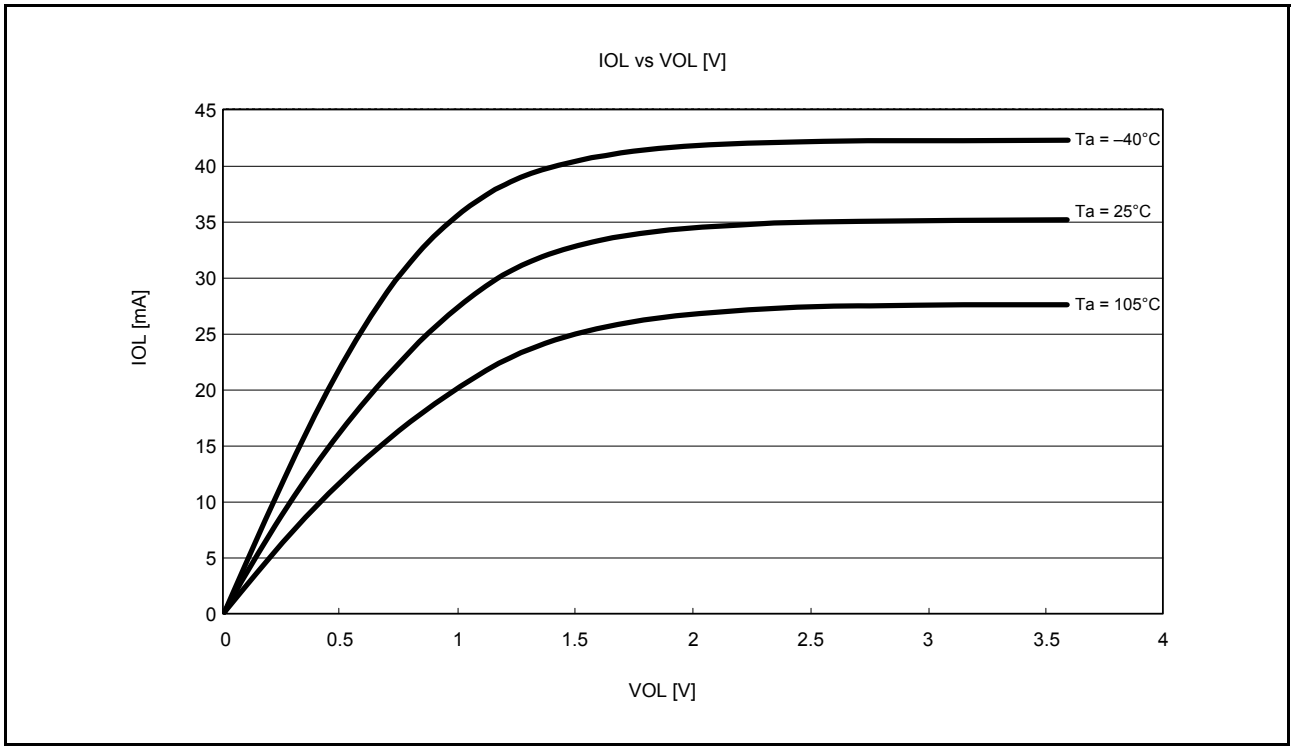



**Figure 5.24 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.6 V (Reference Data)**

**Table 5.31 Timing of On-Chip Peripheral Modules (2)**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C
When high-drive output is selected by the drive capacity register while 1.8 V ≤ VCC < 2.7 V

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | C = 30 pF Figure 5.46 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 | — | $t_{Pcyc}$ | C = 30 pF Figure 5.47 |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time | Clock synchronous (master) | $t_{TXD}$ | — | 40 | ns | |
| | Transmit data delay time | Clock synchronous (slave) 2.7 V ≤ VCC ≤ 3.6 V | | — | 65 | | |
| | | Clock synchronous (slave) 1.8 V ≤ VCC < 2.7 V | | — | 85 | | |
| | Receive data setup time | Clock synchronous (master) 2.7 V ≤ VCC ≤ 3.6 V | $t_{RXS}$ | 65 | — | ns | |
| | | Clock synchronous (master) 1.8 V ≤ VCC < 2.7 V | | 75 | — | | |
| | | Clock synchronous (slave) | | 40 | — | | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 40 | — | ns | |

Note 1. $t_{Pcyc}$: PCLK cycle

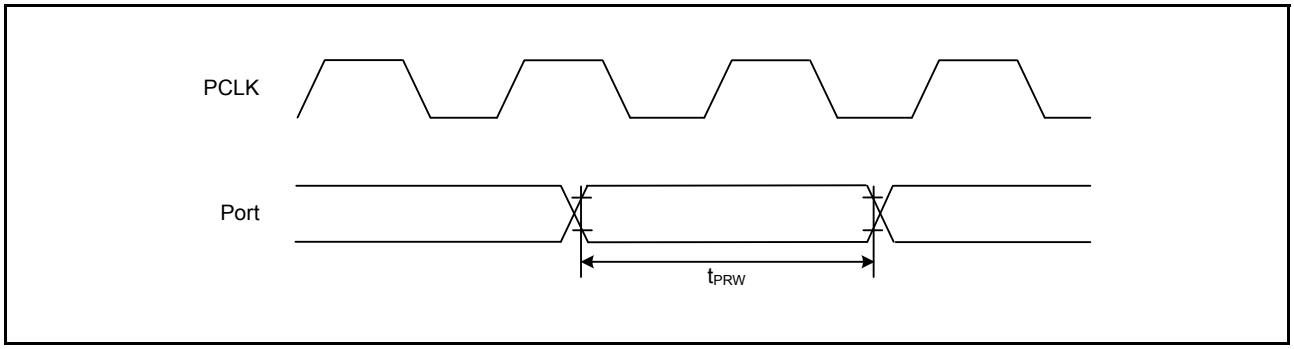



**Figure 5.41 I/O Port Input Timing**

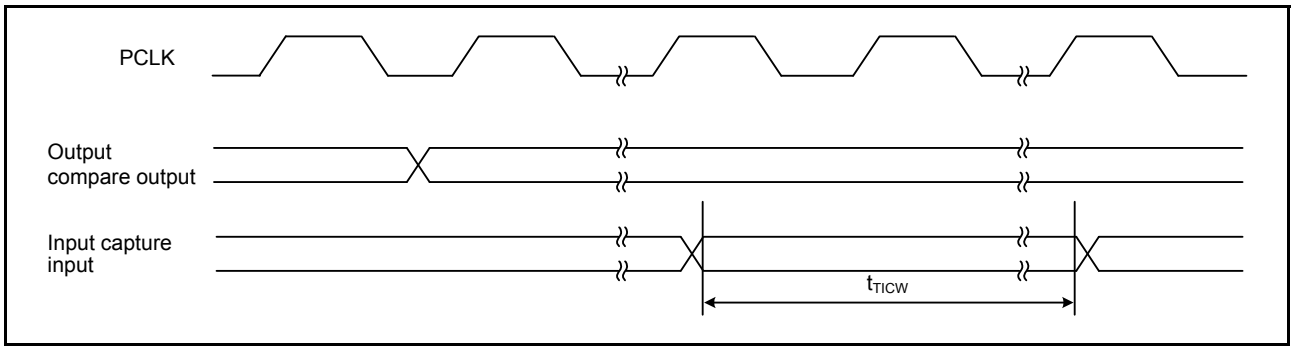



**Figure 5.42 MTU Input/Output Timing**

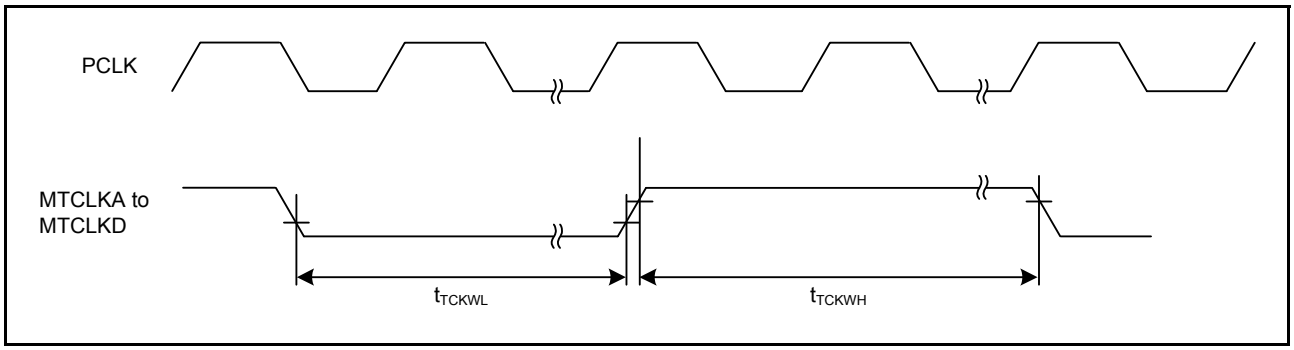



**Figure 5.43 MTU Clock Input Timing**

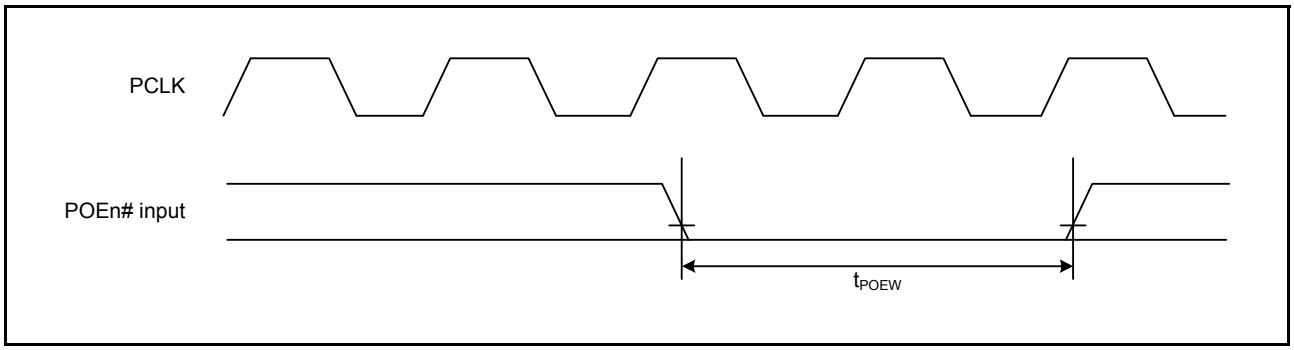



**Figure 5.44 POE# Input Timing**

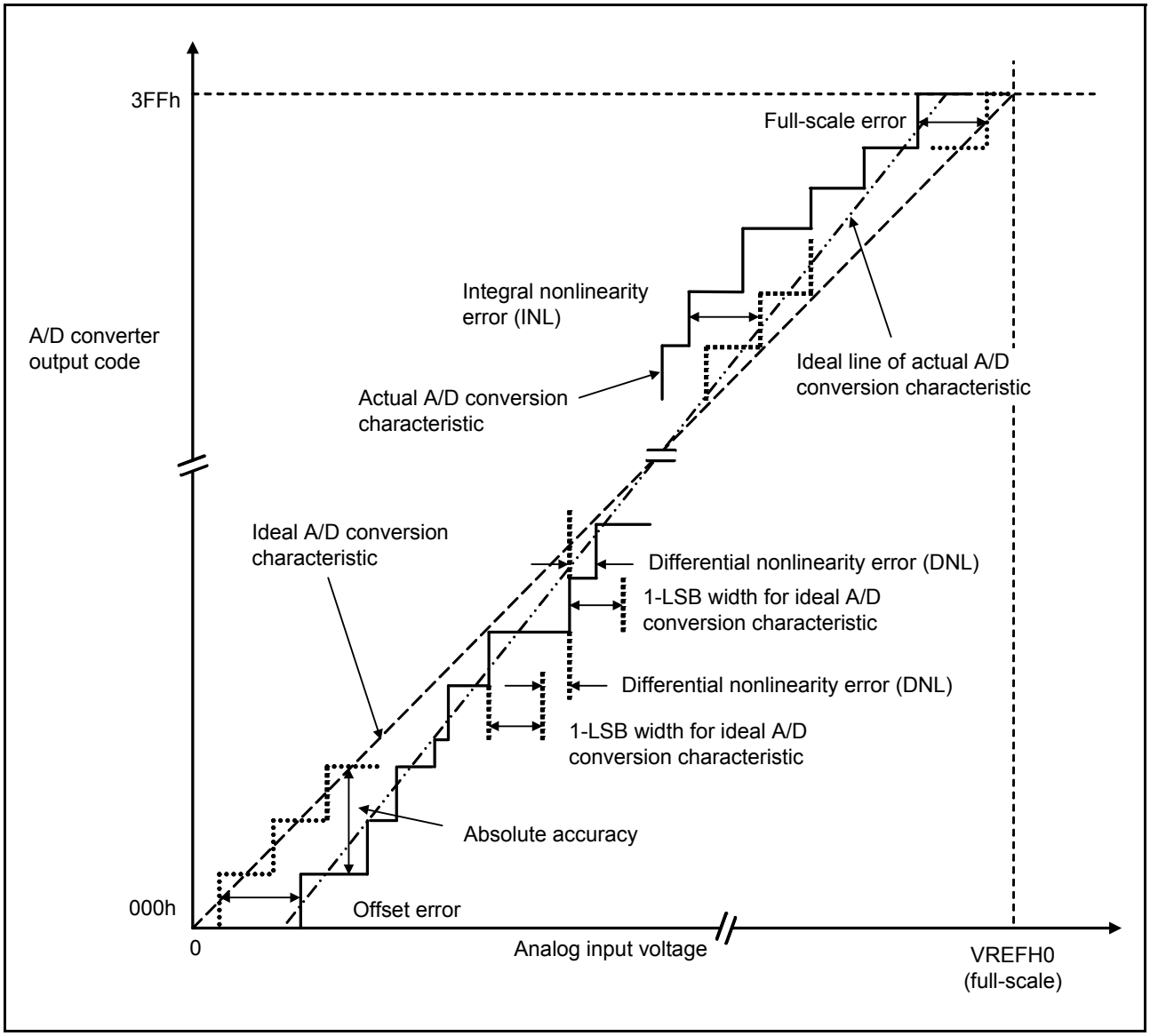



**Figure 5.62 Illustration of A/D Converter Characteristic Terms**

### Absolute accuracy

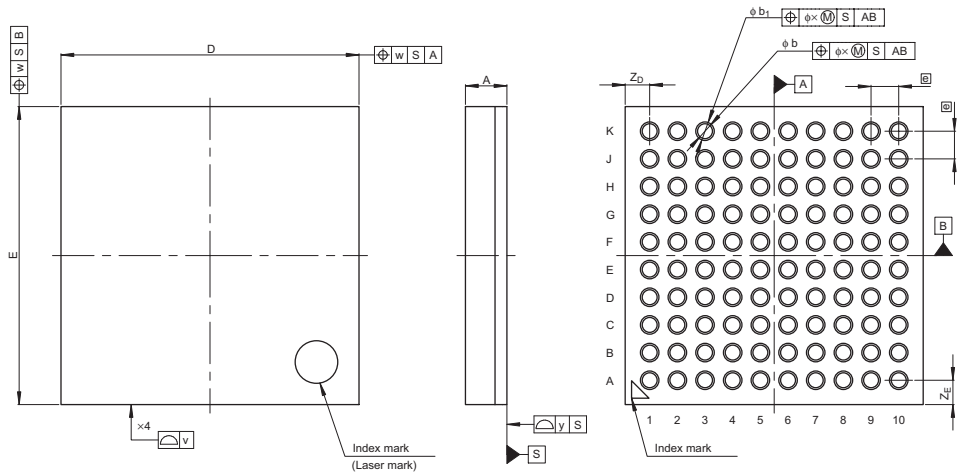
Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if reference voltage VREFH0 = 2.56 V, then 1-LSB width becomes 2.5 mV, and 0 mV, 2.5 mV, 5.0 mV, ... are used as analog input voltages.

If analog input voltage is 20 mV, absolute accuracy = ±4 LSB means that the actual A/D conversion result is in the range of 004h to 00Ch though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

Figure D 100-Pin TFLGA (PTLG0100JA-A)