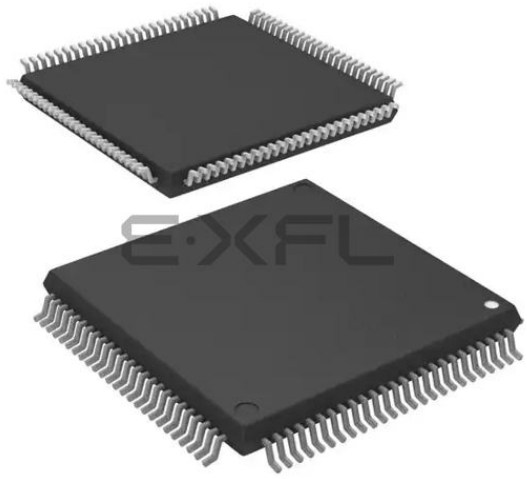
Renesas Electronics America Inc - R5F521A6BDFP#30 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdfp-30

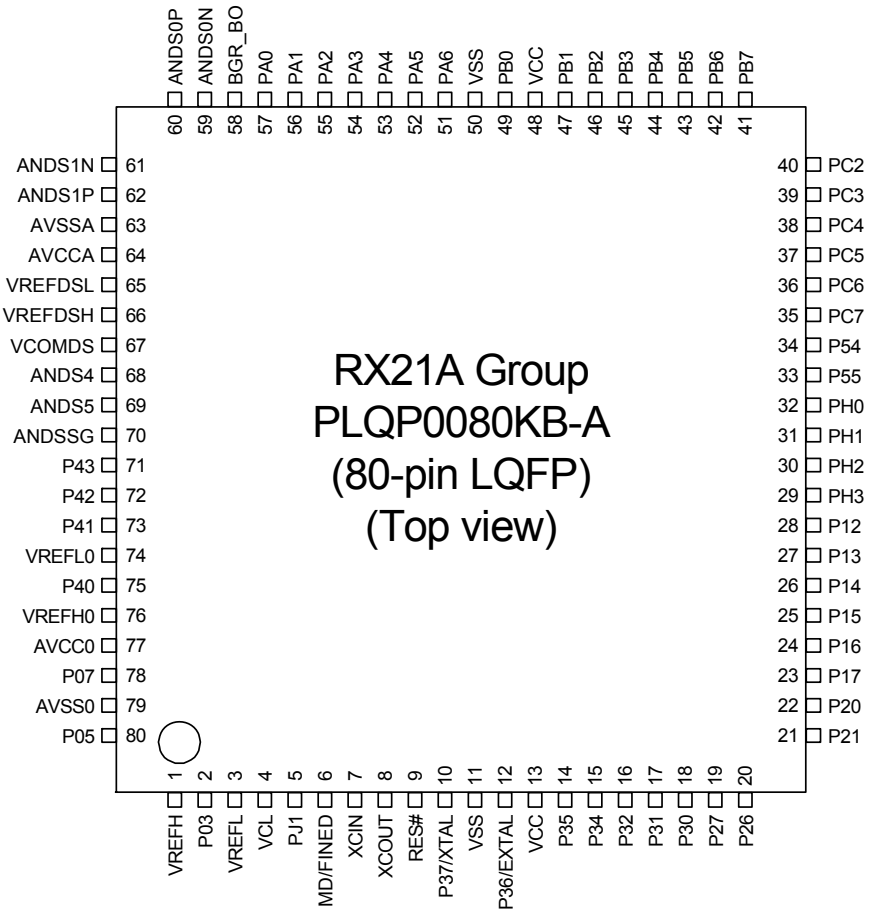
1. Overview

1.1 Outline of Specifications

Table 1.1 shows the outline of the specifications and Table 1.2 shows the comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

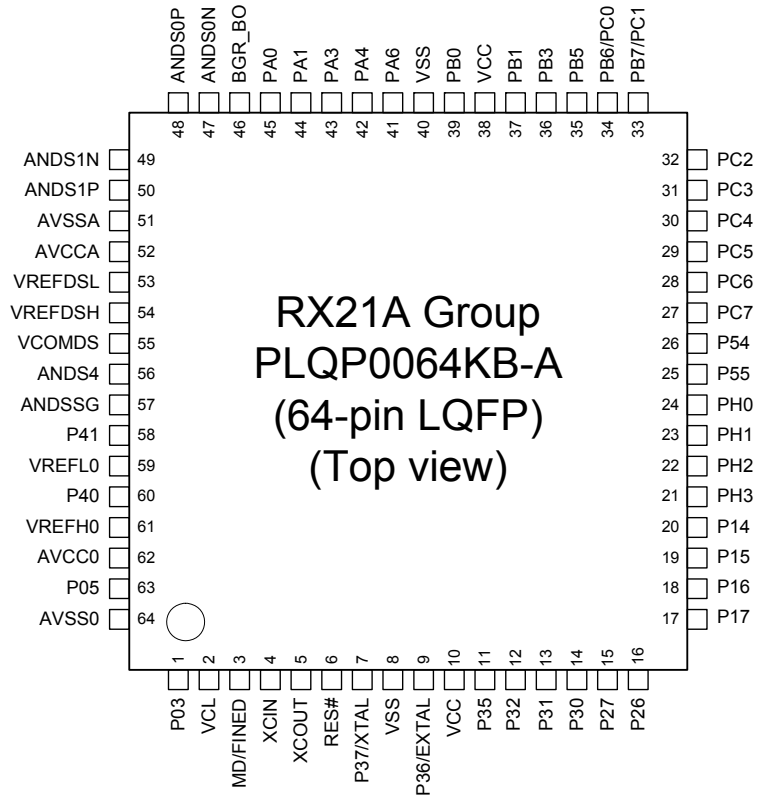
Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
Memory	ROM	• Capacity: 256 K/384 K/512 Kbytes • 50 MHz, no-wait memory access • On-board programming: 3 types
	RAM	• Capacity:32 K/64 Kbytes • 50 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLK):25 MHz (at max.) The flash peripheral circuit runs in synchronization with the flash peripheral clock (FCLK): 25 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit (LVDAa)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 2 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 9 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 122 • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

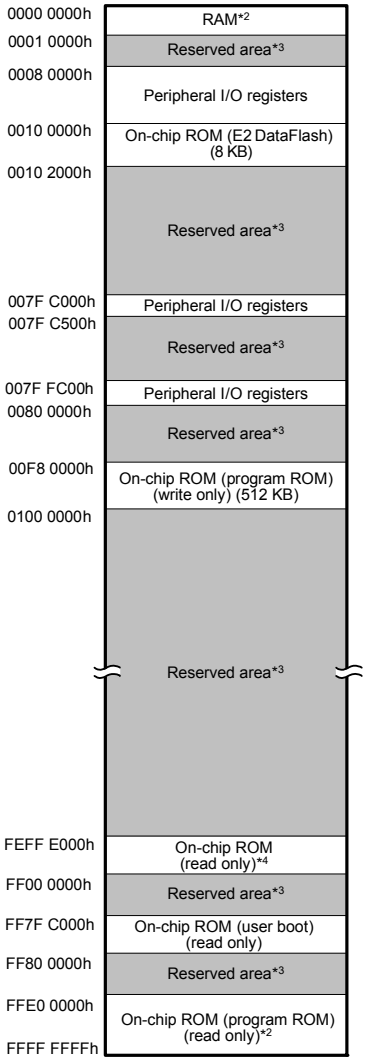
Figure 1.4 Pin Assignments of the 80-Pin LQFP



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LQFP

Single-chip mode*1



Note 1. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh

Note:•See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
Note 4. Only some specific addresses are usable. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
Section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
Section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
Section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
Section 37.3, Using the Temperature Sensor
Section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

Figure 3.1 Memory Map

Table 4.1 List of I/O Registers (Address Order) (9 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 73FBh	ICU	Interrupt source priority register 251	IPR251	8	8		2 ICLK
0008 73FCh	ICU	Interrupt source priority register 252	IPR252	8	8		2 ICLK
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8		2 ICLK
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8		2 ICLK
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8		2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
0008 C121h	PORT	Port switching register A	PSRA	8	8	2, 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (22 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to DPSBKR31	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK
0008 C402h	RTC	Second counter/Binary counter 0	RSECCNT/ BCNT0	8	8	2, 3 PCLKB	2 ICLK
0008 C404h	RTC	Minute counter/Binary counter 1	RMINCNT/ BCNT1	8	8	2, 3 PCLKB	2 ICLK
0008 C406h	RTC	Hour counter/Binary counter 2	RHRCNT/ BCNT2	8	8	2, 3 PCLKB	2 ICLK
0008 C408h	RTC	Day-of-week counter/Binary counter 3	RWKCNT/ BCNT3	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK
0008 C410h	RTC	Second alarm register/Binary counter 0 alarm register	RSECAR/ BCNT0AR	8	8	2, 3 PCLKB	2 ICLK
0008 C412h	RTC	Minute alarm register/Binary counter 1 alarm register	RMINAR/ BCNT1AR	8	8	2, 3 PCLKB	2 ICLK
0008 C414h	RTC	Hour alarm register/Binary counter 2 alarm register	RHRAR/ BCNT2AR	8	8	2, 3 PCLKB	2 ICLK
0008 C416h	RTC	Day-of-week alarm register/Binary counter 3 alarm register	RWKAR/ BCNT3AR	8	8	2, 3 PCLKB	2 ICLK
0008 C418h	RTC	Date alarm register/Binary counter 0 alarm enable register	RDAYAR/ BCNT0AER	8	8	2, 3 PCLKB	2 ICLK
0008 C41Ah	RTC	Month alarm register/Binary counter 1 alarm enable register	RMONAR/ BCNT1AER	8	8	2, 3 PCLKB	2 ICLK
0008 C41Ch	RTC	Year alarm register/Binary counter 2 alarm enable register	RYRAR/ BCNT2AER	16	16	2, 3 PCLKB	2 ICLK
0008 C41Eh	RTC	Year alarm enable register/Binary counter 3 alarm enable register	RYRAREN/ BCNT3AER	8	8	2, 3 PCLKB	2 ICLK
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK
0008 C452h	RTC	Second capture register 0/BCNT0 capture register 0	RSECCP0/ BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C454h	RTC	Minute capture register 0/BCNT1 capture register 0	RMINCP0/ BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C456h	RTC	Hour capture register 0/BCNT2 capture register 0	RHRCP0/ BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ah	RTC	Date capture register 0/BCNT3 capture register 0	RDAYCP0/ BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK
0008 C45Ch	RTC	Month capture register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK
0008 C462h	RTC	Second capture register 1/BCNT0 capture register 1	RSECCP1/ BCNT0CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C464h	RTC	Minute capture register 1/BCNT1 capture register 1	RMINCP1/ BCNT1CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C466h	RTC	Hour capture register 1/BCNT2 capture register 1	RHRCP1/ BCNT2CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ah	RTC	Date capture register 1/BCNT3 capture register 1	RDAYCP1/ BCNT3CP1	8	8	2, 3 PCLKB	2 ICLK
0008 C46Ch	RTC	Month capture register 1	RMONCP1	8	8	2, 3 PCLKB	2 ICLK
0008 C472h	RTC	Second capture register 2/BCNT0 capture register 2	RSECCP2/ BCNT0CP2	8	8	2, 3 PCLKB	2 ICLK

5.2.3 RIIC Pin Output Characteristics

Figure 5.21 to Figure 5.24 show the output characteristics of the RIIC pin.

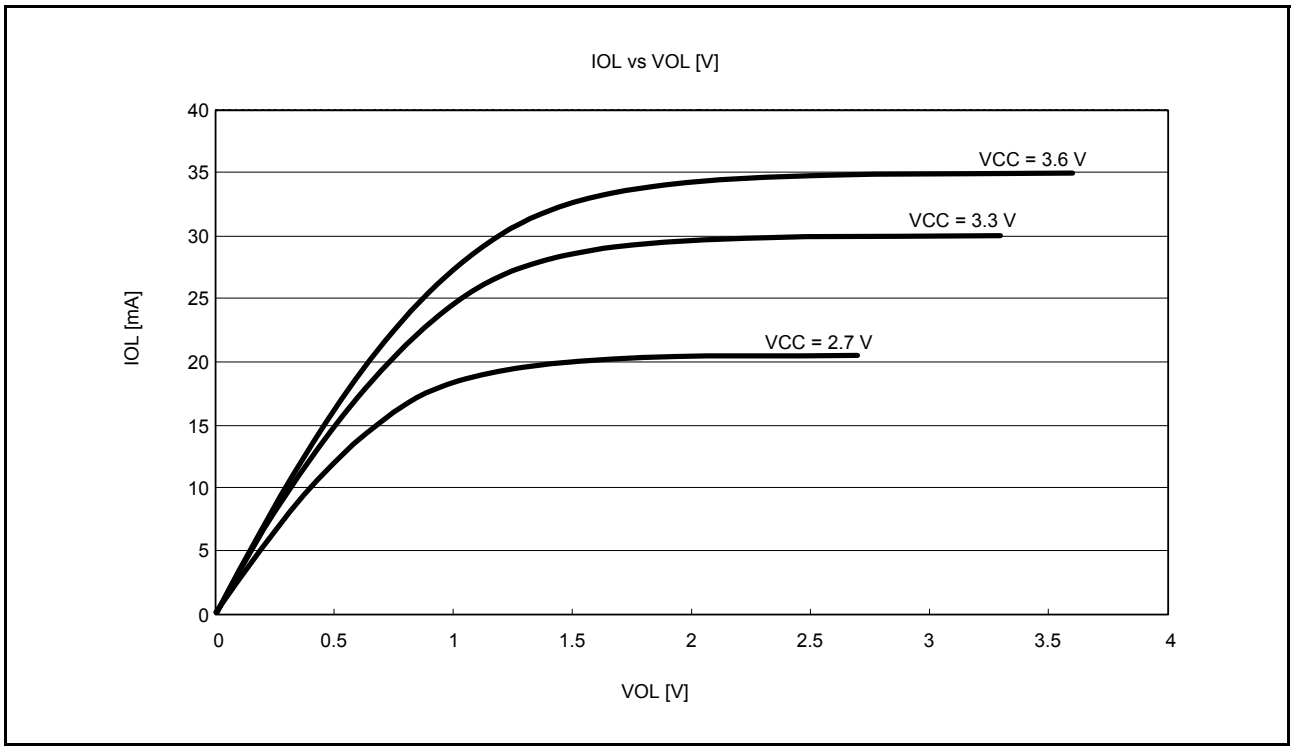


Figure 5.21 VOH and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)

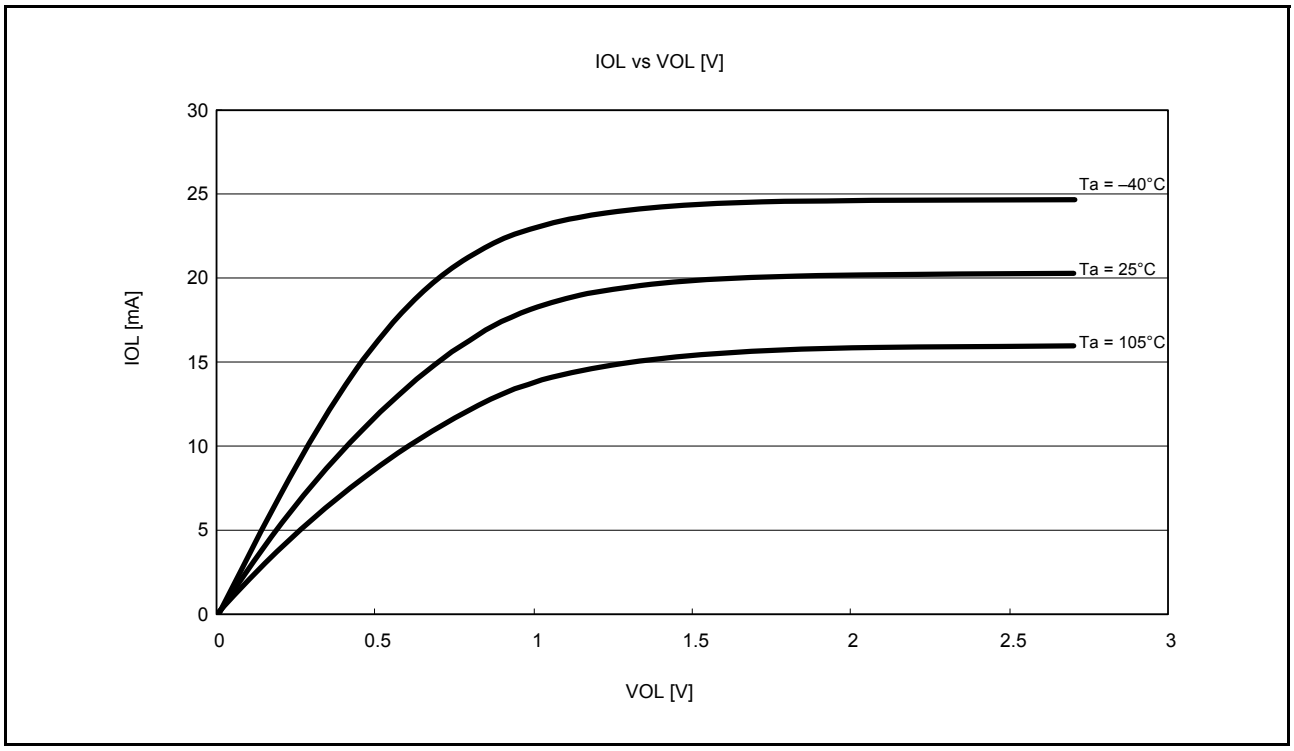


Figure 5.22 VOH and IOL Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

Note 2. When specifying the main clock oscillator stabilization time, load MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 3. Sum of the main clock oscillation stabilization time and the PLL oscillation stabilization time.
Note 4. The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 5. When specifying the sub-clock oscillation stabilization time, load SOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.

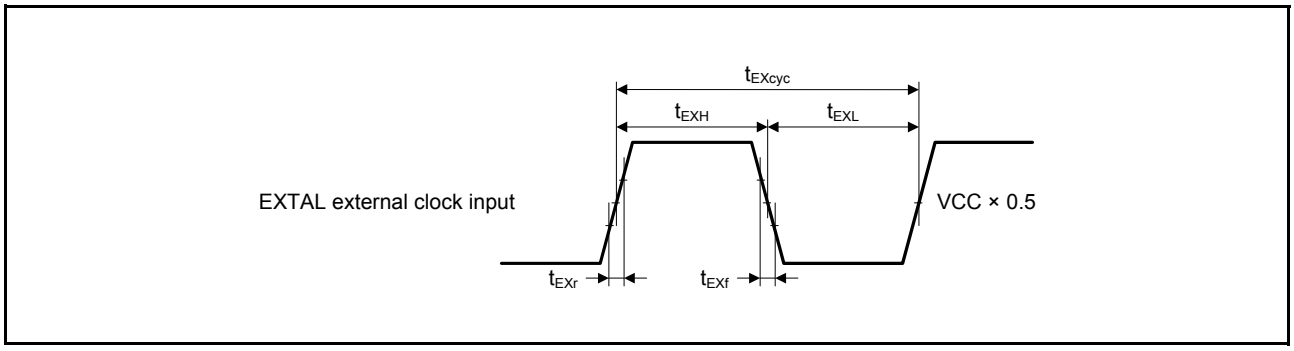


Figure 5.25 EXTAL External Clock Input Timing

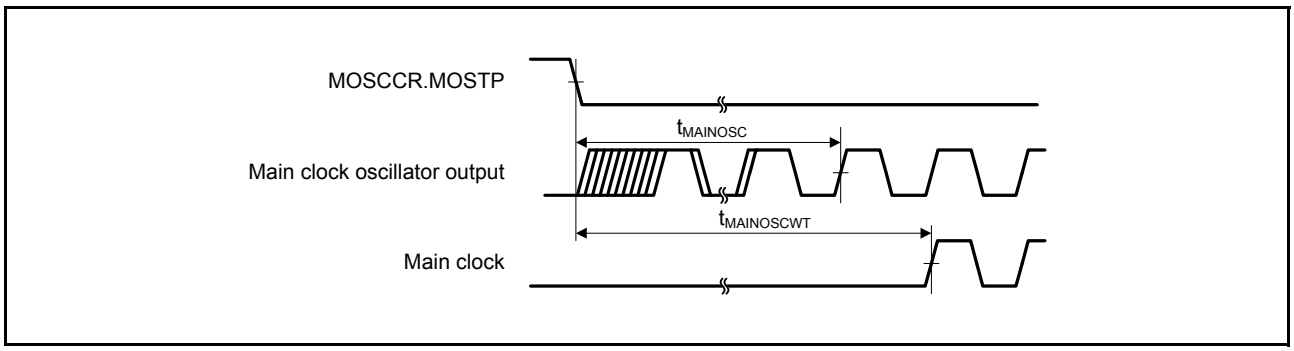


Figure 5.26 Main Clock Oscillation Start Timing

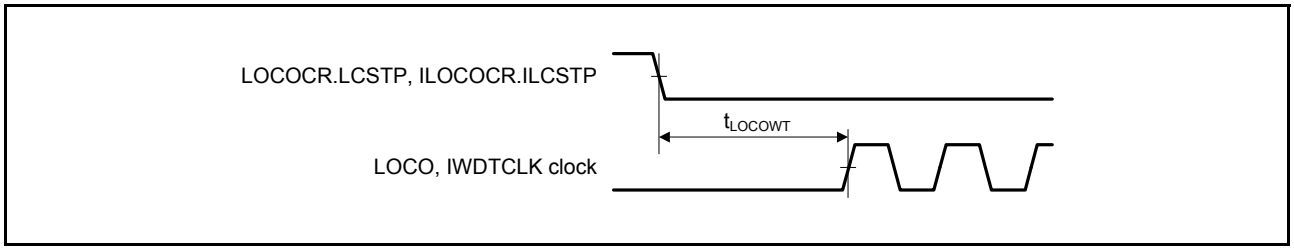


Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing

Table 5.32 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.49
		Master 1.8 V ≤ VCC < 2.7 V		4	4096		
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	10	ns	
		Input		—	1	µs	
	Data input setup time	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	4	—	ns	C = 30 pF Figure 5.50 to Figure 5.53
		Master 1.8 V ≤ VCC < 2.7 V		16	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	t_{Pcyc}	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	10	ns	
		Slave 2.7 V ≤ VCC ≤ 3.6 V		—	$3 \times t_{Pcyc} + 55$		
		Slave 1.8 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 72$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	10	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	20	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.52 and Figure 5.53
	Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	4	t_{Pcyc}	
		1.8 V ≤ VCC < 2.7 V		—	5		

Note 1. t_{Pcyc}: PCLK cycle

Table 5.35 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 5.54
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	Figure 5.54
	SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{pcyc}*2	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: • t_{Pcyc}: PCLK cycle
Note 1. C_b indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

Item	Min.	Typ.	Max.	Unit	Test Conditions	
Input impedance for single-ended input (×4)	54	91	—	kΩ		
Oversampling frequency	3.125	3.125	3.125	MHz		
Oversampling period	0.32	0.32	0.32	µs		
Conversion time	81.92	—	245.76	µs		
Sampling frequency	4.07	—	12.21	kHz		
SNDR (Gain: ×1 Input amplitude: 500.0 mV)	—	80	—	dB		Sampling frequency = 12.21 kHz Clock source: Resonator
	—	85	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×2 Input amplitude: 250.0 mV)	—	80	—	dB		
	—	85	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×4 Input amplitude: 125.0 mV)	—	78	—	dB		
	—	83	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×8 Input amplitude: 62.5 mV)	—	75	—	dB		
	—	80	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×16 Input amplitude: 31.2 mV)	—	71	—	dB		
	—	76	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×32 Input amplitude: 14.4 mV)	—	64	—	dB		
	—	69	—	dB	Bandwidth = up to 1.7 kHz	
SNDR (Gain: ×64 Input amplitude: 5 mV)	—	54	—	dB		
	—	59	—	dB	Bandwidth = up to 1.7 kHz	

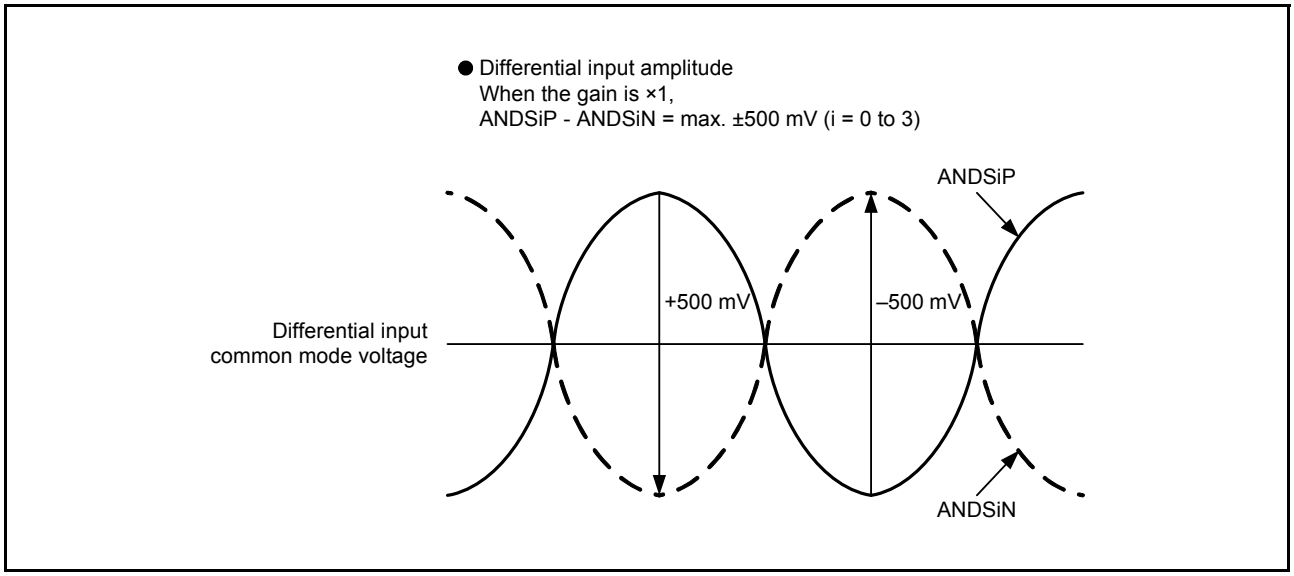


Figure 5.55 Differential Input Amplitude

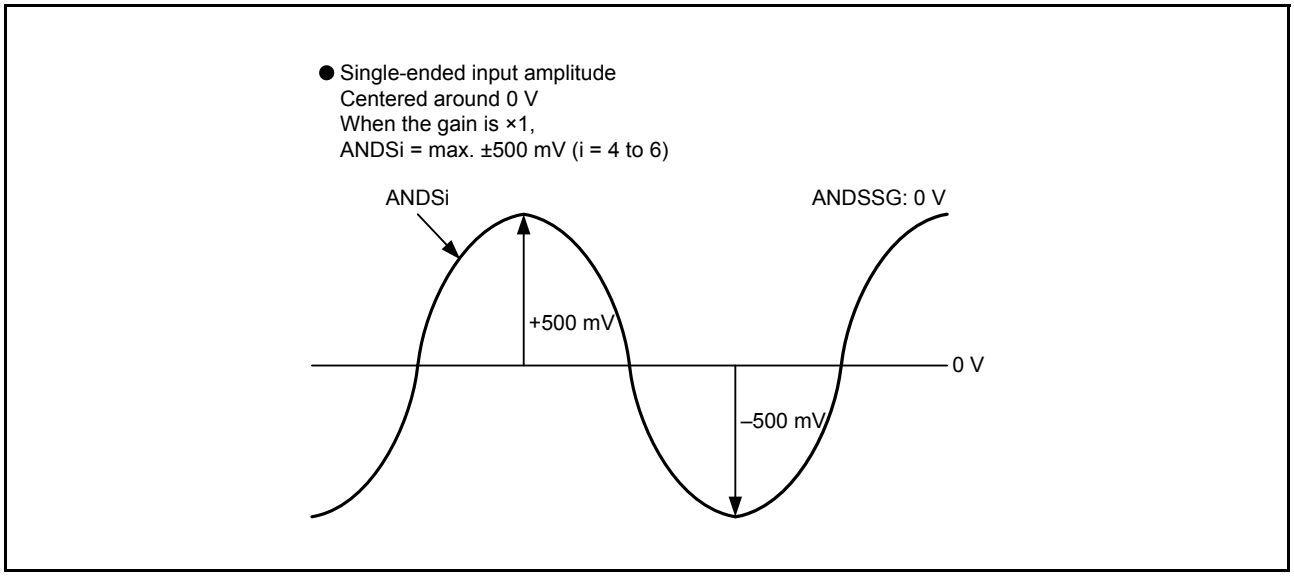


Figure 5.56 Single-ended Input Amplitude

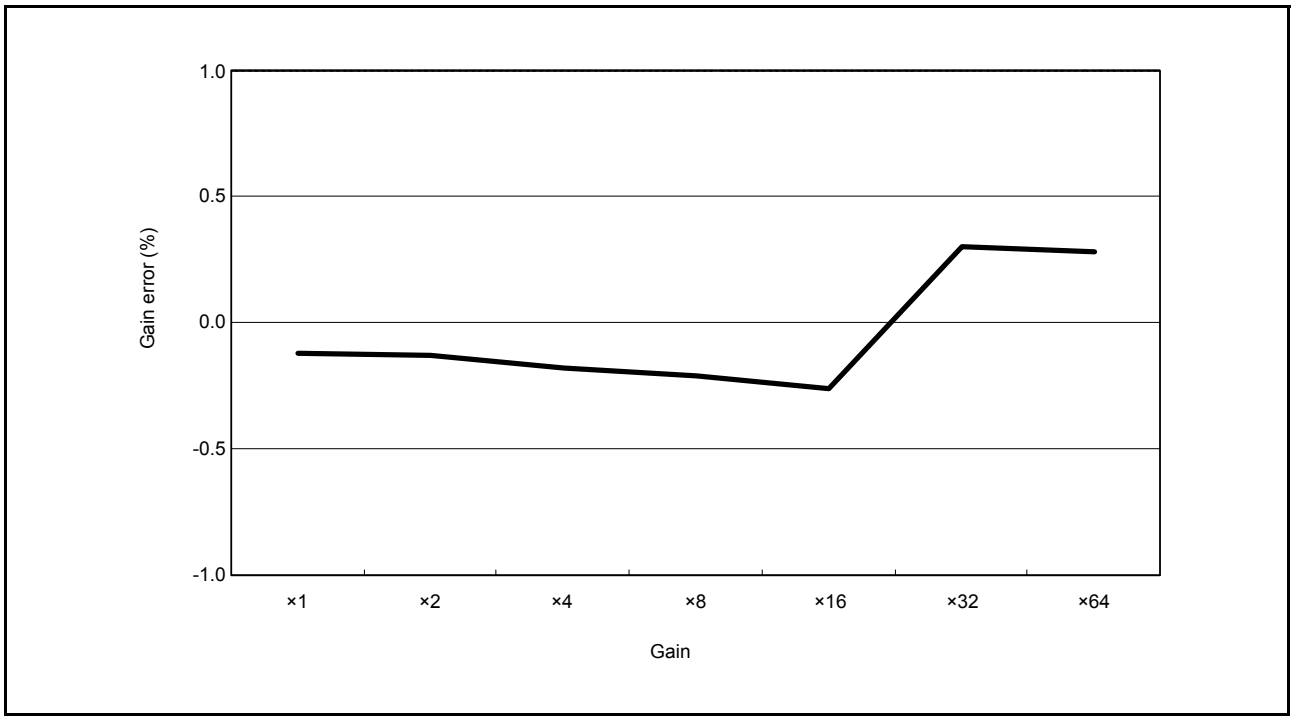


Figure 5.57 Gain Error (Reference Data)

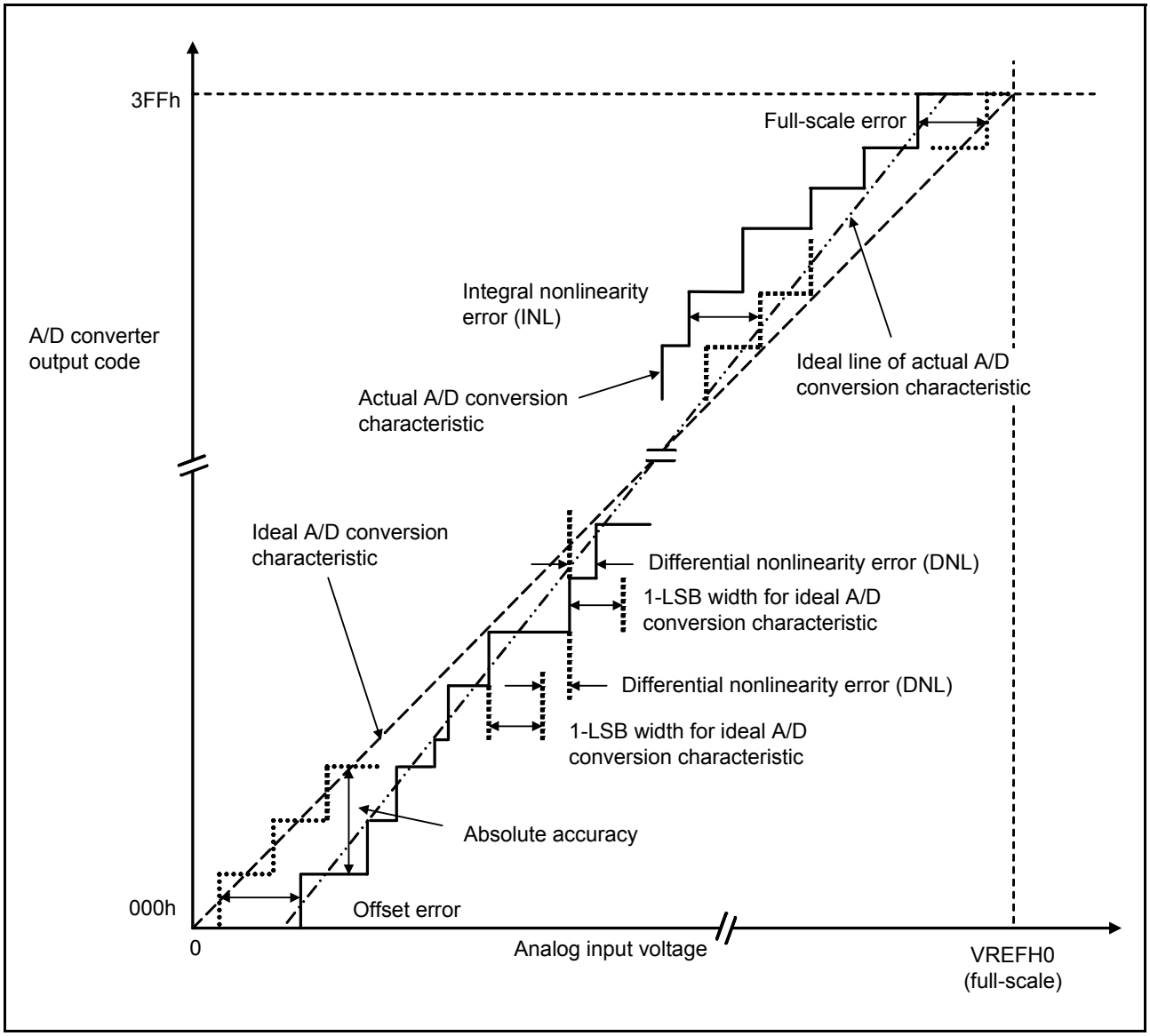


Figure 5.62 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if reference voltage VREFH0 = 2.56 V, then 1-LSB width becomes 2.5 mV, and 0 mV, 2.5 mV, 5.0 mV, ... are used as analog input voltages.

If analog input voltage is 20 mV, absolute accuracy = ±4 LSB means that the actual A/D conversion result is in the range of 004h to 00Ch though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

5.7 D/A Conversion Characteristics

Table 5.40 D/A Conversion Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

Table 5.41 D/A Conversion Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH =1.8 V to AVCC0,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	10.0	µs	20-pF capacitive load
Absolute accuracy	—	±5.0	±6.0	LSB	4-MΩ resistive load
	—	—	±5.0	LSB	8-MΩ resistive load
RO output resistance	—	4.1	—	kΩ	

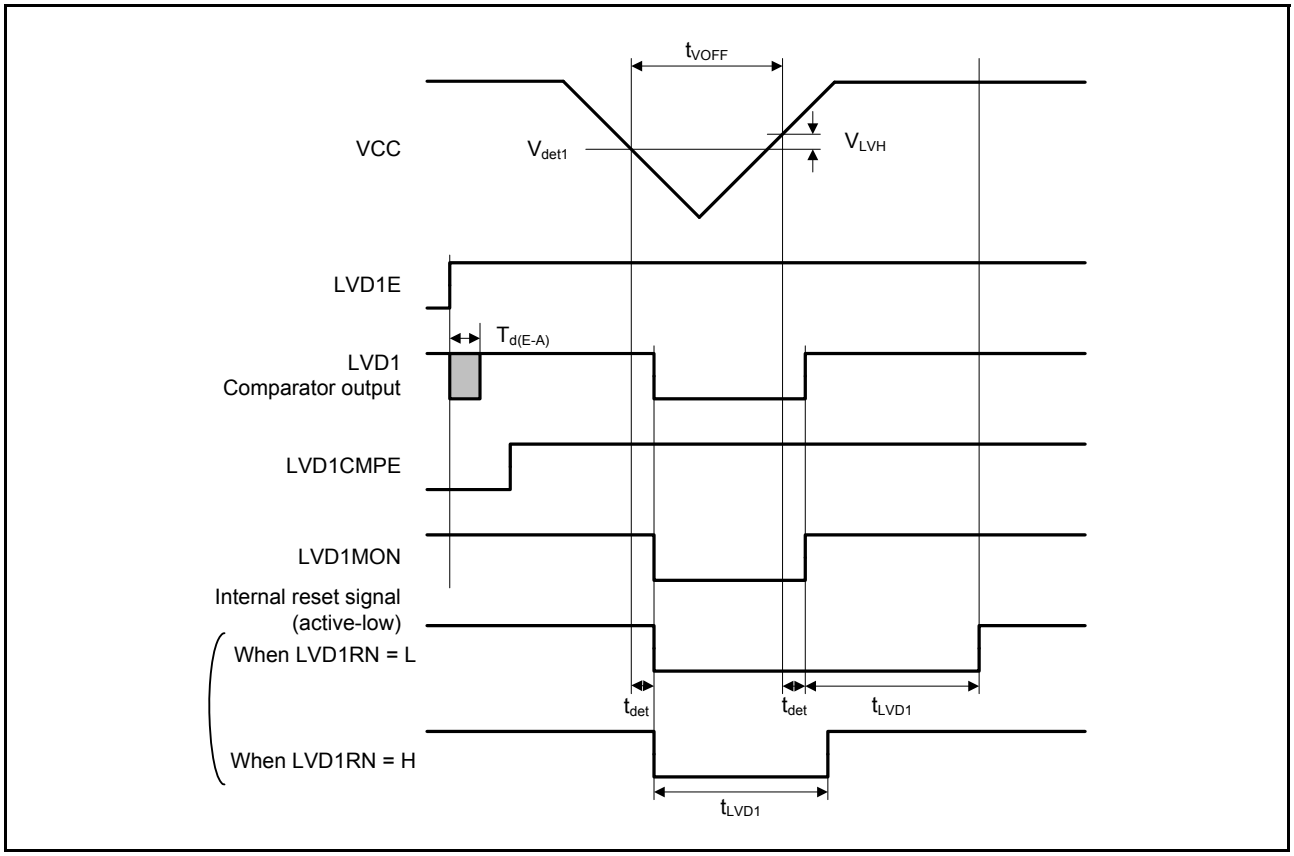


Figure 5.67 Voltage Detection Circuit Timing (V_{det1})

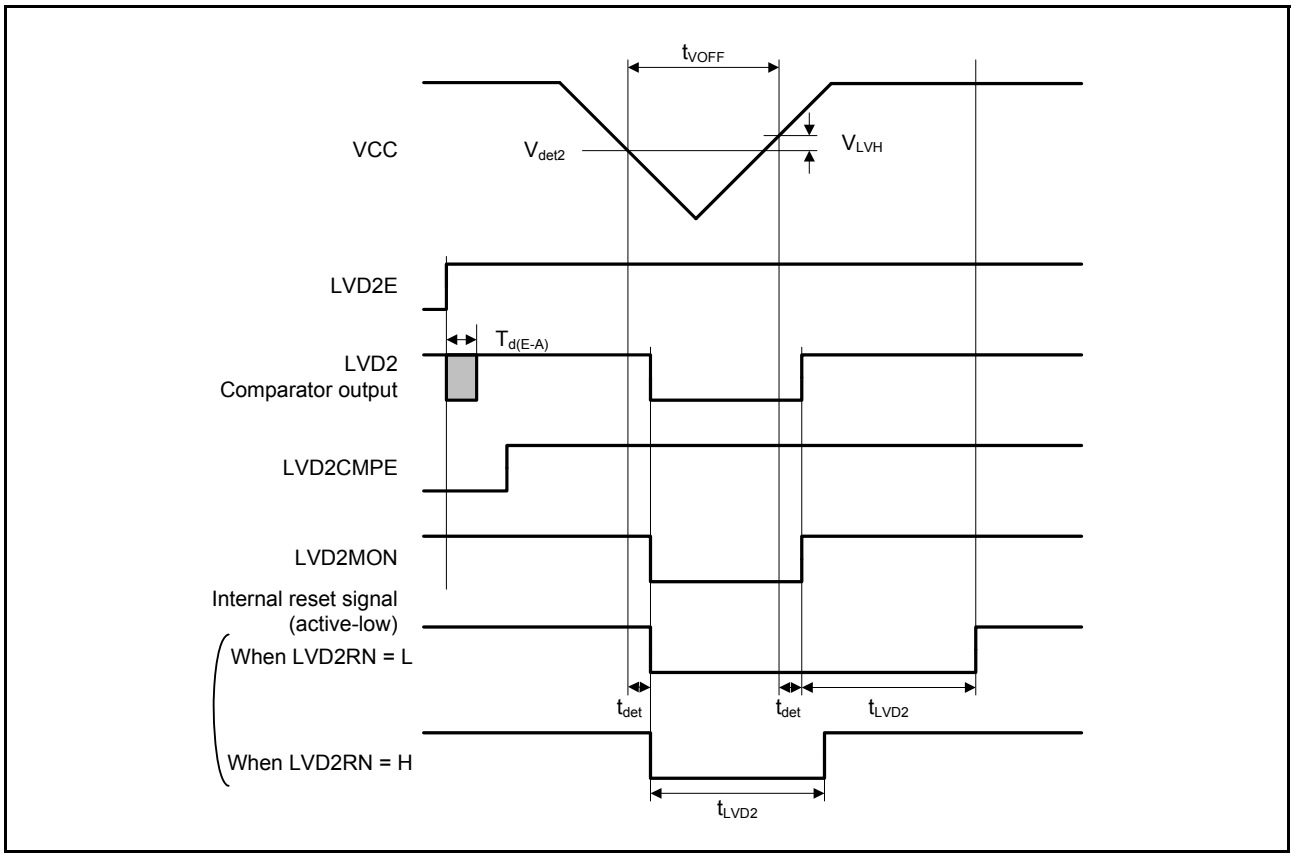
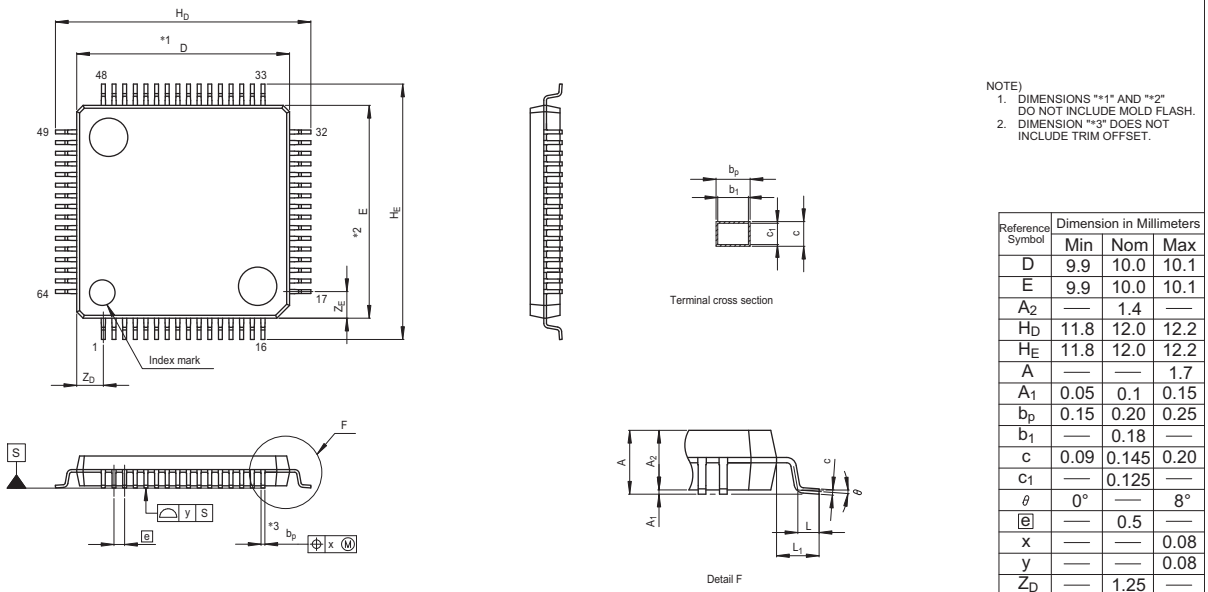


Figure 5.68 Voltage Detection Circuit Timing (V_{det2})

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 64-Pin LQFP (PLQP0064KB-A)