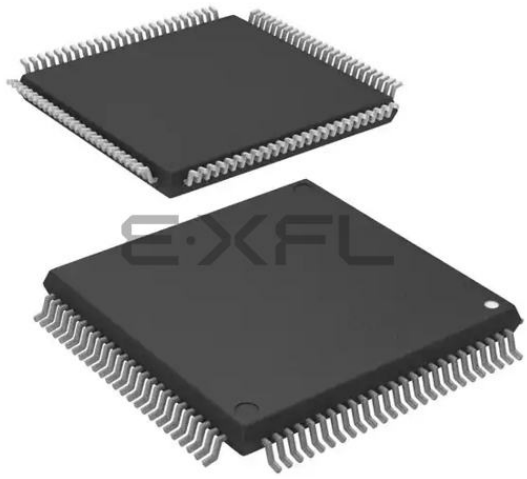
Renesas Electronics America Inc - R5F521A6BDFP#V0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdfp-v0

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating temperature
RX21A	R5F521A8BDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F521A8BDFN	PLQP0080KB-A					
	R5F521A8BDFM	PLQP0064KB-A					
	R5F521A8BDLJ	PTLG0100JA-A					
	R5F521A7BDFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BDFN	PLQP0080KB-A					
	R5F521A7BDFM	PLQP0064KB-A					
	R5F521A7BDLJ	PTLG0100JA-A					
	R5F521A6BDFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BDFN	PLQP0080KB-A					
	R5F521A6BDFM	PLQP0064KB-A					
	R5F521A6BDLJ	PTLG0100JA-A					
	R5F521A8BGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +105°C *1, *2
	R5F521A8BGFN	PLQP0080KB-A					
	R5F521A8BGFM	PLQP0064KB-A					
	R5F521A7BGFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BGFN	PLQP0080KB-A					
	R5F521A7BGFM	PLQP0064KB-A					
	R5F521A6BGFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BGFN	PLQP0080KB-A					
	R5F521A6BGFM	PLQP0064KB-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 2. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
section 37.3, Using the Temperature Sensor
section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
42		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
44		PB4		CTS9#/RTS9#/SS9#	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
46		PB2		CTS6#/RTS6#/SS6#	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
48	VCC				
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	CMPB0
50	VSS				
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
52		PA5		RSPCKA	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0	IRQ5-DS/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/IRRXD5	IRQ6-DS/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	CMPA2
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
57		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
58	BGR_BO				
59					ANDS0N
60					ANDS0P
61					ANDS1N
62					ANDS1P
63	AVSSA				
64	AVCCA				
65	VREFDSL				
66	VREFDSH				
67	VCOMDS				
68					ANDS4
69					ANDS5
70	ANDSSG				
71		P43			AN3
72		P42			AN2
73		P41			AN1
74	VREFL0				
75		P40			AN0
76	VREFH0				
77	AVCC0				
78		P07			AN6/ADTRG0#
79	AVSS0				
80		P05			AN5/DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
J2		P21	MTIOC1B/TMCI0	SCL1	
J3		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
J4		P13	MTIOC0B/TMO3	SDA0	IRQ3
J5		PH0			CACREF
J6		PH3	TMCI0		
J7		P50		SSLB1	
J8		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
J9		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
J10		PC1	MTIOC3A	SCK5/SSLA2	
K1		P23	MTIOC3D/MTCLKD		
K2		P22	MTIOC3B/MTCLKC/TMO0		
K3		P20	MTIOC1A/TMRI0	SDA1	
K4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2	TMRI0		IRQ1
K6		PH1	TMO0		IRQ0
K7		P51		SSLB2	
K8		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
K9		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
K10		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16		3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16		3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16		3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16		3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32		3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32		3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32		3 ICLK
0008 001Ch	SYSTEM	Module stop control register D	MSTPCRD	32	32		3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32		3 ICLK
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16		3 ICLK
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16		3 ICLK
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8		3 ICLK
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8		3 ICLK
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8		3 ICLK
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8		3 ICLK
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8		3 ICLK
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8		3 ICLK
0008 0037h	SYSTEM	High-speed on-chip oscillator control register 2	HOCOCR2	8	8		3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8		3 ICLK
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8		3 ICLK
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8		3 ICLK
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8		3 ICLK
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8		3 ICLK
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8		3 ICLK
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8		3 ICLK
0008 00A9h	SYSTEM	HOCO wait control register 2	HOCOWTCR2	8	8		3 ICLK
0008 00C0h	SYSTEM	Reset status register 2	RSTSR2	8	8		3 ICLK
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16		3 ICLK
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 control register 1	LVD1CR1	8	8		3 ICLK
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit/comparator A1 status register	LVD1SR	8	8		3 ICLK
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 control register 1	LVD2CR1	8	8		3 ICLK
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit/comparator A2 status register	LVD2SR	8	8		3 ICLK
0008 03FEh	SYSTEM	Protect register	PRCR	16	16		3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8		2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8		2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8		2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16		2 ICLK
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16		2 ICLK
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32		2 ICLK
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16		2 ICLK
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32		2 ICLK
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8		2 ICLK
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8		2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8		2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8		2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8		2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8		2 ICLK
0008 716Bh	ICU	DTC activation enable register 107	DTCER107	8	8		2 ICLK
0008 716Ch	ICU	DTC activation enable register 108	DTCER108	8	8		2 ICLK
0008 716Dh	ICU	DTC activation enable register 109	DTCER109	8	8		2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8		2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8		2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8		2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8		2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8		2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8		2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8		2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8		2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8		2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8		2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8		2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8		2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8		2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8		2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8		2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8		2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8		2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8		2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8		2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8		2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8		2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8		2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8		2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8		2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8		2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8		2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8		2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8		2 ICLK
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8		2 ICLK
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8		2 ICLK
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8		2 ICLK
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8		2 ICLK
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8		2 ICLK
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8		2 ICLK
0008 71D1h	ICU	DTC activation enable register 209	DTCER209	8	8		2 ICLK
0008 71D2h	ICU	DTC activation enable register 210	DTCER210	8	8		2 ICLK
0008 71D3h	ICU	DTC activation enable register 211	DTCER211	8	8		2 ICLK
0008 71D4h	ICU	DTC activation enable register 212	DTCER212	8	8		2 ICLK
0008 71D5h	ICU	DTC activation enable register 213	DTCER213	8	8		2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8		2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8		2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8		2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 B444h	DSAD	ΔΣ A/D data register 3	DSADDR3	32	32	2, 3 PCLKB	2 ICLK
0008 B448h	DSAD	ΔΣ A/D input select register 3	DSADISR3	8	8	2, 3 PCLKB	2 ICLK
0008 B450h	DSAD	ΔΣ A/D control register 4	DSADCR4	8	8	2, 3 PCLKB	2 ICLK
0008 B451h	DSAD	ΔΣ A/D control/status register 4	DSADCSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B452h	DSAD	ΔΣ A/D gain select register 4	DSADGSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B453h	DSAD	ΔΣ A/D overwrite flag register 4	DSADFR4	8	8	2, 3 PCLKB	2 ICLK
0008 B454h	DSAD	ΔΣ A/D data register 4	DSADDR4	32	32	2, 3 PCLKB	2 ICLK
0008 B458h	DSAD	ΔΣ A/D input select register 4	DSADISR4	8	8	2, 3 PCLKB	2 ICLK
0008 B460h	DSAD	ΔΣ A/D control register 5	DSADCR5	8	8	2, 3 PCLKB	2 ICLK
0008 B461h	DSAD	ΔΣ A/D control/status register 5	DSADCSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B462h	DSAD	ΔΣ A/D gain select register 5	DSADGSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B463h	DSAD	ΔΣ A/D overwrite flag register 5	DSADFR5	8	8	2, 3 PCLKB	2 ICLK
0008 B464h	DSAD	ΔΣ A/D data register 5	DSADDR5	32	32	2, 3 PCLKB	2 ICLK
0008 B468h	DSAD	ΔΣ A/D input select register 5	DSADISR5	8	8	2, 3 PCLKB	2 ICLK
0008 B470h	DSAD	ΔΣ A/D control register 6	DSADCR6	8	8	2, 3 PCLKB	2 ICLK
0008 B471h	DSAD	ΔΣ A/D control/status register 6	DSADCSR6	8	8	2, 3 PCLKB	2 ICLK
0008 B472h	DSAD	ΔΣ A/D gain select register 6	DSADGSR6	8	8	2, 3 PCLKB	2 ICLK
0008 B473h	DSAD	ΔΣ A/D overwrite flag register 6	DSADFR6	8	8	2, 3 PCLKB	2 ICLK
0008 B474h	DSAD	ΔΣ A/D data register 6	DSADDR6	32	32	2, 3 PCLKB	2 ICLK
0008 B478h	DSAD	ΔΣ A/D input select register 6	DSADISR6	8	8	2, 3 PCLKB	2 ICLK
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C011h	PORTH	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C031h	PORTH	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK
0008 C040h	PORT0	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C041h	PORT1	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing

Table 4.1 List of I/O Registers (Address Order) (23 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C474h	RTC	Minute capture register 2/BCNT1 capture register 2	RMINCP2/ BCNT1CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C476h	RTC	Hour capture register 2/BCNT2 capture register 2	RHRCP2/ BCNT2CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ah	RTC	Date capture register 2/BCNT3 capture register 2	RDAYCP2/ BCNT3CP2	8	8	2, 3 PCLKB	2 ICLK
0008 C47Ch	RTC	Month capture register 2	RMONCP2	8	8	2, 3 PCLKB	2 ICLK
0008 C500h	TEMPS	Temperature sensor control register	TSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C580h	CMPB	Comparator B control register 1	CPBCNT1	8	8	2, 3 PCLKB	2 ICLK
0008 C582h	CMPB	Comparator B flag register	CPBFLG	8	8	2, 3 PCLKB	2 ICLK
0008 C583h	CMPB	Comparator B interrupt control register	CPBINT	8	8	2, 3 PCLKB	2 ICLK
0008 C584h	CMPB	Comparator B filter select register	CPBF	8	8	2, 3 PCLKB	2 ICLK
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 FCLK	2 ICLK
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 FCLK	2 ICLK
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 FCLK	2 ICLK
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 FCLK	2 ICLK
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2, 3 FCLK	2 ICLK
007F C450h	FLASH	E2 DataFlash programming/erasure enable register 0	DFLWE0	16	16	2, 3 FCLK	2 ICLK
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 FCLK	2 ICLK
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 FCLK	2 ICLK
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 FCLK	2 ICLK
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2, 3 FCLK	2 ICLK
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 FCLK	2 ICLK
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 FCLK	2 ICLK
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 FCLK	2 ICLK
007F FFCAh	FLASH	E2 DataFlash blank check control register	DFLBCCNT	16	16	2, 3 FCLK	2 ICLK
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 FCLK	2 ICLK
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2, 3 FCLK	2 ICLK
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 FCLK	2 ICLK
FEFF FAC0h	FLASH	Unique ID register 0*3	UIDR0	32	32	1ICLK	
FEFF FAC4h	FLASH	Unique ID register 1*3	UIDR1	32	32	1ICLK	
FEFF FAC8h	FLASH	Unique ID register 2*3	UIDR2	32	32	1ICLK	
FEFF FACCh	FLASH	Unique ID register 3*3	UIDR3	32	32	1ICLK	
FEFF FAD0h	TEMPS	Temperature sensor calibration data register 0*3	TSCDR0	32	32	1ICLK	
FEFF FAD4h	TEMPS	Temperature sensor calibration data register 1*3	TSCDR1	32	32	1ICLK	
FEFF FADCh	TEMPS	Temperature sensor calibration data register 3*3	TSCDR3	32	32	1ICLK	
FEFF FB30h	DSAD	ΔΣA/D gain calibration data register 0 X1*3	DSADG0X1	32	32	1ICLK	
FEFF FB34h	DSAD	ΔΣA/D gain calibration data register 1 X1*3	DSADG1X1	32	32	1ICLK	
FEFF FB38h	DSAD	ΔΣA/D gain calibration data register 2 X1*3	DSADG2X1	32	32	1ICLK	
FEFF FB3Ch	DSAD	ΔΣA/D gain calibration data register 3 X1*3	DSADG3X1	32	32	1ICLK	
FEFF FB40h	DSAD	ΔΣA/D gain calibration data register 4 X1*3	DSADG4X1	32	32	1ICLK	
FEFF FB44h	DSAD	ΔΣA/D gain calibration data register 5 X1*3	DSADG5X1	32	32	1ICLK	
FEFF FB48h	DSAD	ΔΣA/D gain calibration data register 6 X1*3	DSADG6X1	32	32	1ICLK	
FEFF FB50h	DSAD	ΔΣA/D gain calibration data register 0 X2*3	DSADG0X2	32	32	1ICLK	
FEFF FB54h	DSAD	ΔΣA/D gain calibration data register 1 X2*3	DSADG1X2	32	32	1ICLK	
FEFF FB58h	DSAD	ΔΣA/D gain calibration data register 2 X2*3	DSADG2X2	32	32	1ICLK	
FEFF FB5Ch	DSAD	ΔΣA/D gain calibration data register 3 X2*3	DSADG3X2	32	32	1ICLK	
FEFF FB60h	DSAD	ΔΣA/D gain calibration data register 4 X2*3	DSADG4X2	32	32	1ICLK	
FEFF FB64h	DSAD	ΔΣA/D gain calibration data register 5 X2*3	DSADG5X2	32	32	1ICLK	
FEFF FB68h	DSAD	ΔΣA/D gain calibration data register 6 X2*3	DSADG6X2	32	32	1ICLK	
FEFF FB70h	DSAD	ΔΣA/D gain calibration data register 0 X4*3	DSADG0X4	32	32	1ICLK	

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz	I_{CC}	5.9	—	mA	
			All peripheral operation: Normal*4	ICLK = 25 MHz		8.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	38		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		4.1	—		
			All peripheral operation: Normal	ICLK = 25 MHz		6.2	—		
		All-module clock stop mode		ICLK = 25 MHz		3.6	—		
		Increase during BGO operation*2	Medium-speed operating mode 1A			23	—		
			Medium-speed operating mode 1B			20	—		
	Medium-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz		5.4	—		
				ICLK = 12.5 MHz		3.9	—		
			All peripheral operation: Normal*4	ICLK = 25 MHz		7.4	—		
				ICLK = 12.5 MHz		5.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	37		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		3.5	—		
				ICLK = 12.5 MHz		3.0	—		
			All peripheral operation: Normal	ICLK = 25 MHz		5.6	—		
				ICLK = 12.5 MHz		4.1	—		
		All-module clock stop mode		ICLK = 25 MHz		3.0	—		
				ICLK = 12.5 MHz		2.7	—		
		Increase during BGO operation*2	Medium-speed operating mode 2A			23	—		
			Medium-speed operating mode 2B			20	—		

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*6	ICLK = 8 MHz	I_{CC}	1.9	—	mA	
				ICLK = 4 MHz		1.2	—		
			All peripheral operation: Normal*7	ICLK = 8 MHz		2.5	—		
				ICLK = 4 MHz		1.7	—		
			All peripheral operation: Max.*8	ICLK = 8 MHz		—	12		
		Sleep mode	No peripheral operation	ICLK = 8 MHz		1.3	—		
				ICLK = 4 MHz		0.9	—		
			All peripheral operation: Normal	ICLK = 8 MHz		1.9	—		
				ICLK = 4 MHz		1.3	—		
		All-module clock stop mode		ICLK = 8 MHz		1.1	—		
				ICLK = 4 MHz		0.9	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*9	ICLK = 32 kHz		0.027	—		
			All peripheral operation: Normal*10	ICLK = 32 kHz		0.030	—		
			All peripheral operation: Max.*11	ICLK = 32 kHz		—	1.0		
		Sleep mode	No peripheral operation	ICLK = 32 kHz		0.022	—		
			All peripheral operation: Normal	ICLK = 32 kHz		0.025	—		
		All-module clock stop mode		ICLK = 32 kHz		0.022	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are ICLK divided by 1.
Note 6. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are ICLK divided by 1.

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	20	µA	
			T_a = 55°C		12	41		
			T_a = 85°C		18	113		
			T_a = 105°C		29	233		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.7	7.9		
			T_a = 55°C		2.7	25		
			T_a = 85°C		7.0	86		
			T_a = 105°C		16	189		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled	T_a = 25°C		0.3	0.8		
			T_a = 55°C		0.4	1.1		
			T_a = 85°C		0.8	2.2		
			T_a = 105°C		1.3	4.7		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.2	—		
	Increment for RTC operation (low CL)				0.6	—		
	Increment for RTC operation (standard CL)				1.4	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

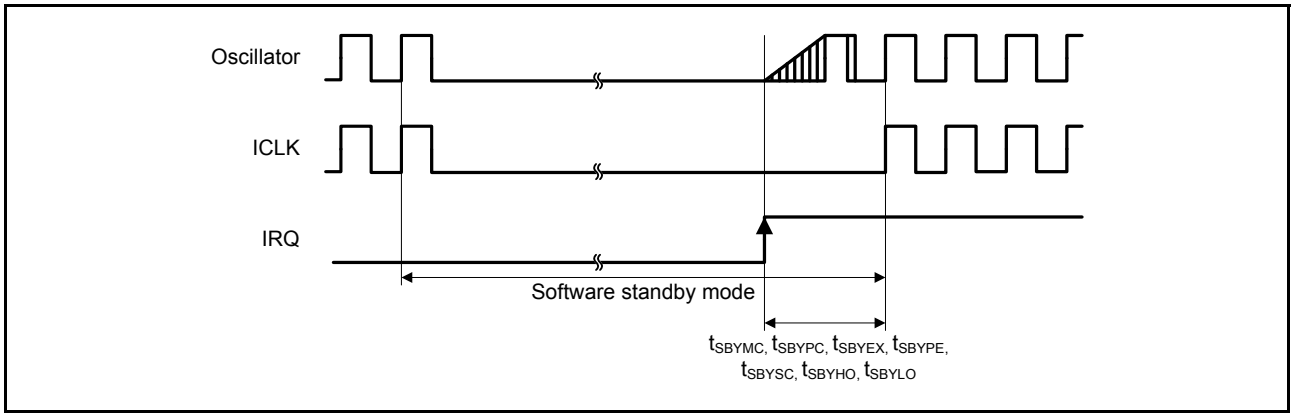


Figure 5.37 Software Standby Mode Cancellation Timing

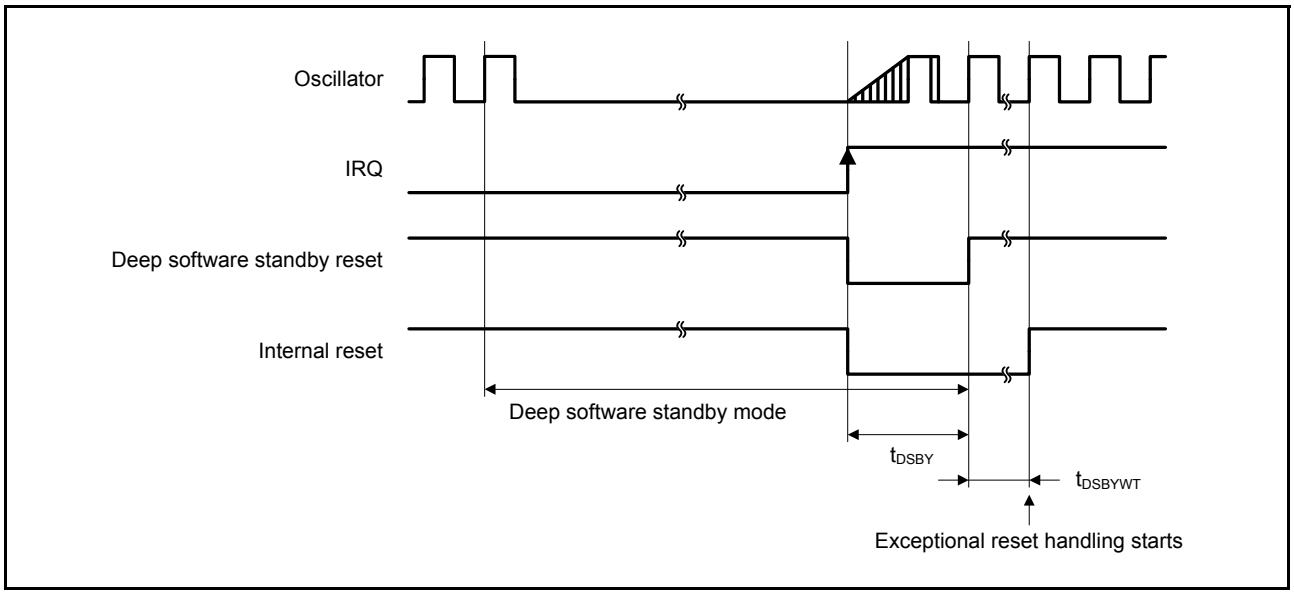


Figure 5.38 Deep Software Standby Mode Cancellation Timing

Table 5.32 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C
When high-drive output is selected by the drive capacity register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SPcyc}	2	4096	t_{Pcyc}	C = 30 pF Figure 5.49
		Master 1.8 V ≤ VCC < 2.7 V		4	4096		
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	10	ns	
		Input		—	1	µs	
	Data input setup time	Master 2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	4	—	ns	C = 30 pF Figure 5.50 to Figure 5.53
		Master 1.8 V ≤ VCC < 2.7 V		16	—		
		Slave		$20 - t_{Pcyc}$	—		
	Data input hold time	Master	t_H	t_{Pcyc}	—	ns	
		Slave		$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	—	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	—	10	ns	
		Slave 2.7 V ≤ VCC ≤ 3.6 V		—	$3 \times t_{Pcyc} + 55$		
		Slave 1.8 V ≤ VCC < 2.7 V		—	$3 \times t_{Pcyc} + 72$		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	10	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	20	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	5	t_{Pcyc}	C = 30 pF Figure 5.52 and Figure 5.53
	Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	4	t_{Pcyc}	
		1.8 V ≤ VCC < 2.7 V		—	5		

Note 1. t_{Pcyc}: PCLK cycle

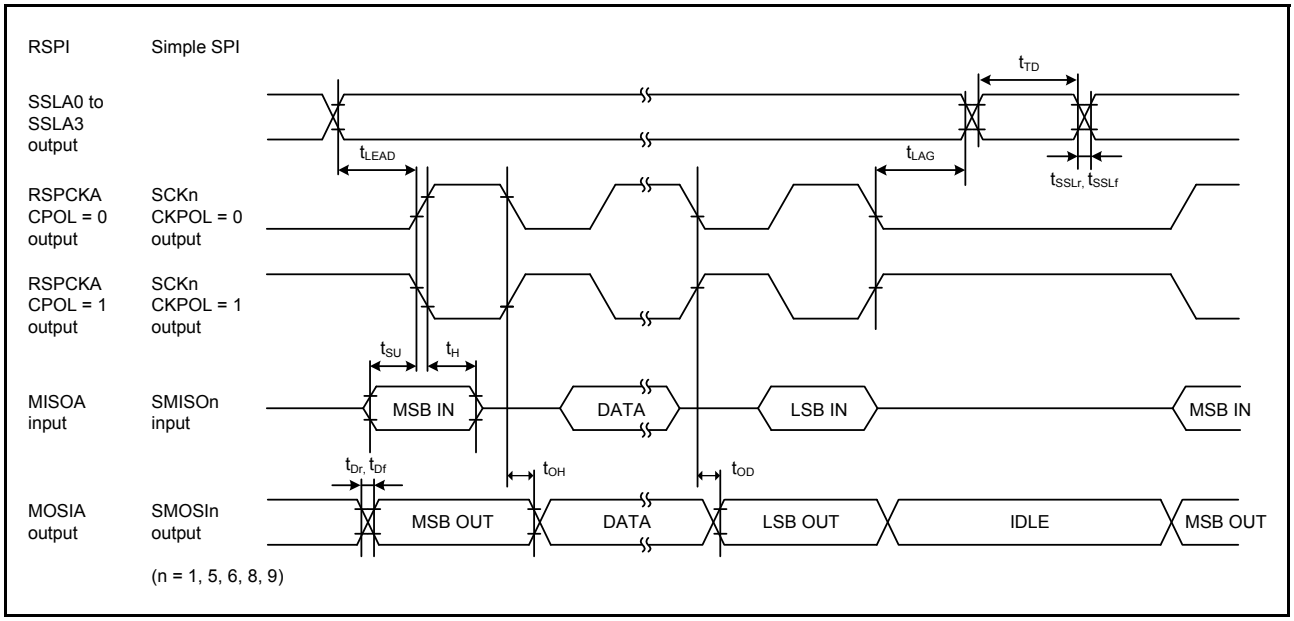


Figure 5.50 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

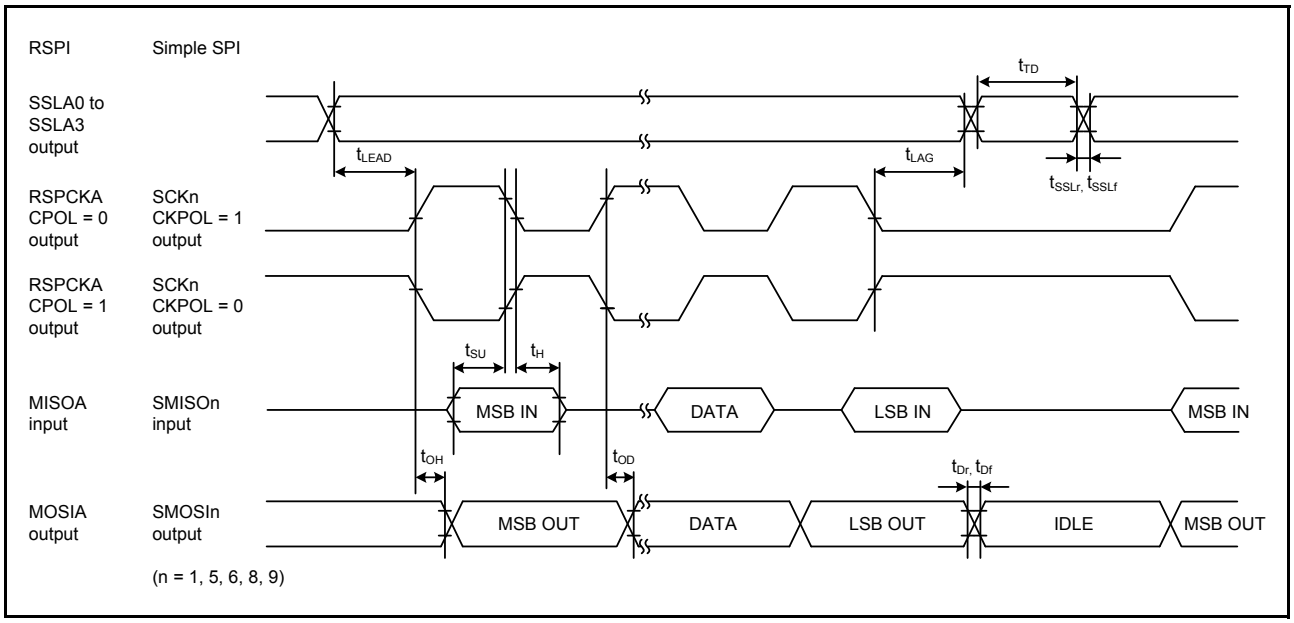


Figure 5.51 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

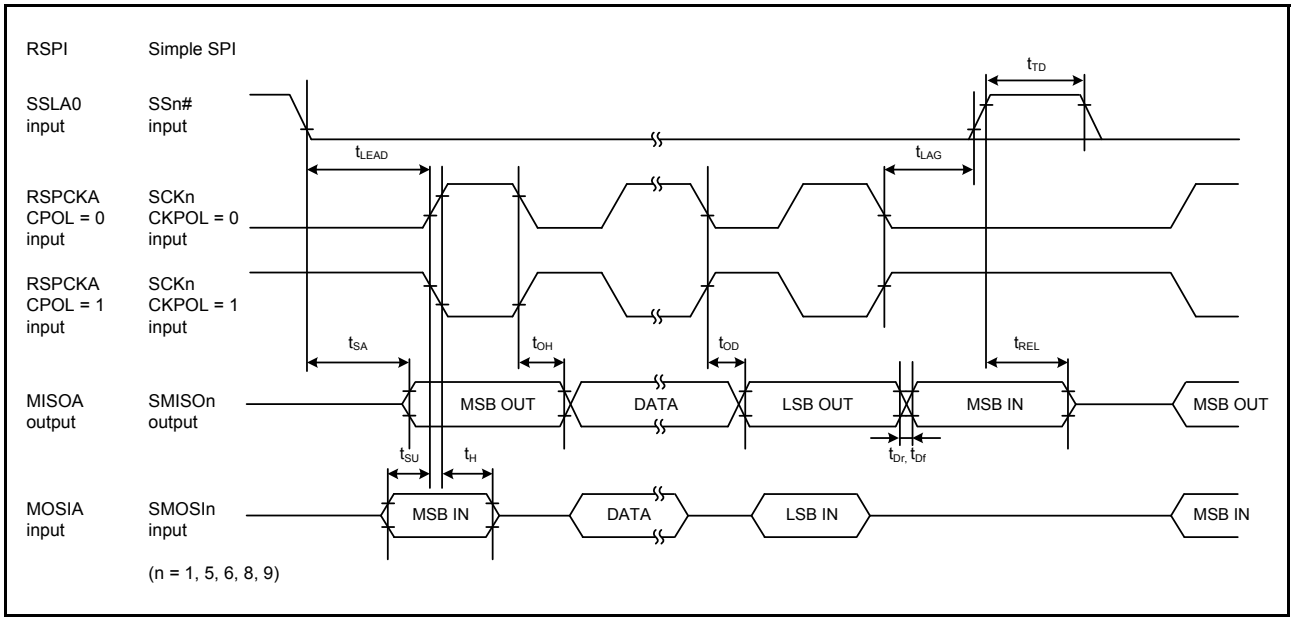


Figure 5.52 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

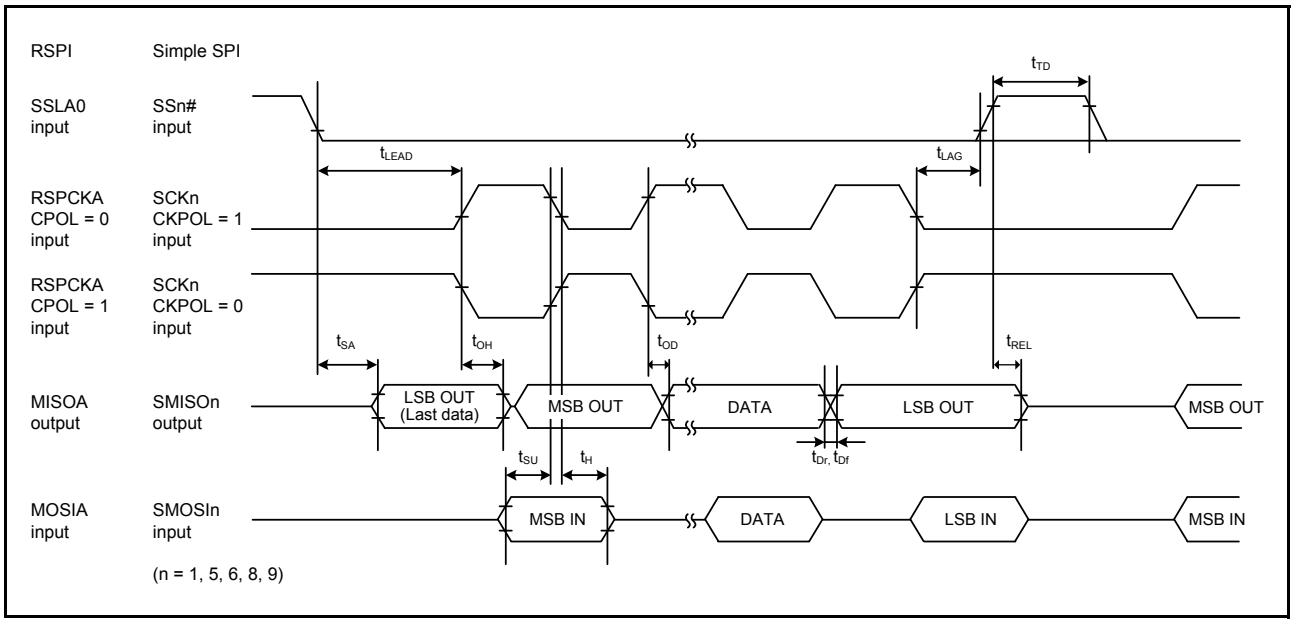
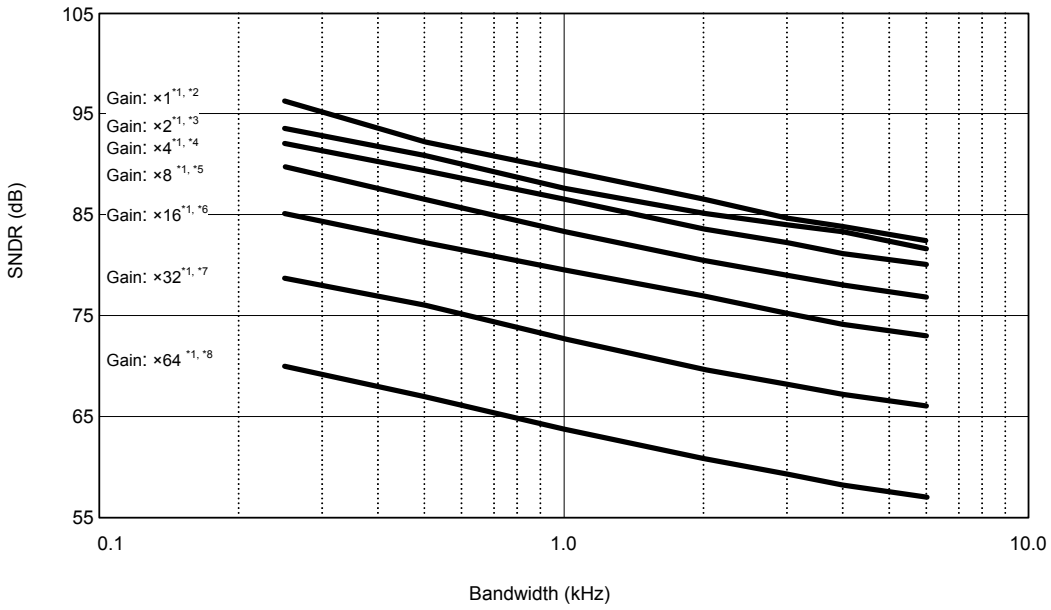


Figure 5.53 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)



Note 1. Input frequency: 50 Hz, sampling period: 81.92 µs
Note 2. Input amplitude: 500.0 mV
Note 3. Input amplitude: 250.0 mV
Note 4. Input amplitude: 125.0 mV
Note 5. Input amplitude: 62.5 mV
Note 6. Input amplitude: 31.2 mV
Note 7. Input amplitude: 14.4 mV
Note 8. Input amplitude: 5.0 mV

Figure 5.60 Bandwidth Dependency of SNDR (Reference Data)

5.11 Oscillation Stop Detection Timing

Table 5.46 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.69

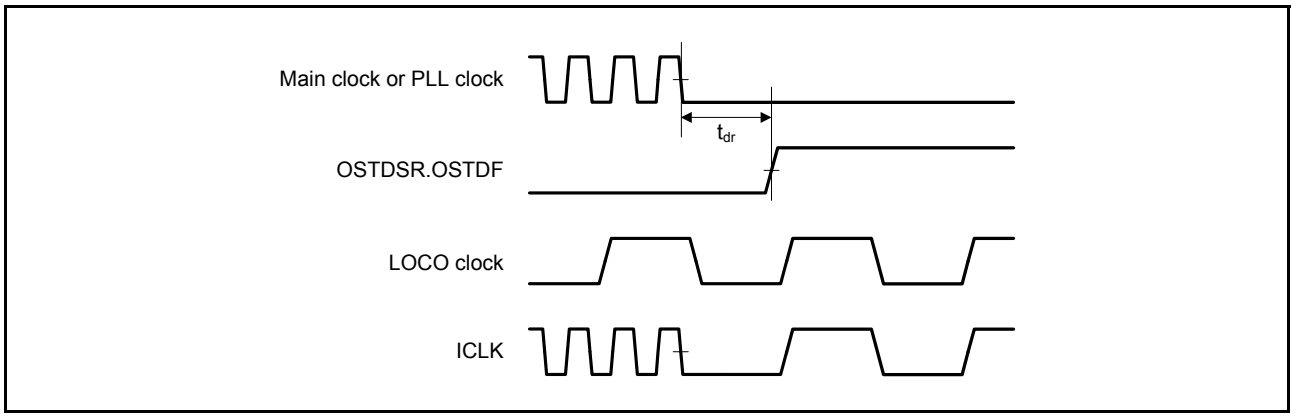
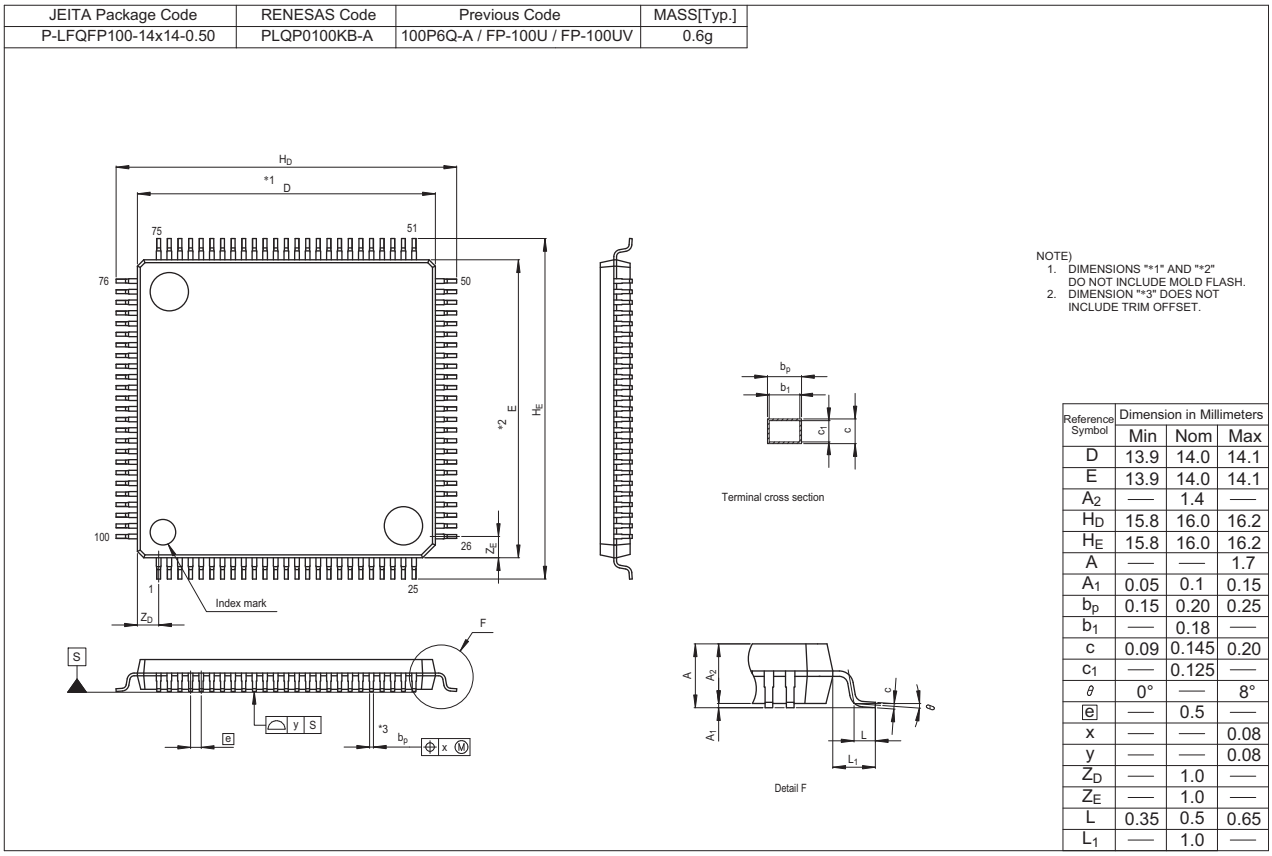


Figure 5.69 Oscillation Stop Detection Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

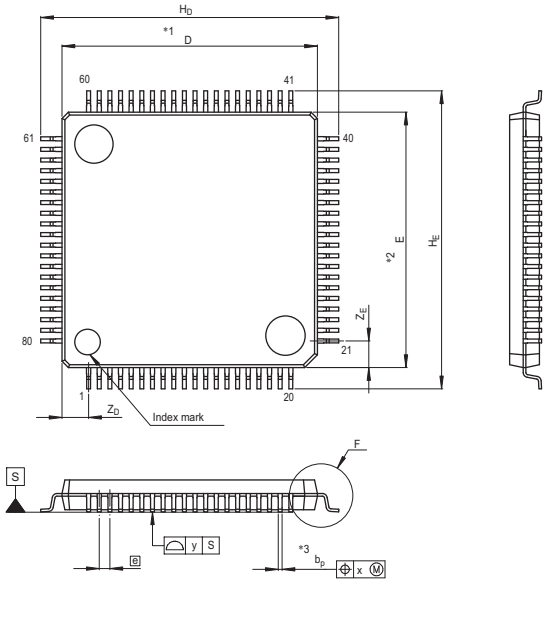
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 80-Pin LQFP (PLQP0080KB-A)