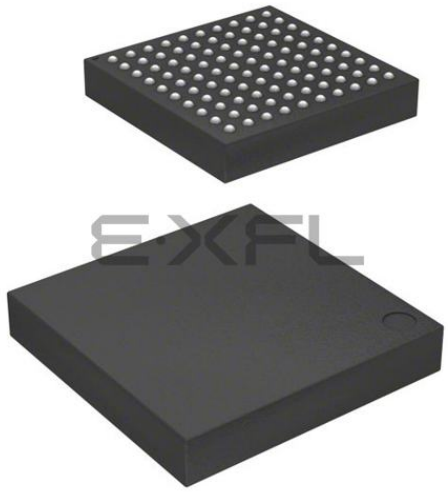


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a6bdlj-u0

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating temperature
RX21A	R5F521A8BDFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +85°C
	R5F521A8BDFN	PLQP0080KB-A					
	R5F521A8BDFM	PLQP0064KB-A					
	R5F521A8BDLJ	PTLG0100JA-A					
	R5F521A7BDFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BDFN	PLQP0080KB-A					
	R5F521A7BDFM	PLQP0064KB-A					
	R5F521A7BDLJ	PTLG0100JA-A					
	R5F521A6BDFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BDFN	PLQP0080KB-A					
	R5F521A6BDFM	PLQP0064KB-A					
	R5F521A6BDLJ	PTLG0100JA-A					
	R5F521A8BGFP	PLQP0100KB-A	512 Kbytes	64 Kbytes	8 Kbytes	50 MHz	–40 to +105°C *1, *2
	R5F521A8BGFN	PLQP0080KB-A					
	R5F521A8BGFM	PLQP0064KB-A					
	R5F521A7BGFP	PLQP0100KB-A	384 Kbytes				
	R5F521A7BGFN	PLQP0080KB-A					
	R5F521A7BGFM	PLQP0064KB-A					
	R5F521A6BGFP	PLQP0100KB-A	256 Kbytes	32 Kbytes			
	R5F521A6BGFN	PLQP0080KB-A					
	R5F521A6BGFM	PLQP0064KB-A					

Note: • Orderable part numbers are current as of when this manual was published. Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 2. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
section 37.3, Using the Temperature Sensor
section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 0.1 µF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCIN and XCOUT.
	XCOUT	Output	
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This LSI enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.
Realtime clock	RTCOUT	Output	Output pin for 1-Hz, 64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.

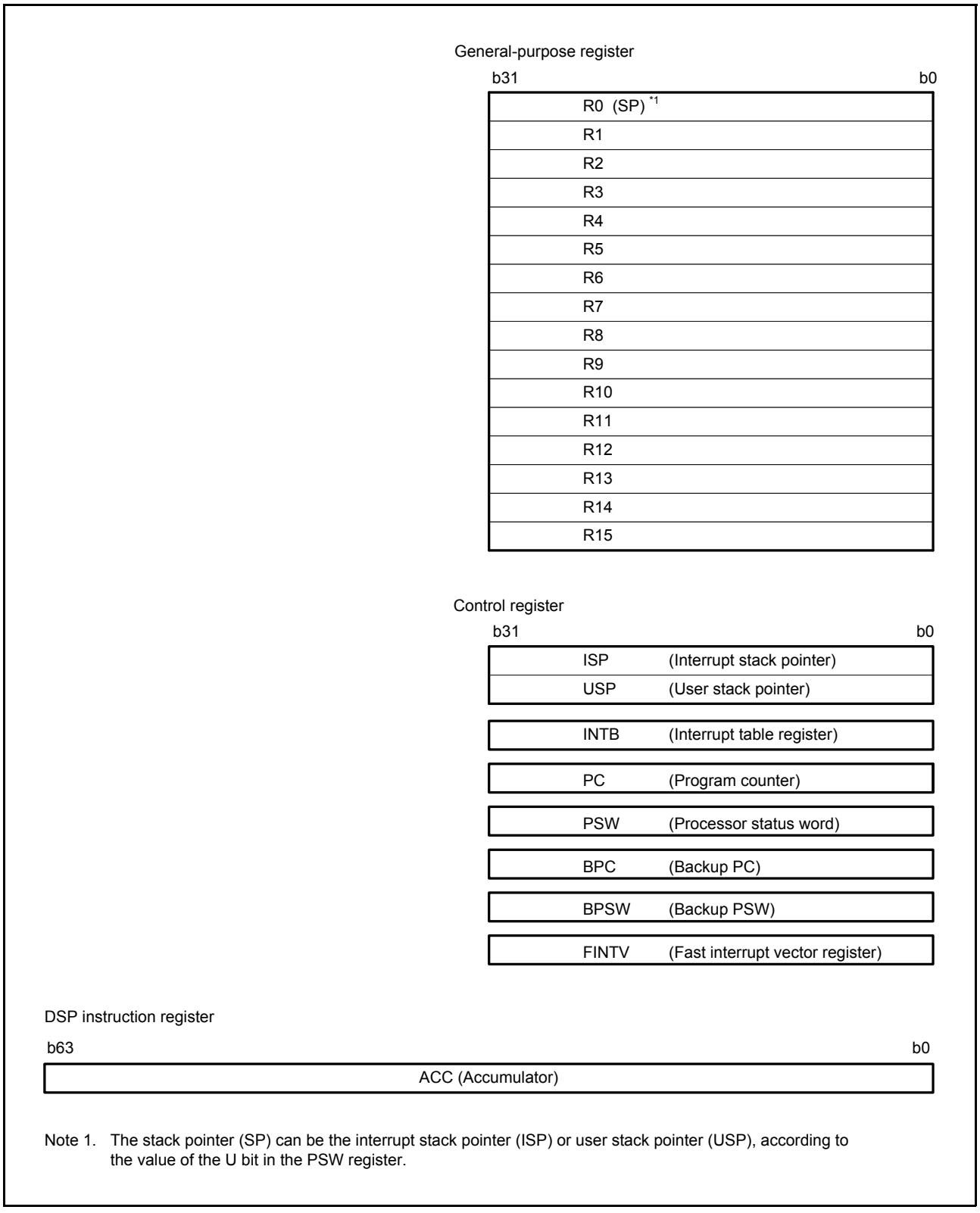
Table 1.7 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
37		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
46	BGR_BO				
47					ANDS0N
48					ANDS0P
49					ANDS1N
50					ANDS1P
51	AVSSA				
52	AVCCA				
53	VREFDSL				
54	VREFDSH				
55	VCOMDS				
56					ANDS4
57	ANDSSG				
58		P41			AN1
59	VREFL0				
60		P40			AN0
61	VREFH0				
62	AVCC0				
63		P05			AN5
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

This CPU has the following eight control registers.

(1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C042h	PORT2	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C043h	PORT3	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C044h	PORT4	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C045h	PORT5	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C051h	PORTH	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C052h	PORTJ	Port input data register	PIDR	8	8	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing
0008 C060h	PORT0	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C061h	PORT1	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C071h	PORTH	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK

Table 5.6 DC Characteristics (5)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*3	ICLK = 50 MHz	I_{CC}	8.6	—	mA	
			All peripheral operation: Normal*4	ICLK = 50 MHz		13	—		
			All peripheral operation: Max.*5	ICLK = 50 MHz		—	59		
		Sleep mode	No peripheral operation	ICLK = 50 MHz		4.9	—		
			All peripheral operation: Normal	ICLK = 50 MHz		9.0	—		
		All-module clock stop mode		ICLK = 50 MHz		3.9	—		
		Increase during BGO operation*2				23	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. PCLKA is ICLK divided by 1. FCLK, PCLKB, PCLKC, and PCLKD are ICLK divided by 2.

Table 5.7 DC Characteristics (6)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Medium-speed operating modes 1A and 1B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz	I_{CC}	5.9	—	mA	
			All peripheral operation: Normal*4	ICLK = 25 MHz		8.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	38		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		4.1	—		
			All peripheral operation: Normal	ICLK = 25 MHz		6.2	—		
		All-module clock stop mode		ICLK = 25 MHz		3.6	—		
		Increase during BGO operation*2	Medium-speed operating mode 1A			23	—		
			Medium-speed operating mode 1B			20	—		
	Medium-speed operating modes 2A and 2B	Normal operating mode	No peripheral operation*3	ICLK = 25 MHz		5.4	—		
				ICLK = 12.5 MHz		3.9	—		
			All peripheral operation: Normal*4	ICLK = 25 MHz		7.4	—		
				ICLK = 12.5 MHz		5.0	—		
			All peripheral operation: Max.*5	ICLK = 25 MHz		—	37		
		Sleep mode	No peripheral operation	ICLK = 25 MHz		3.5	—		
				ICLK = 12.5 MHz		3.0	—		
			All peripheral operation: Normal	ICLK = 25 MHz		5.6	—		
				ICLK = 12.5 MHz		4.1	—		
		All-module clock stop mode		ICLK = 25 MHz		3.0	—		
				ICLK = 12.5 MHz		2.7	—		
		Increase during BGO operation*2	Medium-speed operating mode 2A			23	—		
			Medium-speed operating mode 2B			20	—		

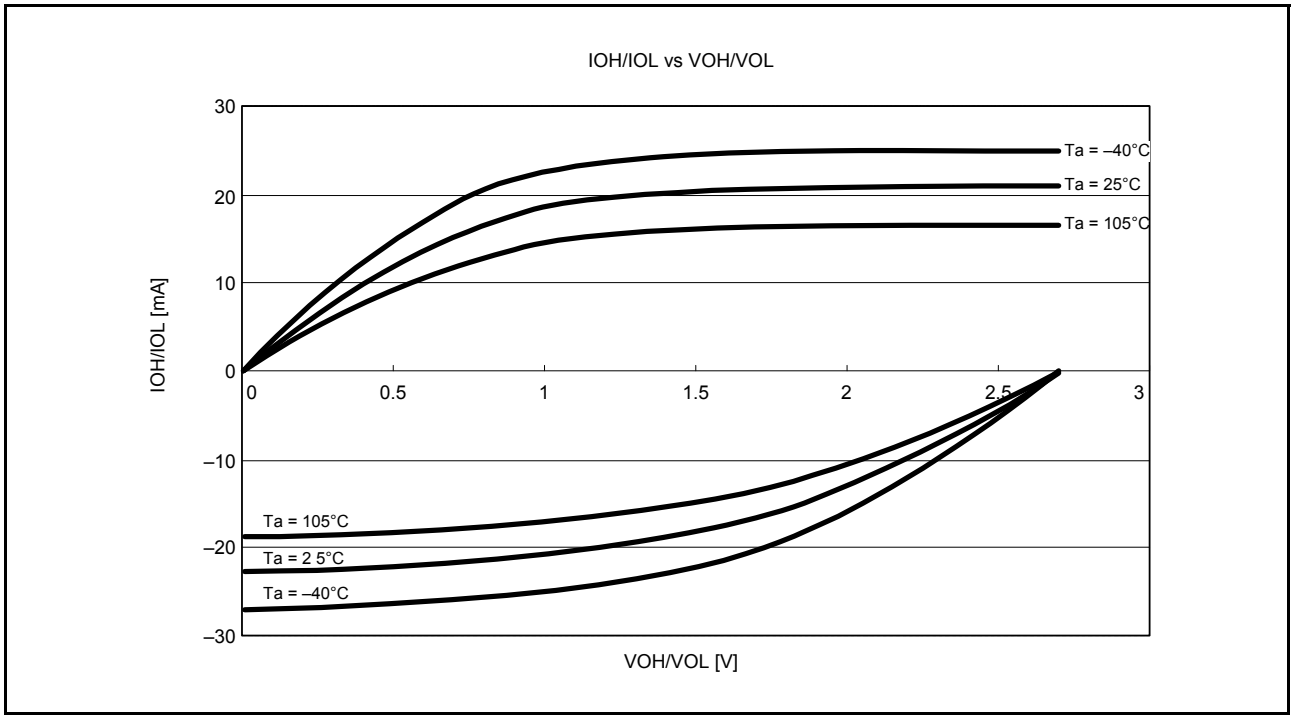


Figure 5.18 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 2.7 V when High-Drive Output is Selected (Reference Data)

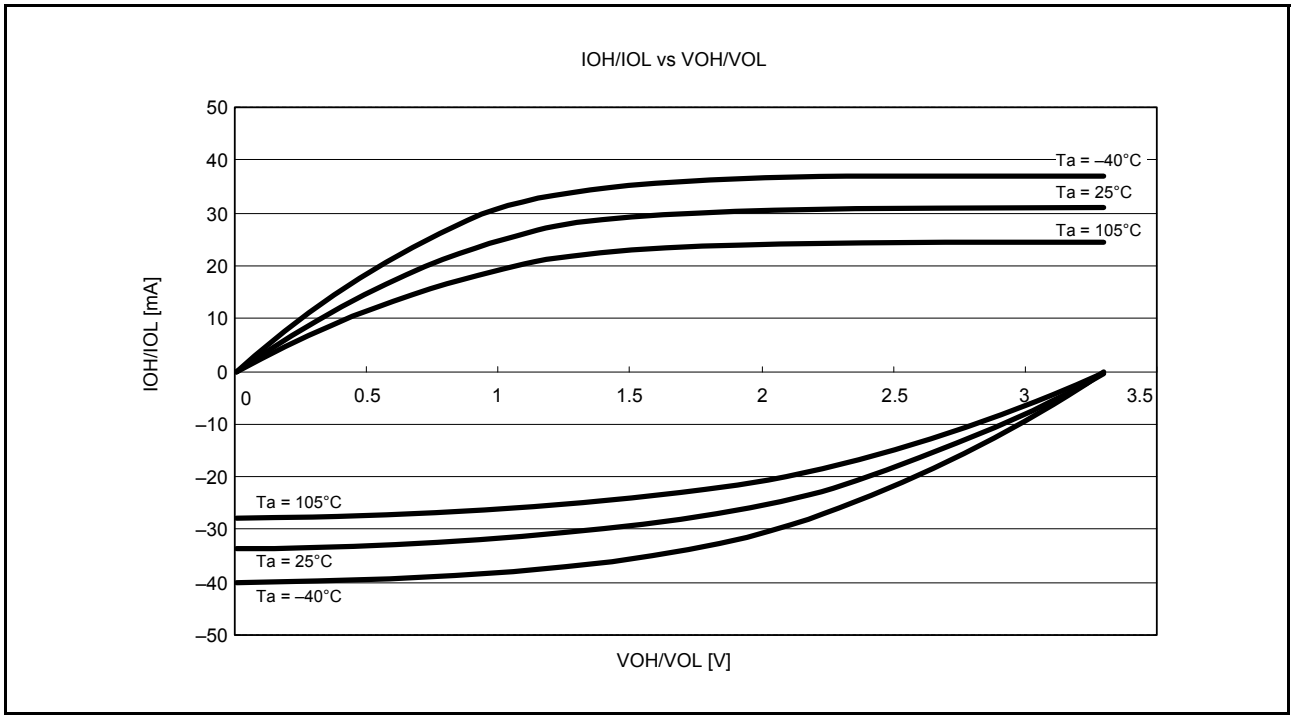


Figure 5.19 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.3 V when High-Drive Output is Selected (Reference Data)

5.4 Clock Timing

Table 5.26 Clock Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{EXcyc}	50	—	—	ns	Figure 5.25
EXTAL external clock input high pulse width		t_{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	20	—	—	ns	
EXTAL external clock rising time		t_{EXr}	—	—	5	ns	
EXTAL external clock falling time		t_{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	1	—	—	ms	
Main clock oscillator oscillation frequency*2		f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.26
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50		µs	
Main clock oscillation stabilization wait time (crystal)*2		$t_{MAINOSCWT}$	—	6	—	ms	
Main clock oscillation stabilization wait time (ceramic resonator)*2		$t_{MAINOSCWT}$	—	100		µs	
LOCO, IWDTCLK clock cycle time		t_{cyc}	7.27	8	8.89	µs	
LOCO, IWDTCLK clock oscillation frequency		f_{LOCO}	112.5	125	137.5	kHz	
LOCO, IWDTCLK clock oscillation stabilization wait time		t_{LOCOWT}	—	—	20	µs	Figure 5.27
HOCO clock oscillation frequency		f_{HOCO}	31.680	32	32.320	MHz	Ta = 0 to 50°C
			36.495	36.864	37.233		
			39.600	40	40.400		
			49.500	50	50.500		
			31.520	32	32.480		Ta = -40 to 105°C
			36.311	36.864	37.417		
			39.400	40	40.600		
			49.250	50	50.750		
HOCO clock oscillation stabilization time 1		t_{HOCO1}	—	—	300	µs	Figure 5.28
HOCO clock oscillation stabilization time 2		t_{HOCO2}	—	—	175	µs	Figure 5.29
HOCO clock oscillation stabilization wait time		t_{HOCOWT}	—	—	350	µs	Figure 5.29
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	350	µs	Figure 5.30
PLL input frequency		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency		f_{PLL}	50	—	100	MHz	
PLL clock oscillation stabilization time	PLL operation started after main clock oscillation has settled	t_{PLL1}	—	—	500	µs	Figure 5.31
PLL clock oscillation stabilization wait time		t_{PLLWT1}	1.5	—	—	ms	
PLL clock oscillation stabilization time*4	PLL operation started before main clock oscillation has settled	t_{PLL2}	—	3.5*3	—	ms	Figure 5.32
PLL clock oscillation stabilization wait time*4		t_{PLLWT2}	—	7	—	ms	
PLL clock power supply stabilization time		t_{PLLPW}	—	—	30	µs	Figure 5.33
Sub-clock oscillator oscillation frequency		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*5		t_{SUBOSC}	2	—	—	s	Figure 5.34
Sub-clock oscillation stabilization wait time*5		$t_{SUBOSCWT}$	4	—	—	s	

Note 1. The time interval from the time P36 and P37 are configured for input and the main clock oscillator stopping bit (MOSCCR.MOSTP) is set to 0 (operating) until the clock becomes available.

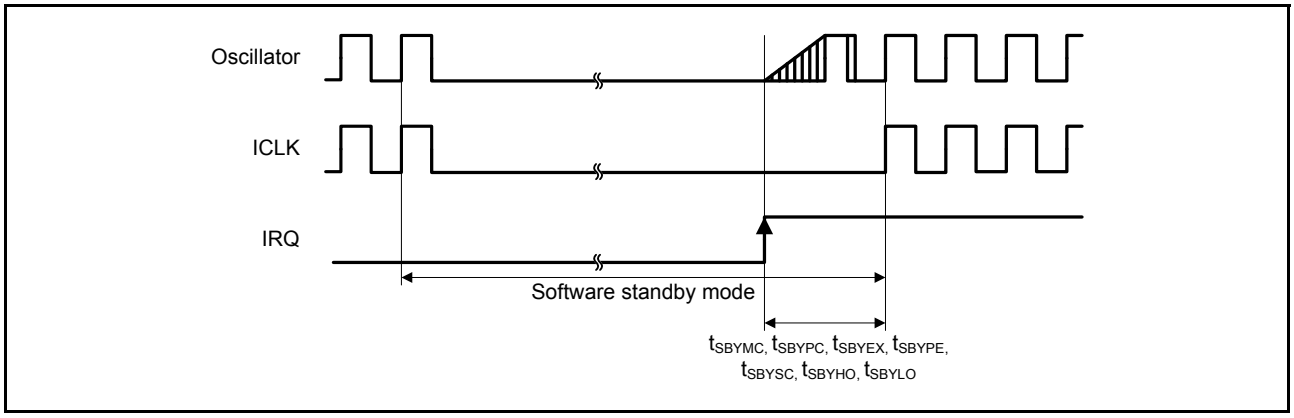


Figure 5.37 Software Standby Mode Cancellation Timing

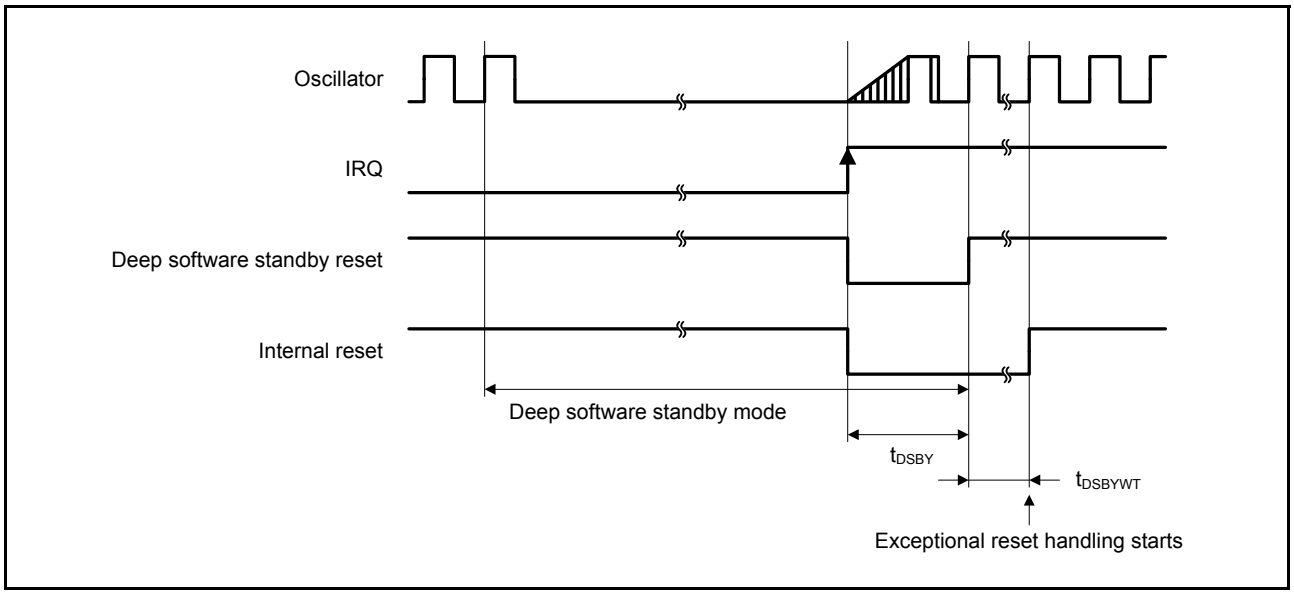


Figure 5.38 Deep Software Standby Mode Cancellation Timing

5.4.4 Timing of On-Chip Peripheral Modules

Table 5.30 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.41
MTU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.42
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.43
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.44
8-bit timer	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.45
		Both-edge setting		2.5	—		
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.48
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

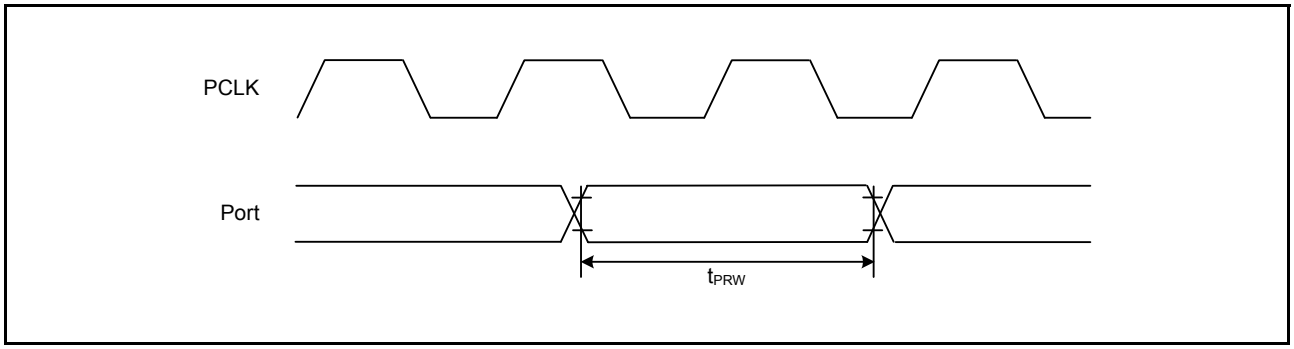


Figure 5.41 I/O Port Input Timing

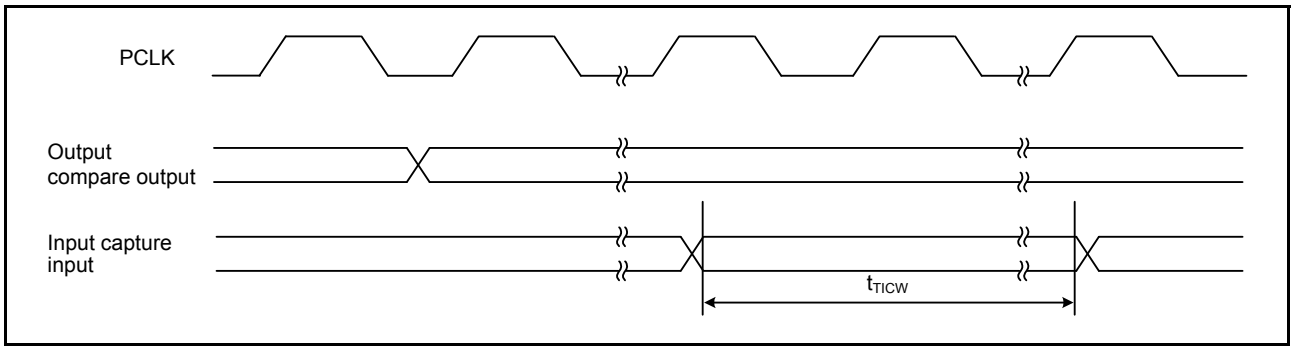


Figure 5.42 MTU Input/Output Timing

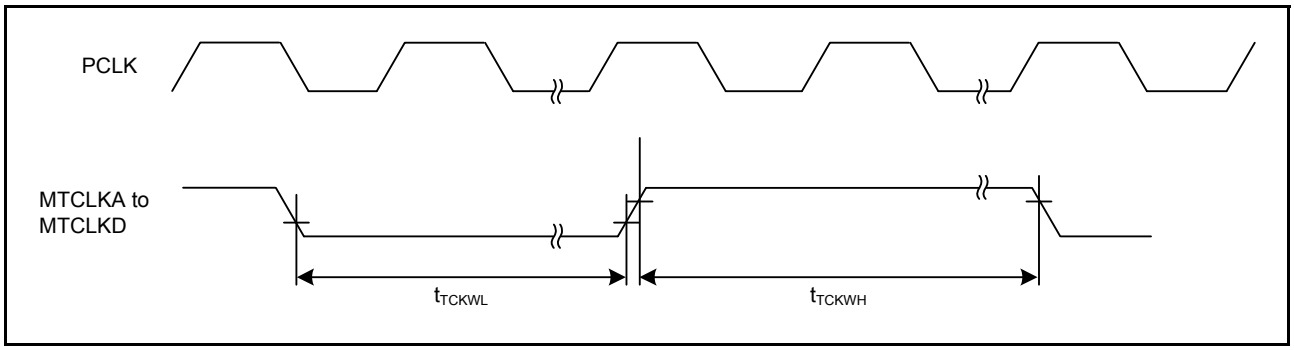


Figure 5.43 MTU Clock Input Timing

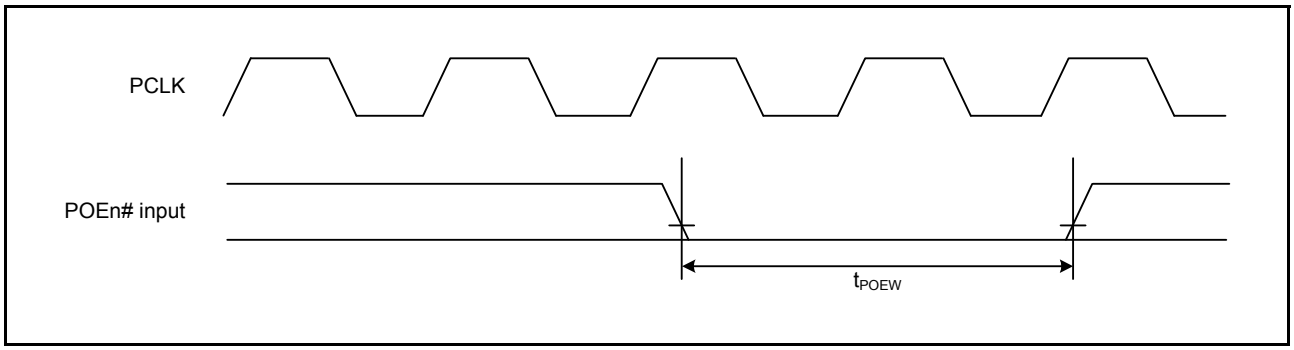


Figure 5.44 POE# Input Timing

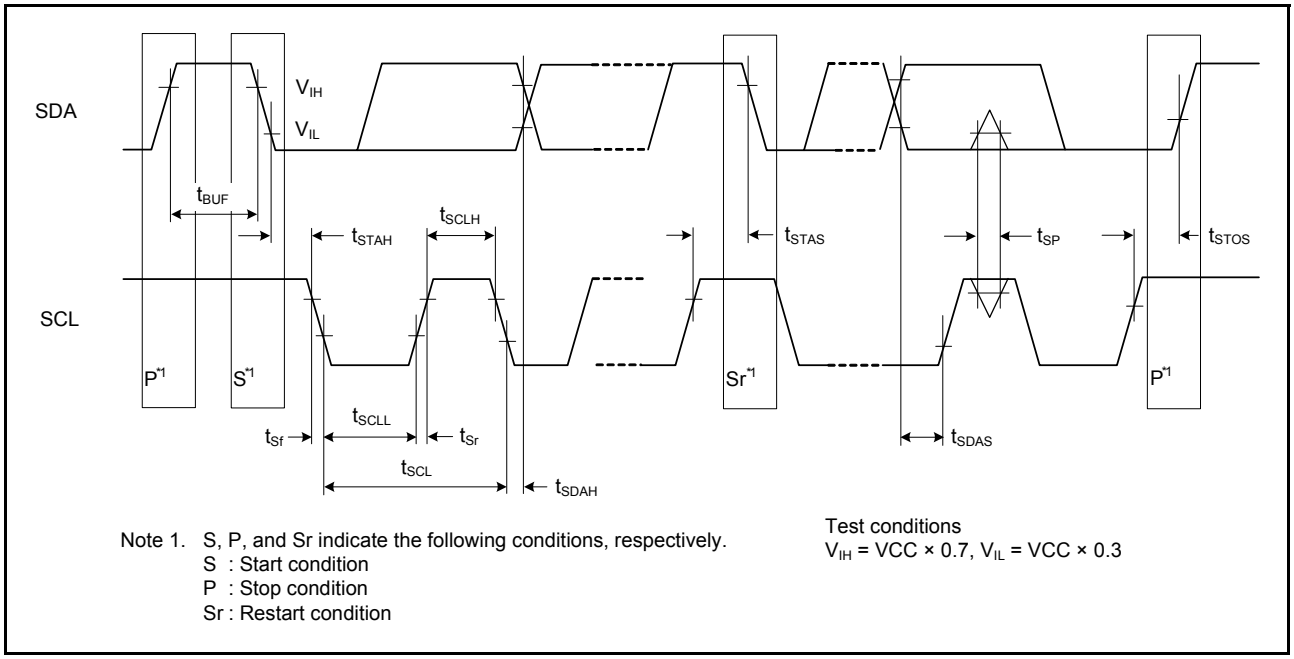


Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

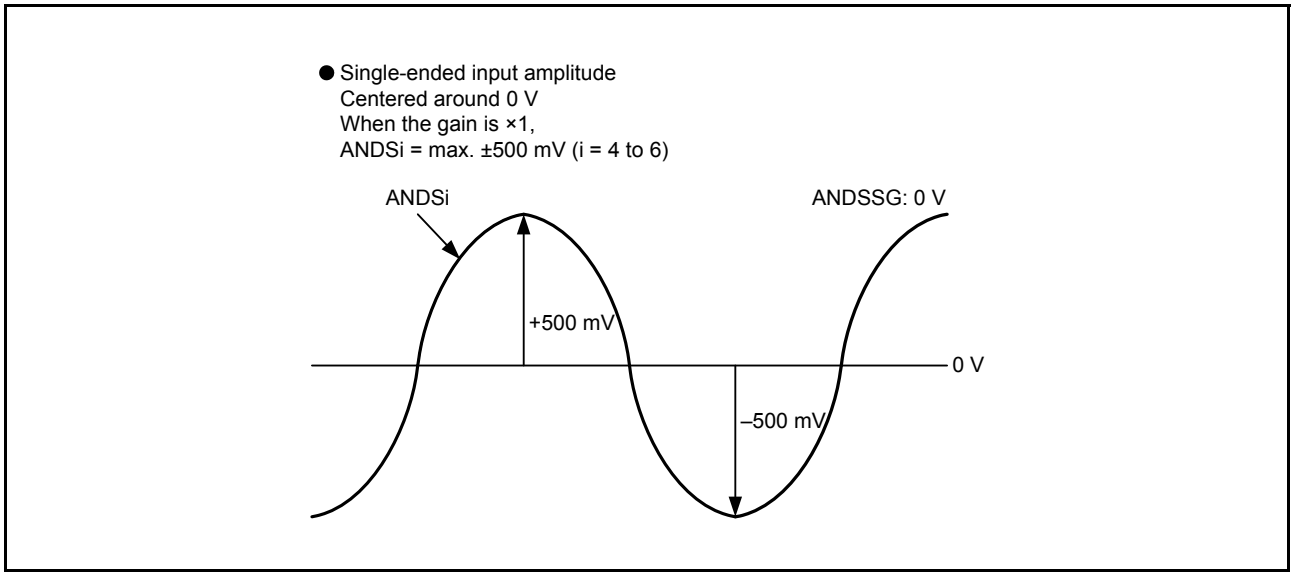


Figure 5.56 Single-ended Input Amplitude

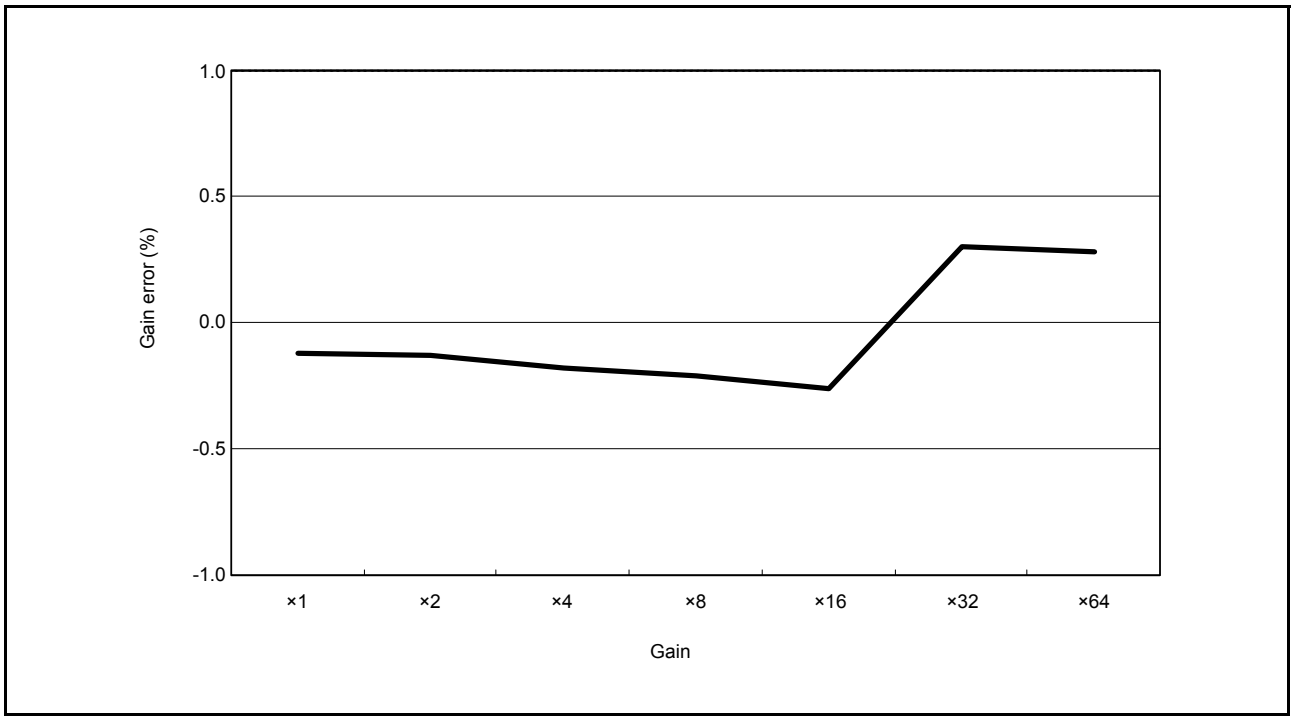


Figure 5.57 Gain Error (Reference Data)

5.9 Comparator Characteristics

Table 5.43 Comparator Characteristics

Conditions: VCC = AVCC0 = AVCCA =1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Comparator A	External reference voltage input range	LVREF	1.4	—	VCC	V	
	External comparison voltage (CMPA1, CMPA2) input range	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±50	±150	mV	
	Comparator output delay time*1	—	—	3	—	µs	At falling edge VI = LVREF – 110 mV
			—	2	—	µs	At falling edge VI < LVREF – 1 V
			—	3	—	µs	At rising edge VI = LVREF + 160 mV
			—	1.5	—	µs	At rising edge VI > LVREF + 1 V
	Comparator operating current	ICMPA	—	0.5	—	µA	VCC = 3.3 V
Comparator B	Input reference voltage for CVREFB0, CVREFB1	VREF	0	—	VCC – 1.4	V	
	Input voltage for CMPB0, CMPB1	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±10	±100	mV	
	Comparator output delay time	t_d	—	—	1	µs	VI = VREF + 100 mV
	Comparator operating current	ICMPB	—	75	150	µA	VCC = 3.3 V For total two channels

Note 1. When the digital filter is disabled.

Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (3) : medium-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.9	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.1	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.66	8.5	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.6	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.8	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.78	10.3	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.6	—	18.6	48.7	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.7	94.5 (1000 times ≥ N_{PEC} > 100 times), 102.9 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.604	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.604	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.604	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.604	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.

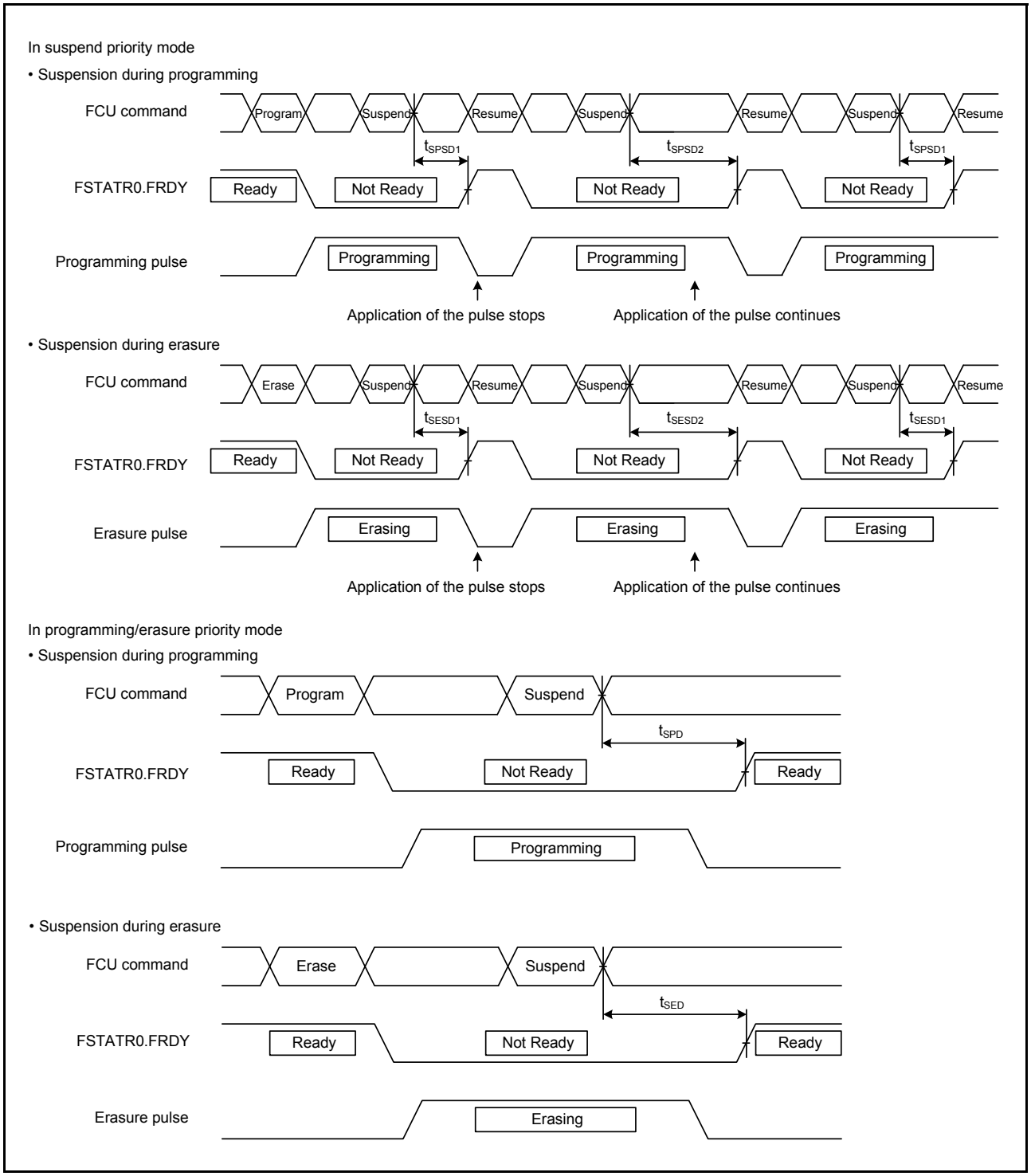
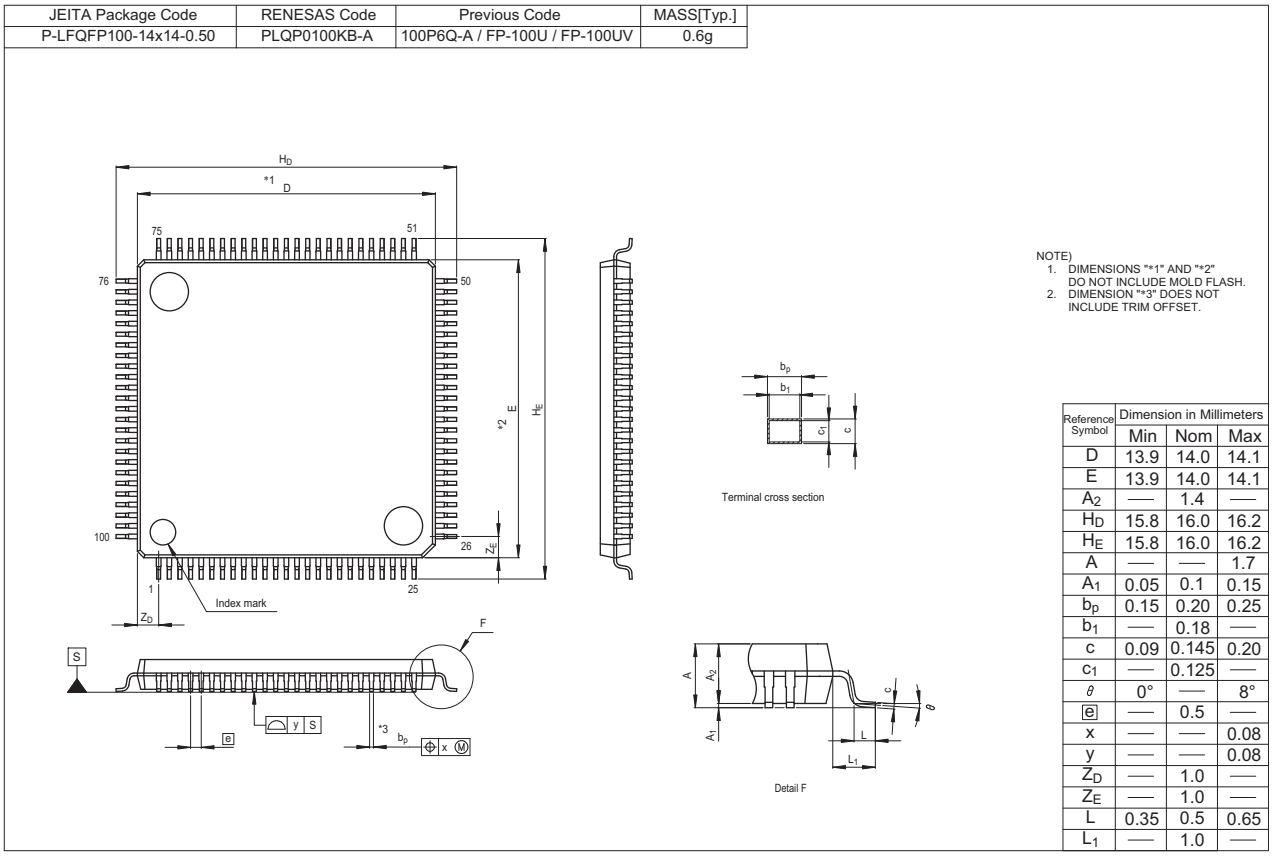


Figure 5.70 Flash Memory Program/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LQFP (PLQP0100KB-A)