Renesas Electronics America Inc - R5F521A7BDFM#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 3x24b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a7bdfm-30

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Package		100-pin LQFP (PLQP0100KB-A) 14 x 14 mm, 0.5-mm pitch 80-pin LQFP (PLQP0080KB-A) 12 x 12mm, 0.5-mm pitch 64-pin LQFP (PLQP0064KB-A) 10 x 10mm, 0.5-mm pitch 100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch
On-chip debugging system		E1 emulator (FINE interfaces)

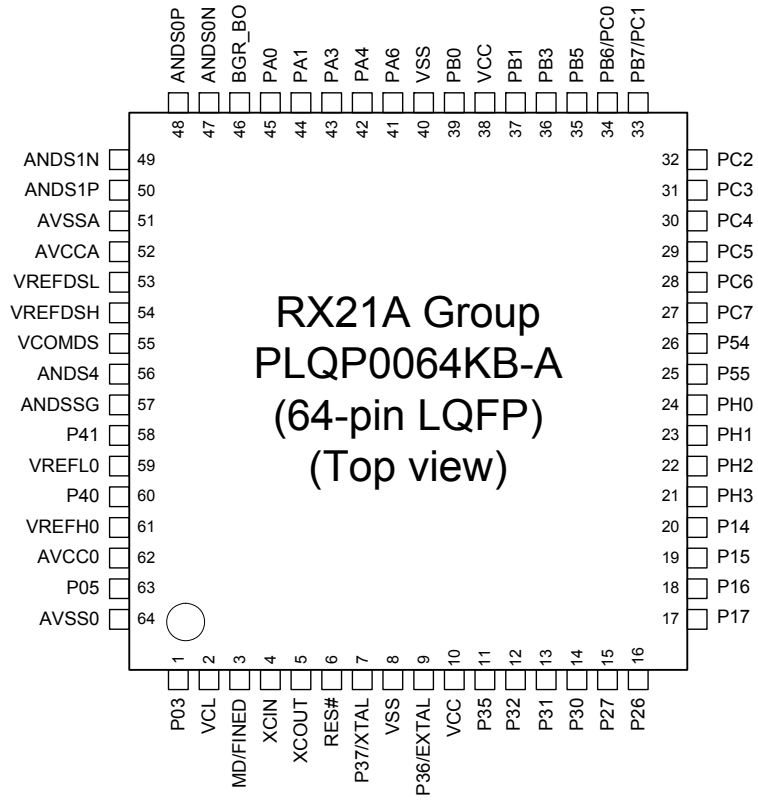
Note 1. Contact a Renesas Electronics sales office for more information.
Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 3. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
Section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
Section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
Section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
Section 37.3, Using the Temperature Sensor
Section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX21A Group		
		100 Pins	80 Pins	64 Pins
Interrupt	External interrupts	NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7
DMA	DMA controller	4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Supported		
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)		
	Port output enable 2	POE0# to POE3#, POE8#		
	8-bit timer	2 channels × 2 units		
	Compare match timer	2 channels × 2 units		
	Realtime clock	Supported		
	Watchdog timer	Supported		
	Independent watchdog timer	Supported		
Communication function	Serial communications interface	5 channels (SCI1, 5, 6, 8, 9) (including one channel for IrDA)		
	I^2C bus interface	2 channels		1 channel
	Serial peripheral interface	2 channels		
24-bit ΔΣ A/D converter		7 channels	4 channels	3 channels
10-bit A/D converter		7 channels (AN0 to AN6)		4 channels (AN0, AN1, AN4, AN5)
Temperature sensor		Supported		
D/A converter		2 channels		—
CRC calculator		Supported		
Data encryption unit		Supported		
Event link controller		Supported		
Comparator A		2 channels		1 channel
Comparator B		2 channels		
Package		100-pin LQFP 100-pin TFLGA	80-pin LQFP	64-pin LQFP

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

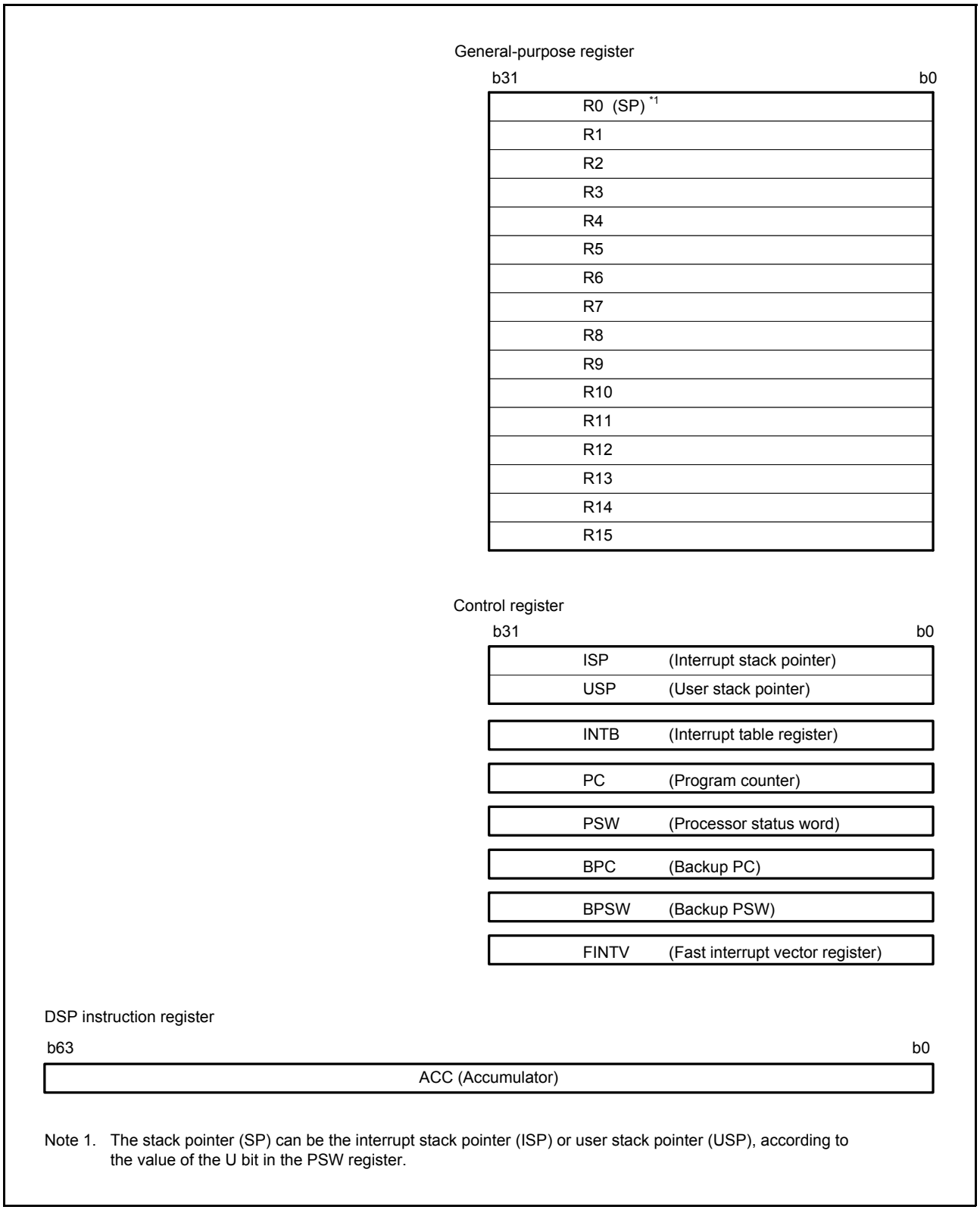
Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
1	VREFH				
2		P03			AN4/DA0
3	VREFL				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL				
6		PJ1	MTIOC3A		
7	MD				FINED
8	XCIN				
9	XCOUT				
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		P35			NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
20		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/ MISOB	IRQ0-DS/RTCIC0
21		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB	
23		P25	MTIOC4C/MTCLKB		ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1		
25		P23	MTIOC3D/MTCLKD		
26		P22	MTIOC3B/MTCLKC/TMO0		
27		P21	MTIOC1B/TMCI0	SCL1	
28		P20	MTIOC1A/TMRI0	SDA1	
29		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
30		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13	MTIOC0B/TMO3	SDA0	IRQ3
34		P12	TMCI1	SCL0	IRQ2
35		PH3	TMCI0		
36		PH2	TMRI0		IRQ1
37		PH1	TMO0		IRQ0
38		PH0			CACREF
39		P55	MTIOC4D/TMO3		
40		P54	MTIOC4B/TMCI1		
41		P53			

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
A1		P05			AN5/DA1
A2	VREFH				
A3		P07			AN6/ADTRG0#
A4	VREFL0				
A5		P43			AN3
A6	VCOMDS				
A7	AVSSA				
A8					ANDS2N
A9					ANDS1P
A10					ANDS1N
B1		P03			AN4/DA0
B2	AVSS0				
B3	AVCC0				
B4		P40			AN0
B5	ANDSSG				
B6	VREFDSH				
B7	AVCCA				
B8					ANDS3N
B9					ANDS2P
B10					ANDS0P
C1	VCL				
C2	VREFL				
C3		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
C4	VREFH0				
C5		P42			AN2
C6					ANDS4
C7	VREFDSL				
C8					ANDS3P
C9	BGR_BO				
C10					ANDS0N
D1	XCIN				
D2	XCOUT				
D3	MD				FINED
D4		PJ1	MTIOC3A		
D5					ANDS6
D6					ANDS5
D7		PE6		MOSIB	IRQ6
D8		PE7		MISOB	IRQ7-DS
D9		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
D10		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
E1	XTAL	P37			
E2	VSS				
E3	RES#				
E4		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
E5		P41			AN1

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (2 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16		2 ICLK
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8		2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8		2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32		2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16		2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8		2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8		2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32		2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32		2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16		2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8		2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8		2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2200h	DMAC	DMA module activation register	DMAST	8	8		2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8		2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32		2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8		2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16		2 ICLK
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32		1 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK
0008 8900h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8902h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLKB	2 ICLK
0008 8908h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLKB	2 ICLK
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLKB	2 ICLK
0008 9800h	AD	A/D control register	ADCSR	16	16	2, 3 PCLKB	2 ICLK
0008 9804h	AD	A/D channel select register A	ADANSA	16	16	2, 3 PCLKB	2 ICLK
0008 9808h	AD	A/D-converted value addition mode select register	ADADS	16	16	2, 3 PCLKB	2 ICLK
0008 980Ch	AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK
0008 980Eh	AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK
0008 9810h	AD	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLKB	2 ICLK
0008 9812h	AD	A/D-converted extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK
0008 981Ah	AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK
0008 981Ch	AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK
0008 981Eh	AD	A/D self-diagnosis data register	ADRD	16	16	2, 3 PCLKB	2 ICLK
0008 9820h	AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK
0008 9822h	AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK
0008 9824h	AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK
0008 9826h	AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK
0008 9828h	AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK
0008 982Ah	AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK
0008 982Ch	AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK
0008 9860h	AD	A/D sampling state register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK
0008 9870h	AD	A/D sampling state register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK
0008 9871h	AD	A/D sampling state register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK
0008 9873h	AD	A/D sampling state register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK
0008 9874h	AD	A/D sampling state register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK
0008 9875h	AD	A/D sampling state register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK
0008 9876h	AD	A/D sampling state register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK
0008 9877h	AD	A/D sampling state register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK
0008 9878h	AD	A/D sampling state register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.11 to Figure 5.15 show the characteristics when normal output is selected by the drive capacity control register.

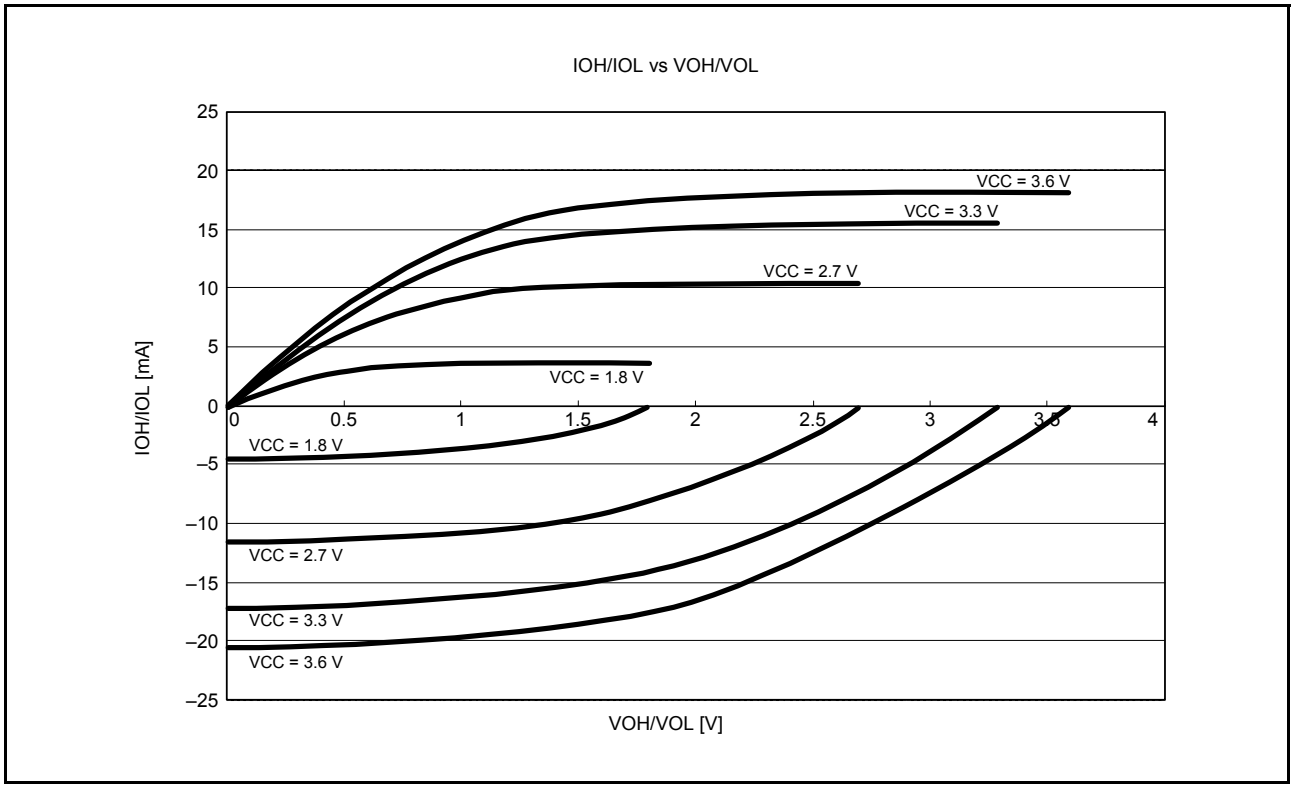


Figure 5.11 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

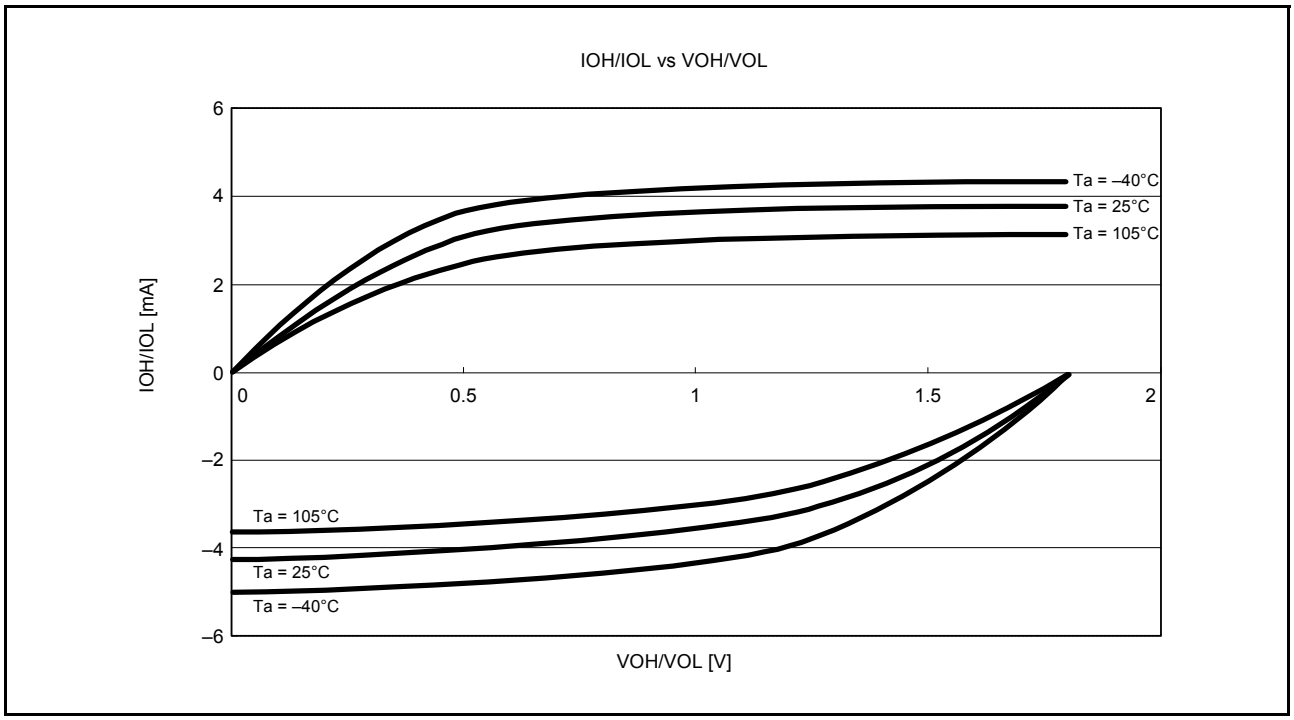


Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when Normal Output is Selected (Reference Data)

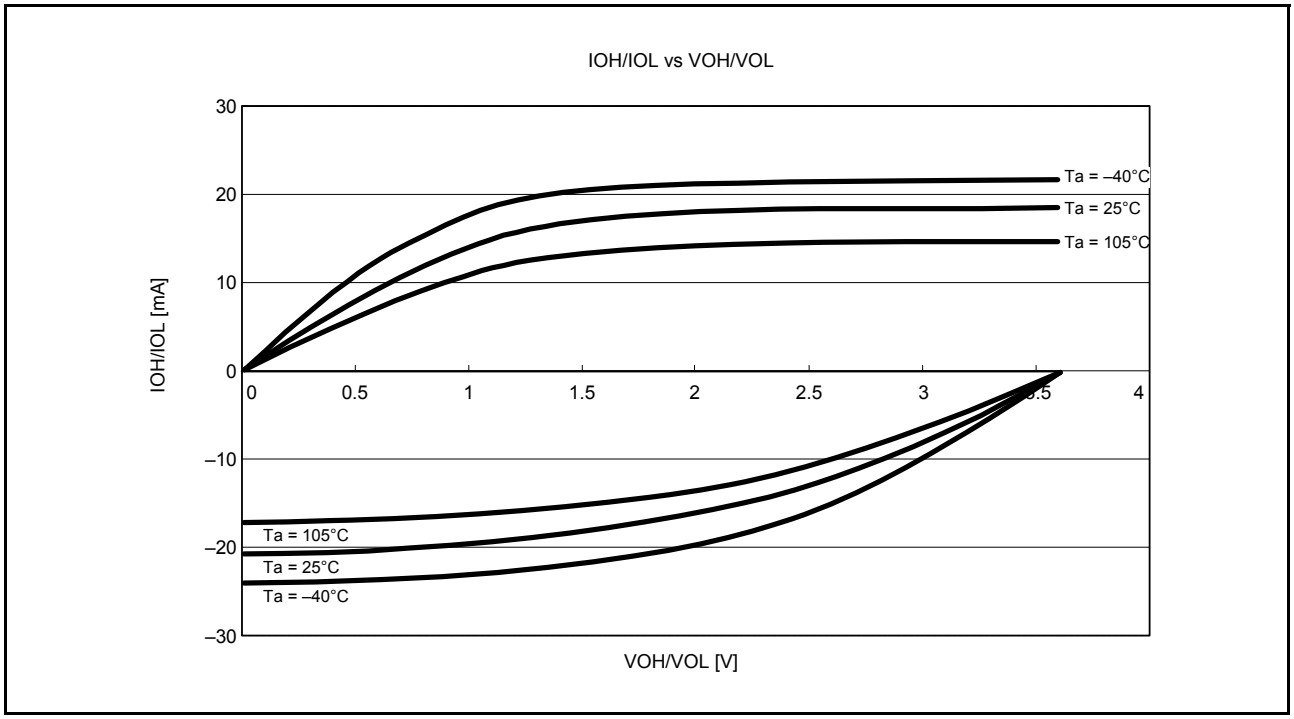


Figure 5.15 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.6 V when Normal Output is Selected (Reference Data)

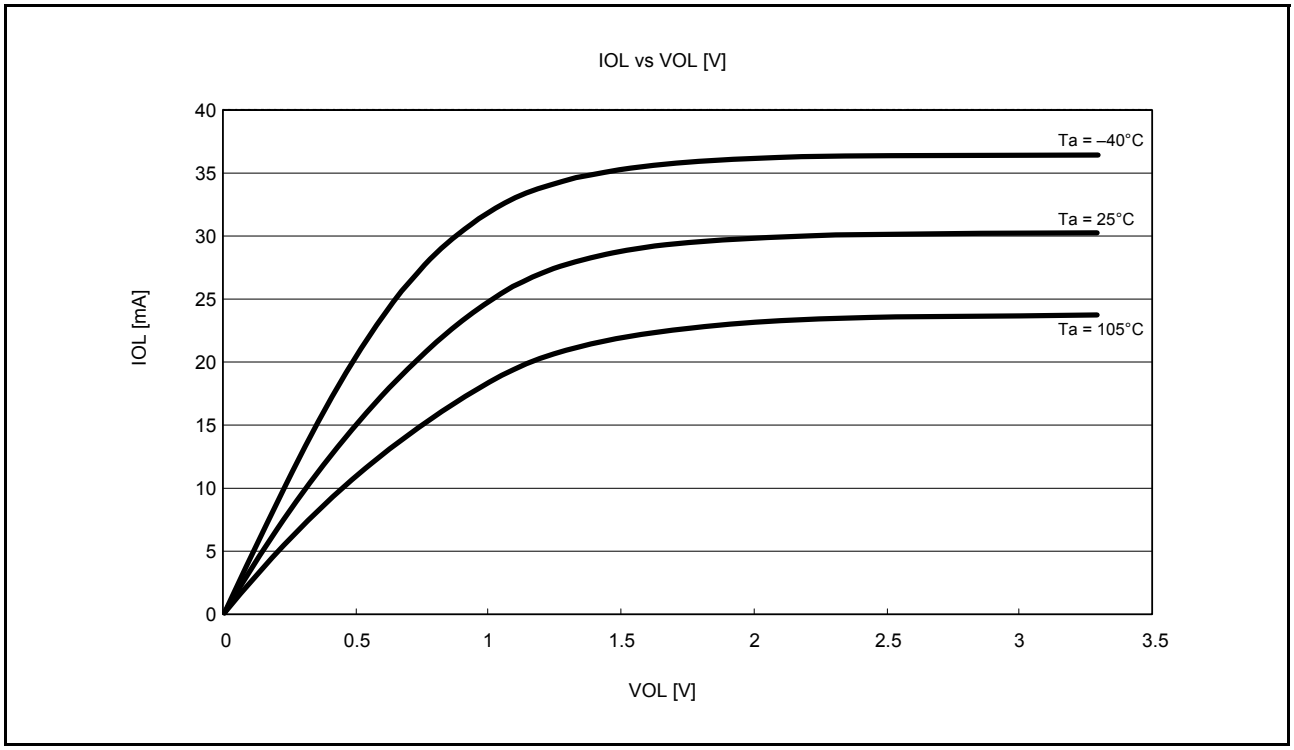


Figure 5.23 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

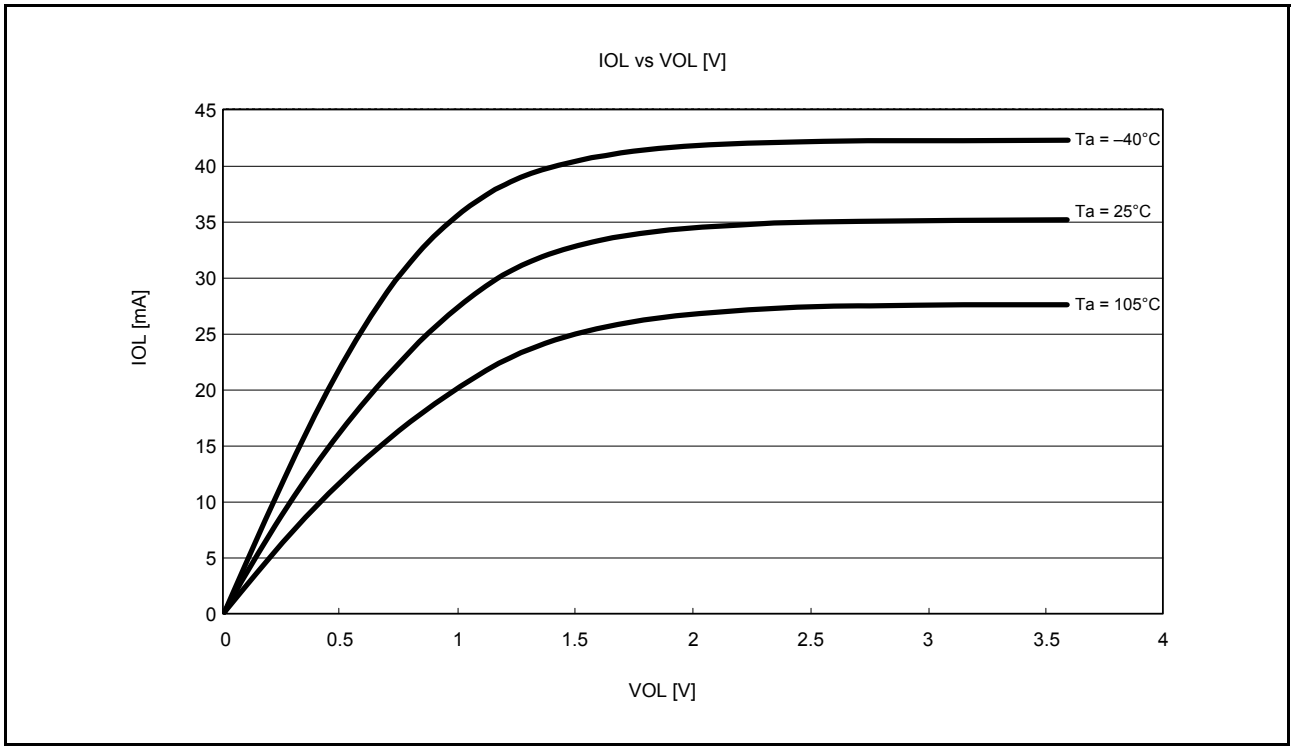


Figure 5.24 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.6 V (Reference Data)

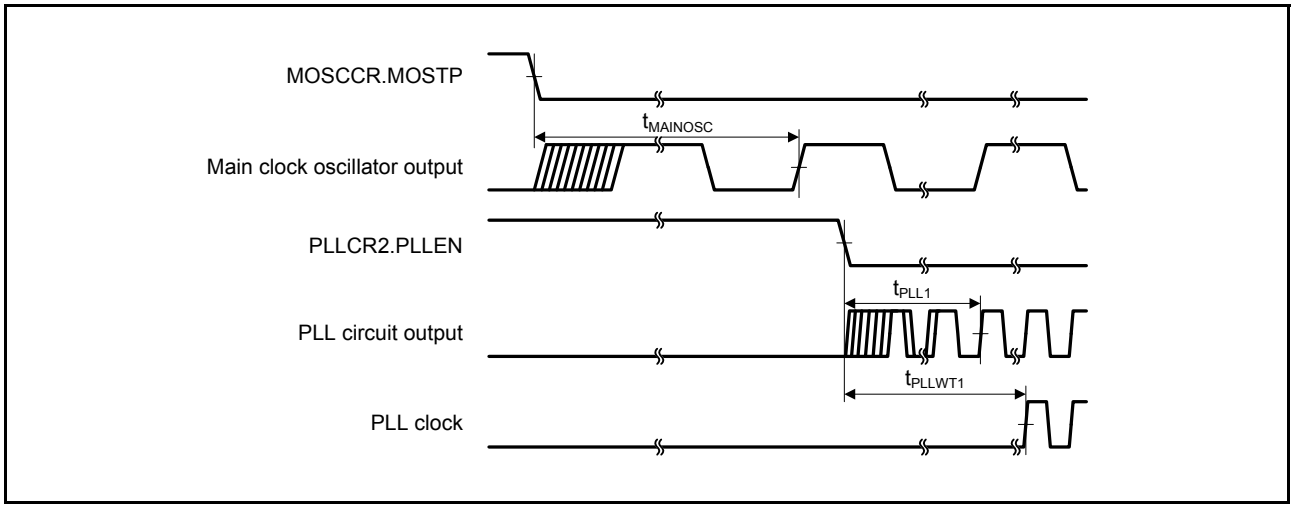


Figure 5.31 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

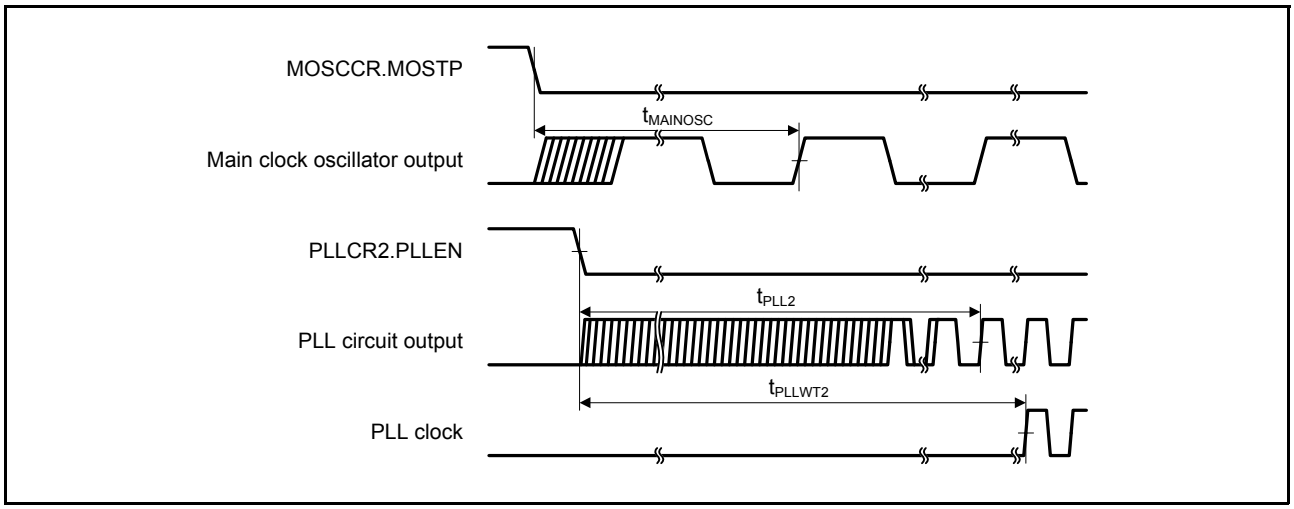


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

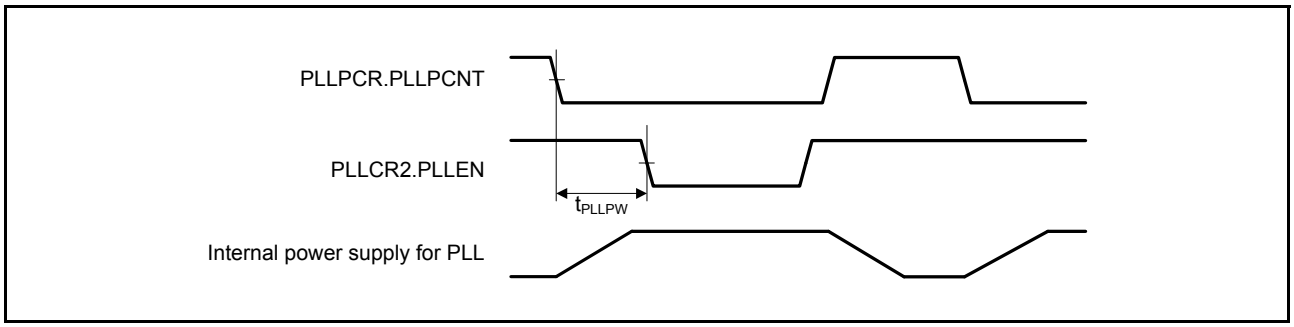


Figure 5.33 PLL Power Control Timing

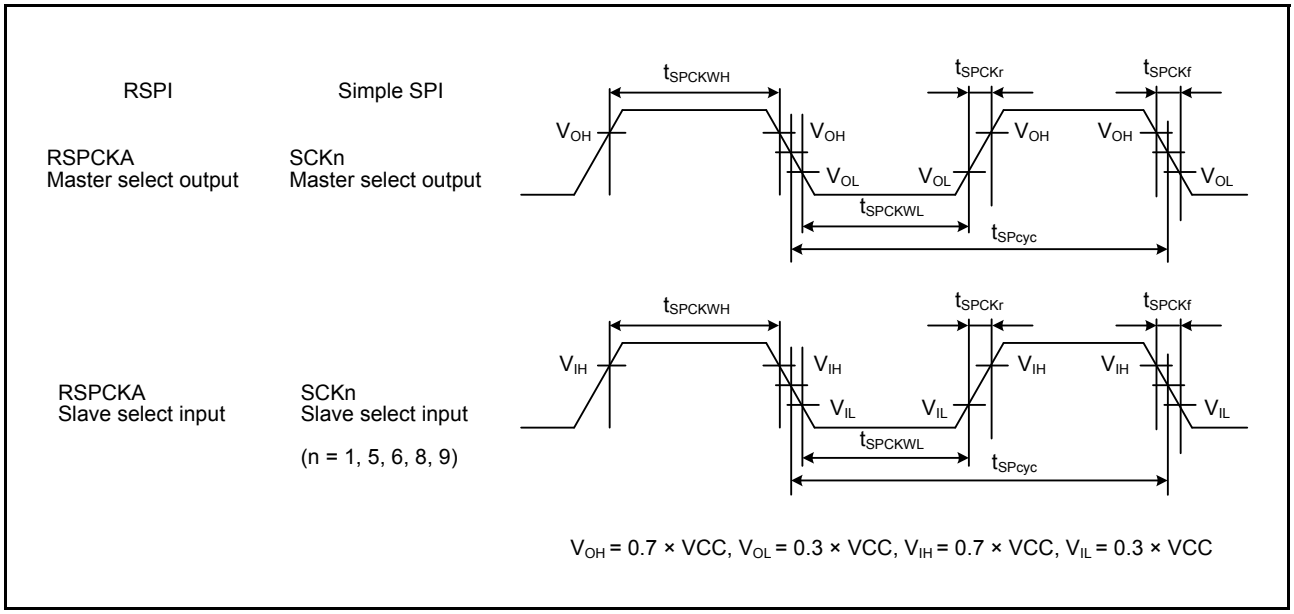


Figure 5.49 RSPI Clock Timing and Simple SPI Clock Timing

5.6 A/D Conversion Characteristics

Table 5.37 A/D Conversion Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0*3,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, fT_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	25	MHz	
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 25 MHz)	Permissible signal source impedance (Max.) = 1.5 kΩ	2.0 (1.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.0	±2.0	LSB	
Full-scale error		—	±1.0	±2.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy*4		—	±1.0	±3.0	LSB	
DNL differential nonlinearity error*4		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.0	±2.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pin LQFP may inferior to the values on this table; ±1.5 LSB in Absolute accuracy, ±0.5 LSB in DNL differential nonlinearity error.

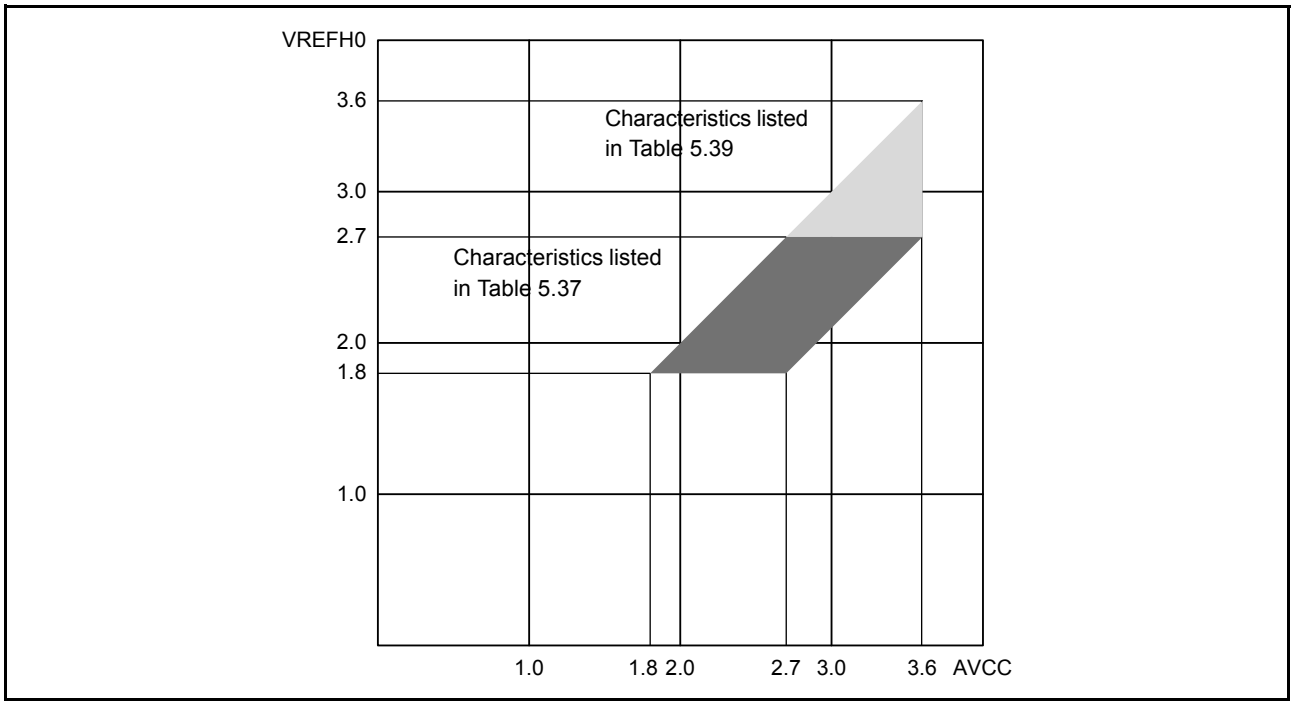


Figure 5.61 AVCC to VREFH0 Voltage Range

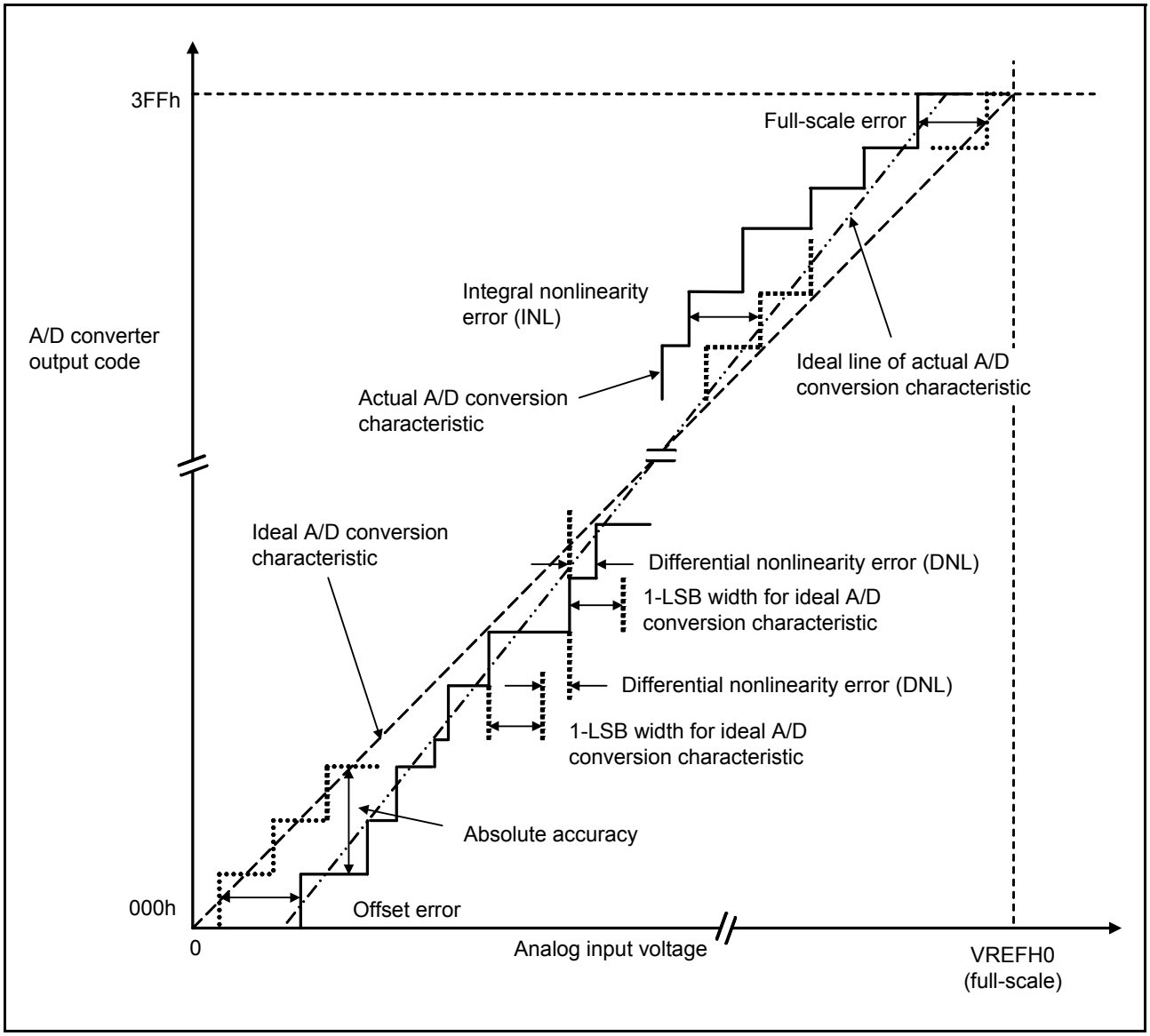


Figure 5.62 Illustration of A/D Converter Characteristic Terms

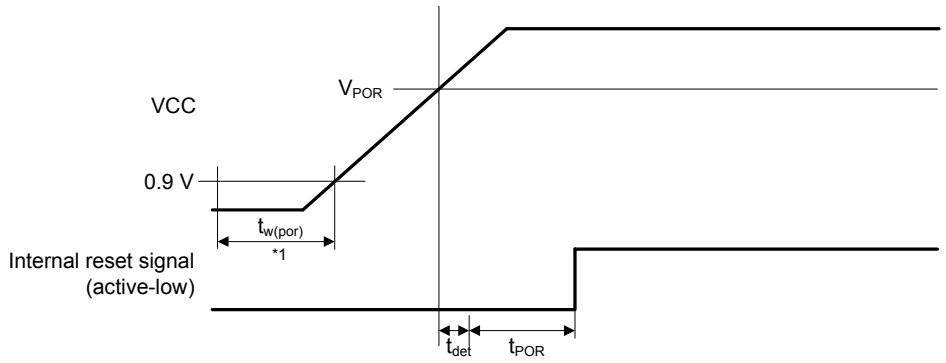
Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 10-bit resolution is used and if reference voltage VREFH0 = 2.56 V, then 1-LSB width becomes 2.5 mV, and 0 mV, 2.5 mV, 5.0 mV, ... are used as analog input voltages.

If analog input voltage is 20 mV, absolute accuracy = ±4 LSB means that the actual A/D conversion result is in the range of 004h to 00Ch though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.65 Power-on Reset Timing

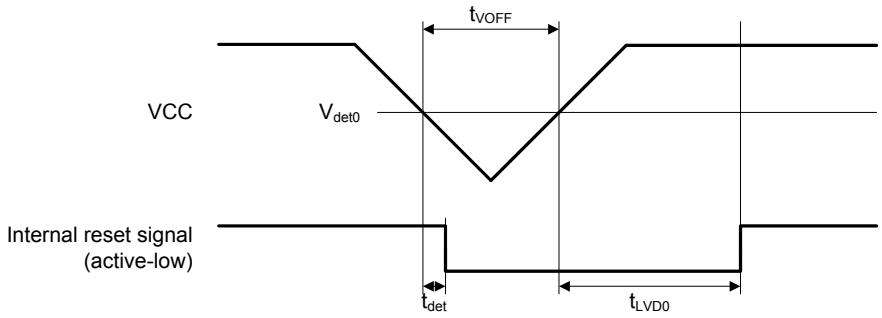


Figure 5.66 Voltage Detection Circuit Timing (V_{det0})

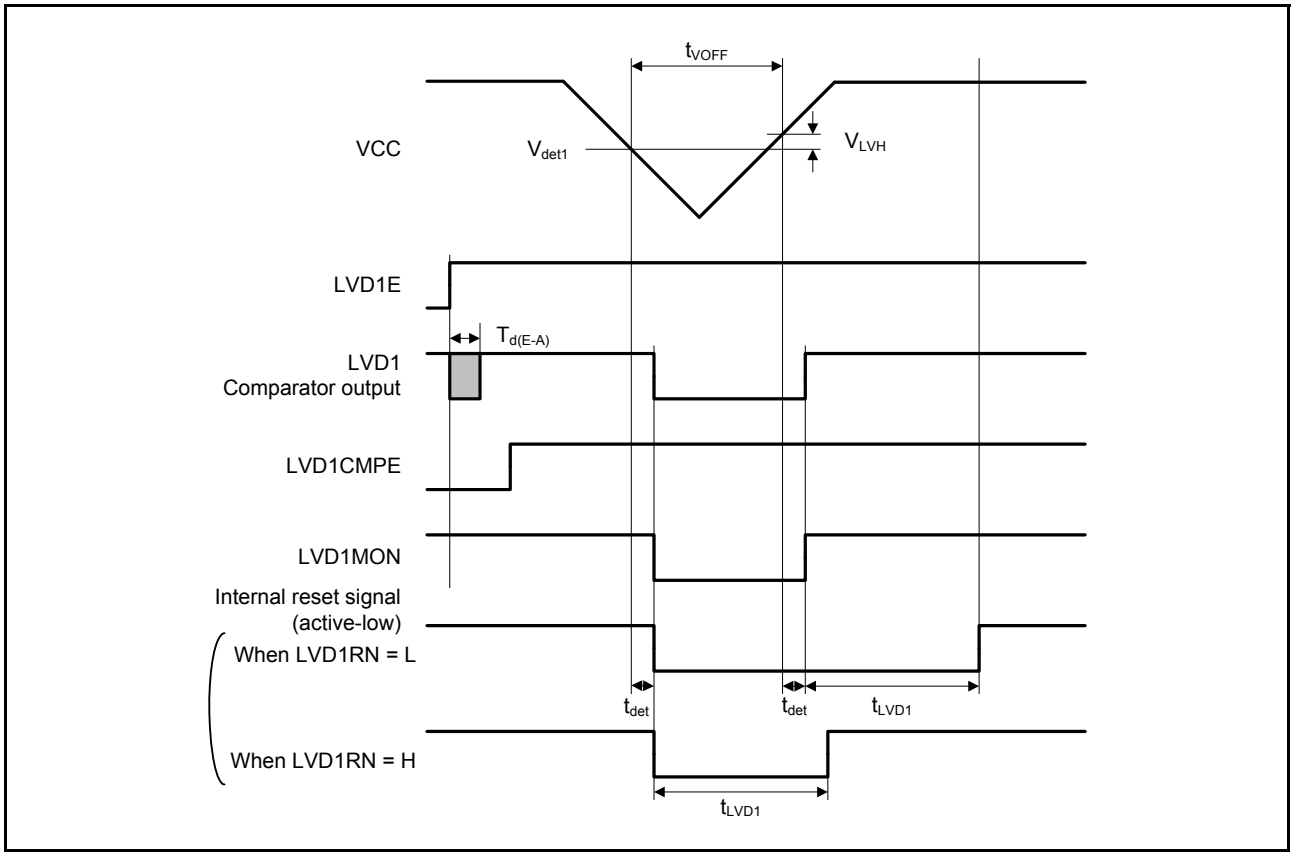


Figure 5.67 Voltage Detection Circuit Timing (V_{det1})

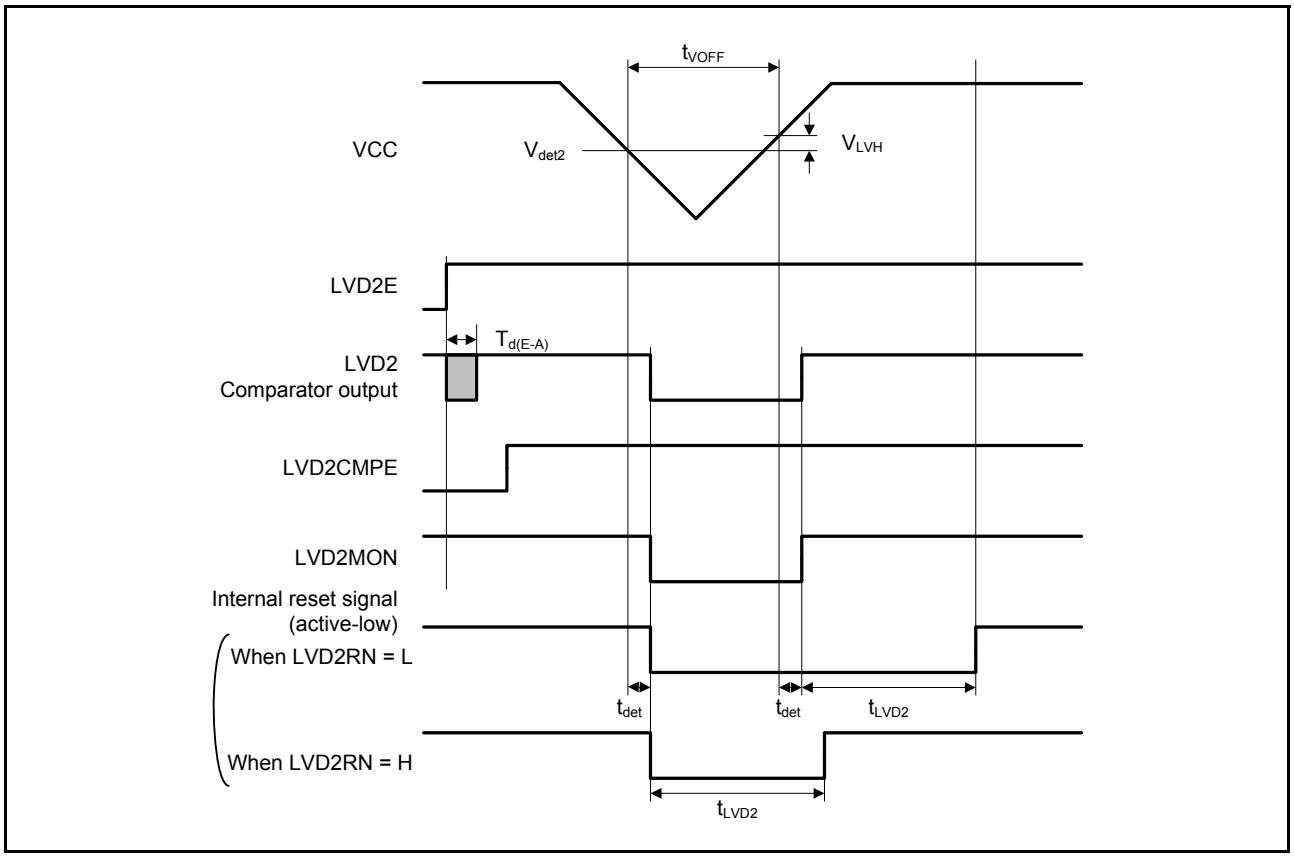


Figure 5.68 Voltage Detection Circuit Timing (V_{det2})

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	2014.08.28	Features		
		1	LGA package, added	TN-RX*-A072A/E
		1. Overview		
		5	Table 1.1 Outline of Specifications: Package added	TN-RX*-A072A/E
		5	Table 1.1 Outline of Specifications: Note 2 added	TN-RX*-A073A/E
		5	Table 1.1 Outline of Specifications: Note 3 added	
		5	Table 1.2 Comparison of Functions for Different Packages, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note 1 added	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note, Note 2 added	
		7	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed	TN-RX*-A072A/E
		9	Table 1.4 Pin Functions: Realtime clock changed	
		15	Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View), added	TN-RX*-A072A/E
		23 to 25	Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA), added	TN-RX*-A072A/E
		3. Address Space		
		29	Figure 3.1 Memory Map, changed	
		4. I/O Registers		
		54 to 55	Table 4.1 List of I/O Registers (Address Order): FEFF FAC0h to FEFF FBD3h added	
		5. Electrical Characteristics		
		57	Table 5.3 DC Characteristics (2)	TN-RX*-A074A/E
		58	Table 5.4 DC Characteristics (3), changed	TN-RX*-A074A/E
		59	Table 5.6 DC Characteristics (5), changed	TN-RX*-A074A/E
		60	Table 5.7 DC Characteristics (6), changed	TN-RX*-A074A/E
		68	Table 5.9 DC Characteristics (8), added	TN-RX*-A074A/E
		68	Table 5.10 DC Characteristics (9), changed	
		68	Table 5.11 DC Characteristics (10), changed	
		69	Table 5.14 DC Characteristics (13), changed	TN-RX*-A074A/E
		69	Table 5.15 Permissible Output Currents (1), changed Table 5.16 Permissible Output Currents (2), added	TN-RX*-A074A/E
		70	Table 5.18 Output Values of Voltage (2), changed	TN-RX*-A074A/E
		82	Table 5.26 Clock Timing, changed	TN-RX*-A097A/E
		83	Table 5.26 Clock Timing: Note 5 changed	TN-RX*-A105A/E
		83	Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		87	Figure 5.35 Reset Input Timing at Power-On, changed	TN-RX*-A074A/E
		94	Table 5.33 Timing of On-Chip Peripheral Modules (4), changed	TN-RX*-A074A/E
		103	Table 5.36 ΔΣ A/D Conversion Characteristics, changed	TN-RX*-A105A/E
		104	Figure 5.55 Differential Input Amplitude, changed	
		108	Table 5.37 A/D Conversion Characteristics (1), changed	TN-RX*-A074A/E
		108	Figure 5.61 AVCC to VREFH0 Voltage Range, added	TN-RX*-A074A/E
		109	Table 5.39 A/D Conversion Characteristics (2), changed	TN-RX*-A074A/E
		111	Differential nonlinearity error (DNL), description changed	TN-RX*-A073A/E
		115	Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1): Note1, Note2 changed	TN-RX*-A074A/E
		Appendix 1. Package Dimensions		
		128	Figure D. 100-Pin TFLGA (PTLG0100JA-A), added	TN-RX*-A072A/E