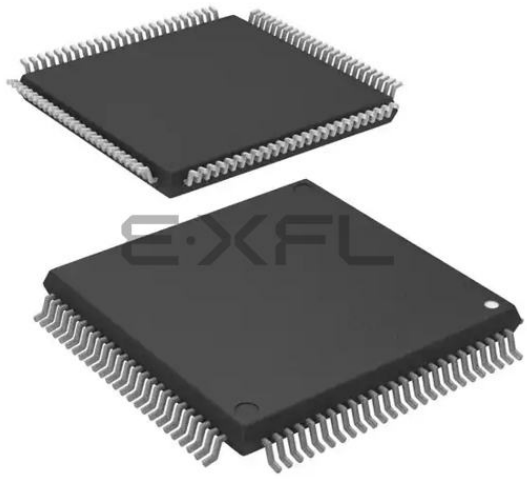


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a7bdfp-30

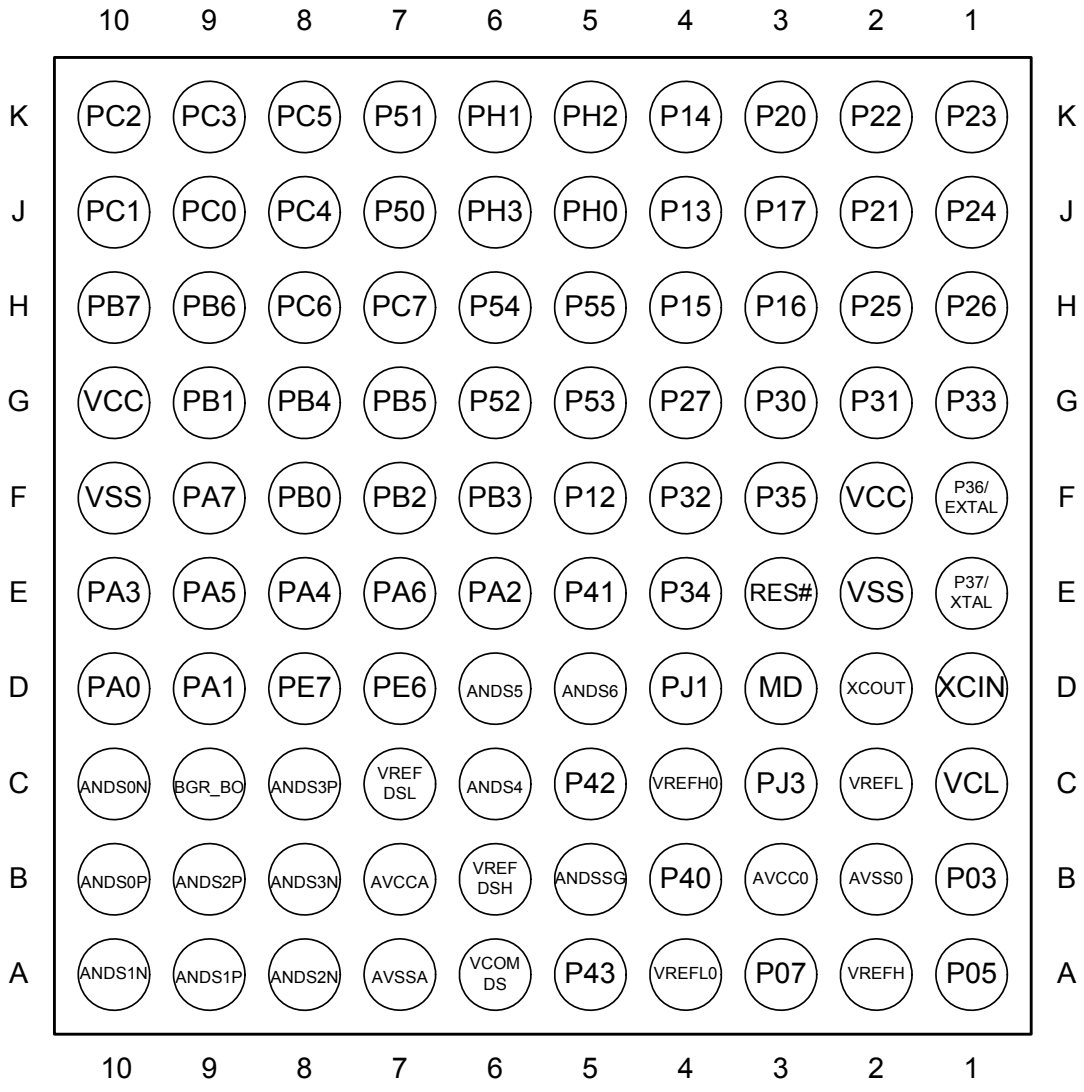
Table 1.1 Outline of Specifications (3 / 4)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIc)	• 5 channels (channel 1, 5, 6, 8, 9) (including one channel for IrDA) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5 and SCI6) • Simple IIC • Simple SPI
	IrDA interface (IRDA)	• 1 channel (SCI5 is used) • Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0
	I^2C bus interface (RIIC)	• 2 channels • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 2 channels • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
24-bit ΔΣ A/D converter (DSAD)		• 7 channels: 4-channel differential input for current; 3-channel single-ended input for voltage • x 1 to x 64 PGA for differential input side for current and x 1 to x 4 PGA for single-ended input side for voltage • Minimum conversion time: 81.92 µs (A/D conversion clock: 25 MHz)
10-bit A/D converter (AD)		• 10 bits (7 channels x 1 unit) • 10-bit resolution • Conversion time: 2.0 µs per channel (A/D conversion clock: 25 MHz) • Operating modes Scan mode (single scan mode and continuous scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • A/D conversion start conditions Conversion can be started by software, a conversion start trigger from a timer (MTU), an external trigger signal, a temperature sensor or ELC.
Temperature sensor (TEMPSa)		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Three levels according to the voltage range
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data encryption unit (DEU)*1		• Encryption and decryption of AES • 128-, 192-, or 256-bit key length • ECB or CBC mode
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B (CMPB)		• 2 channels • Comparison of reference voltage and analog input voltage
Data operating circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/ Operating frequency		VCC = 1.8 to 3.6 V: 25 MHz, VCC = 2.7 to 3.6 V: 50 MHz
Supply current		8.6mA@50MHz (typ)
Operating temperature		D version: –40 to +85°C, G version: –40 to +105°C*2, *3

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

RX21A Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
79					ANDS2P
80					ANDS3N
81					ANDS3P
82	AVSSA				
83	AVCCA				
84	VREFDSL				
85	VREFDSH				
86	VCOMDS				
87					ANDS4
88					ANDS5
89					ANDS6
90	ANDSSG				
91		P43			AN3
92		P42			AN2
93		P41			AN1
94	VREFL0				
95		P40			AN0
96	VREFH0				
97	AVCC0				
98		P07			AN6/ADTRG0#
99	AVSS0				
100		P05			AN5/DA1

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 4.1 List of I/O Registers (Address Order) (2 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16		2 ICLK
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8		2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8		2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32		2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16		2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8		2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8		2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32		2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32		2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16		2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8		2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8		2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2200h	DMAC	DMA module activation register	DMAST	8	8		2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8		2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32		2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8		2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16		2 ICLK
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32		1 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8		2 ICLK
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8		2 ICLK
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8		2 ICLK
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8		2 ICLK
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8		2 ICLK
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8		2 ICLK
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8		2 ICLK
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8		2 ICLK
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8		2 ICLK
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8		2 ICLK
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8		2 ICLK
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8		2 ICLK
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8		2 ICLK
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8		2 ICLK
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8		2 ICLK
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8		2 ICLK
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8		2 ICLK
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8		2 ICLK
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8		2 ICLK
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8		2 ICLK
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8		2 ICLK
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8		2 ICLK
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8		2 ICLK
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8		2 ICLK
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8		2 ICLK
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8		2 ICLK
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8		2 ICLK
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8		2 ICLK
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8		2 ICLK
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8		2 ICLK
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8		2 ICLK
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8		2 ICLK
0008 73D1h	ICU	Interrupt source priority register 209	IPR209	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D3h	ICU	Interrupt source priority register 211	IPR211	8	8		2 ICLK
0008 73D4h	ICU	Interrupt source priority register 212	IPR212	8	8		2 ICLK
0008 73D5h	ICU	Interrupt source priority register 213	IPR213	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C169h	MPC	P51 pin function control register	P51PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ah	MPC	P52 pin function control register	P52PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C190h	MPC	PA0 pin function control register	PA0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C191h	MPC	PA1 pin function control register	PA1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C192h	MPC	PA2 pin function control register	PA2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C193h	MPC	PA3 pin function control register	PA3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C194h	MPC	PA4 pin function control register	PA4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C195h	MPC	PA5 pin function control register	PA5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C196h	MPC	PA6 pin function control register	PA6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C197h	MPC	PA7 pin function control register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C198h	MPC	PB0 pin function control register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C199h	MPC	PB1 pin function control register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ah	MPC	PB2 pin function control register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Bh	MPC	PB3 pin function control register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Ch	MPC	PB4 pin function control register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Dh	MPC	PB5 pin function control register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Eh	MPC	PB6 pin function control register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C19Fh	MPC	PB7 pin function control register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A0h	MPC	PC0 pin function control register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A1h	MPC	PC1 pin function control register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A2h	MPC	PC2 pin function control register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A3h	MPC	PC3 pin function control register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A4h	MPC	PC4 pin function control register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A5h	MPC	PC5 pin function control register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A6h	MPC	PC6 pin function control register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1A7h	MPC	PC7 pin function control register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C8h	MPC	PH0 pin function control register	PH0PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1C9h	MPC	PH1 pin function control register	PH1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CAh	MPC	PH2 pin function control register	PH2PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1CBh	MPC	PH3 pin function control register	PH3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D1h	MPC	PJ1 pin function control register	PJ1PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C28Fh	SYSTEM	Flash HOCO software standby control register	FHSSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C294h	SYSTEM	High-speed clock oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C295h	SYSTEM	PLL power control register	PLLPCR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK
0008 C297h	SYSTEM	Voltage monitoring circuit/comparator A control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK

Table 5.4 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0		—	—	30		

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC				Unit	Test Conditions
			1.8 to 2.7 V		2.7 to 3.6 V			
			Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	|5|	|150|	|10|	|200|	µA	V_{in} = 0 V

Table 5.9 DC Characteristics (8)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	P_d	—	350	mW	Ta = –40 to 85°C
		—	150		85°C < Ta ≤ 105°C

Note: • Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.10 DC Characteristics (9)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VREFH = 1.8 to AVCC0, VREFH0 = 1.8 to AVCC0, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	Conversion time = 2 µs	I_{AVCC0}	—	0.65	1.1	mA	
	Temperature sensor enabled while waiting for A/D conversion			—	60	150	µA	
	During D/A conversion (per channel)		I_{VREFH}*1	—	0.25	0.45	mA	
	Waiting for A/D, D/A conversion (all units)*2		—	—	0.2	2.0	µA	
Reference power supply current	During A/D conversion	Conversion time = 2 µs	I_{VREFH0}	—	0.05	0.1	mA	
	Waiting for A/D conversion			—	0.2	0.4	µA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. The values are the sum of I_{AVCC0} and I_{REFH}.

Table 5.11 DC Characteristics (10)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During ΔΣ A/D conversion (per channel)	AI_{CCA}	—	0.9	1.4	mA	
	ΔΣ A/D bias circuit operating current		—	90	130	µA	
	When ΔΣ A/D conversion is stopped (all units)		—	0.07	1.8		

Table 5.12 DC Characteristics (11)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.13 DC Characteristics (12)

Conditions: VCC = AVCC0 = AVCCA = 0 to 3.6 V, VREFH = VREFH0 = 0 to AVCC0, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrVCC	0.02	—	20	ms/V	At cold start

Table 5.14 DC Characteristics (13)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

The ripple voltage must meet the allowable ripple frequency $fr_{(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.8 V).
When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$fr_{(VCC)}$	—	—	10	kHz	Figure 5.10 VCC × 0.1 < $V_{r(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 5.10 VCC × 0.05 < $V_{r(VCC)}$ ≤ VCC × 0.1
		—	—	10	MHz	Figure 5.10 $V_{r(VCC)}$ ≤ VCC × 0.05
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

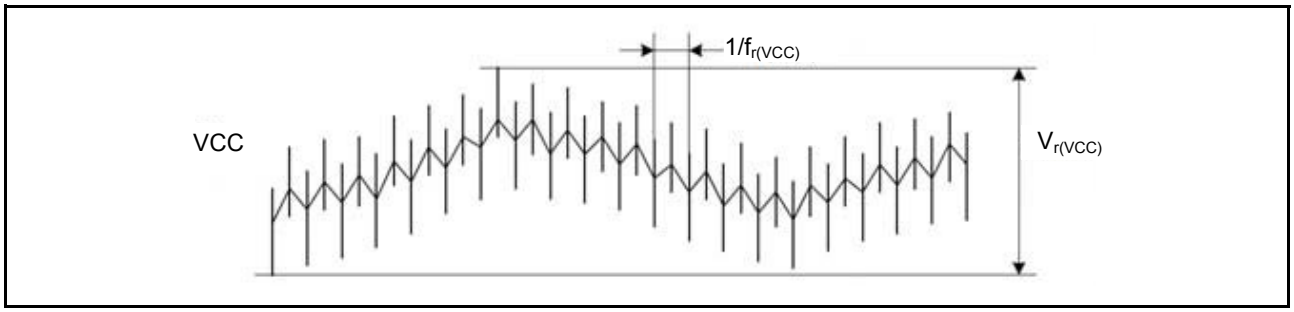


Figure 5.10 Ripple Waveform

Table 5.15 Permissible Output Currents (1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
when total power (mW) < 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	4.0	mA
	High-drive output mode		8.0	
Permissible output low current (total)	Total of all output pins	I_{OL}	60	
Permissible output high current (maximum value per 1 pin)	Normal output mode	I_{OH}	–4.0	
	High-drive output mode		–8.0	
Permissible output high current (total)	Total of all output pins	I_{OH}	–60	

Table 5.16 Permissible Output Currents (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
when total power (mW) ≥ 1000 – 10 × Ta

Item		Symbol	Max.	Unit
Permissible output low current (maximum value per 1 pin)	Normal output mode	I_{OL}	2.0	mA
	High-drive output mode		4.0	
Permissible output low current (total)	Total of all output pins	I_{OL}	30	
Permissible output high current (maximum value per 1 pin)	Normal output mode	I_{OH}	–2.0	
	High-drive output mode		–4.0	
Permissible output high current (total)	Total of all output pins	I_{OH}	–30	

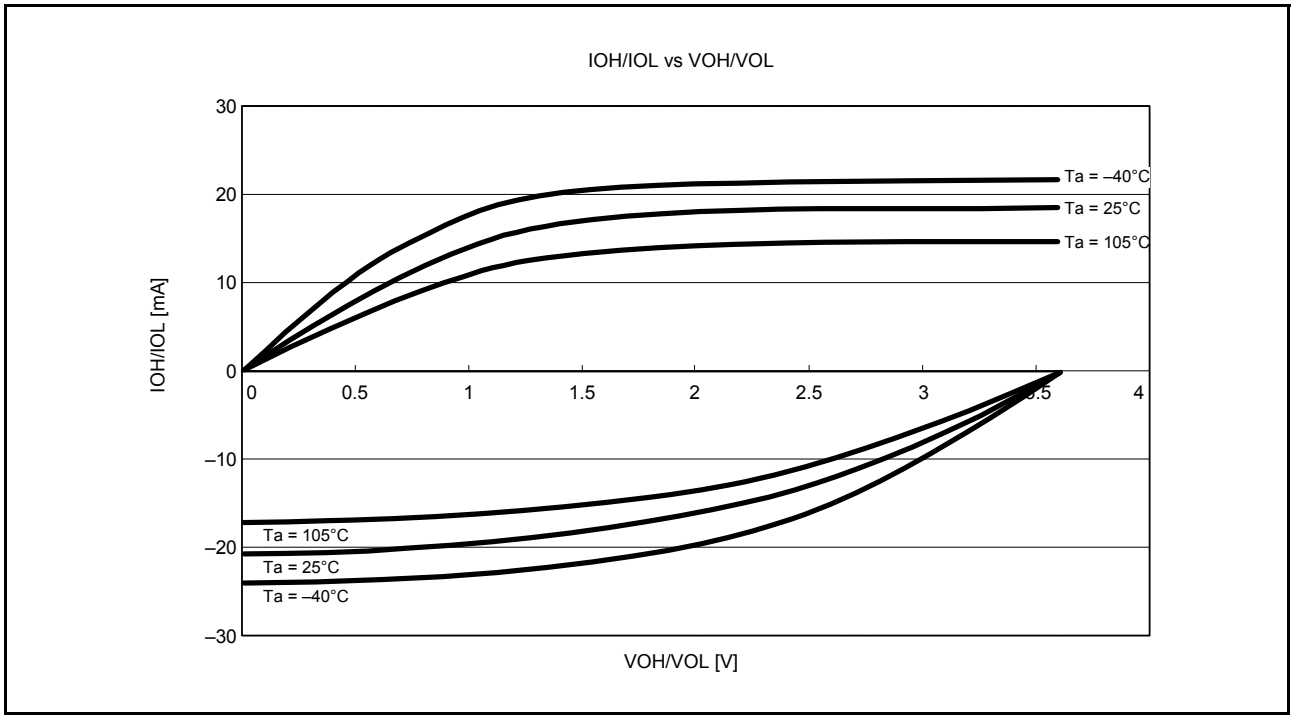


Figure 5.15 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 3.6 V when Normal Output is Selected (Reference Data)

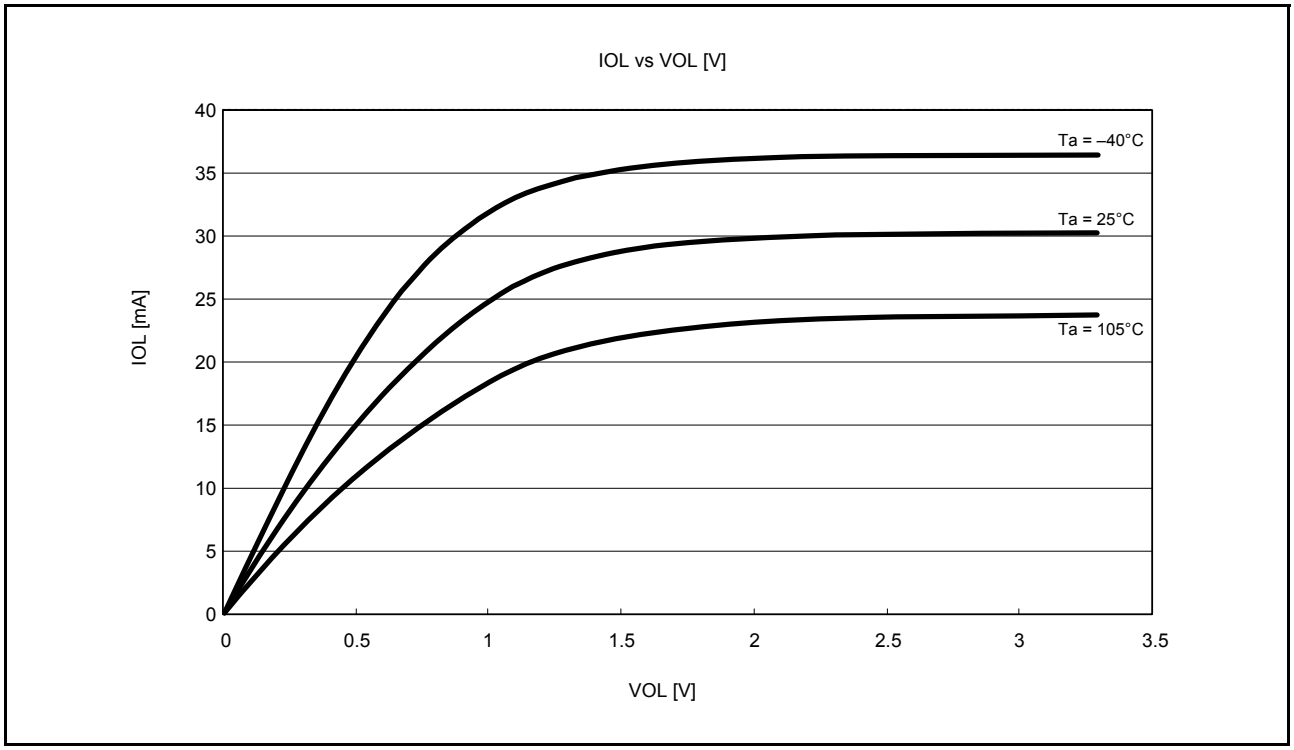


Figure 5.23 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

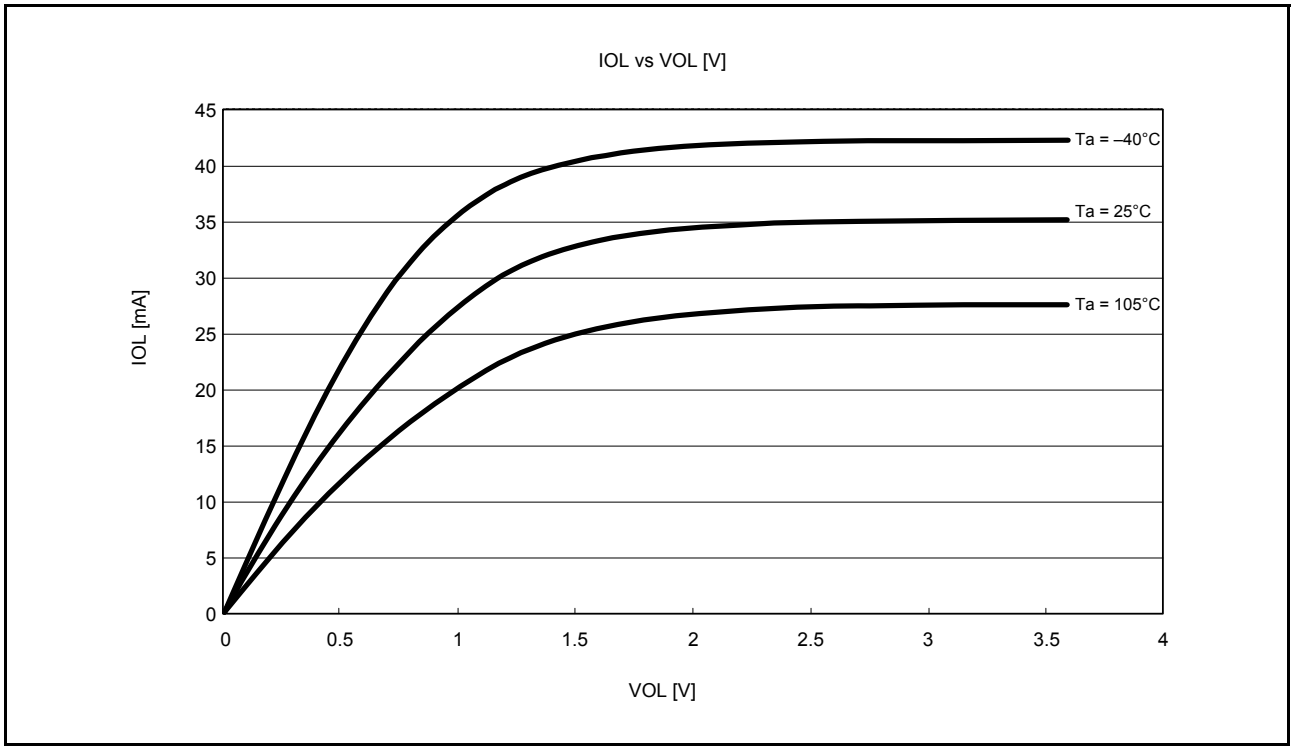


Figure 5.24 VOL and IOL Temperature Characteristics of RIIC Output Pin at VCC = 3.6 V (Reference Data)

Table 5.24 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	4	8	MHz
	FlashIF clock (FCLK)*1		4	8	
	Peripheral module clock (PCLKA)		4	8	
	Peripheral module clock (PCLKB)		4	8	
	Peripheral module clock (PCLKC)*2		4	8	
	Peripheral module clock (PCLKD)*3		4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.25 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	
	Peripheral module clock (PCLKA)		32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	
	Peripheral module clock (PCLKC)*2		32.768	32.768	
	Peripheral module clock (PCLKD)*3		32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The A/D converter cannot be used.

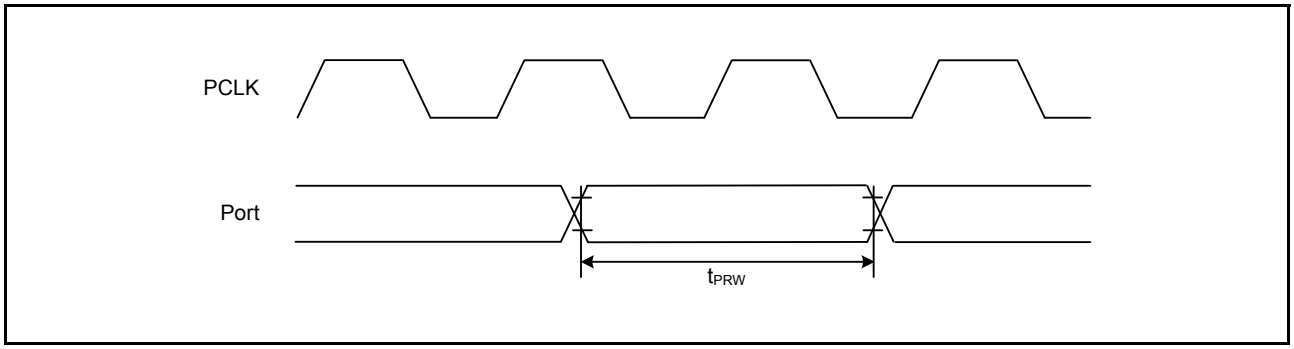


Figure 5.41 I/O Port Input Timing

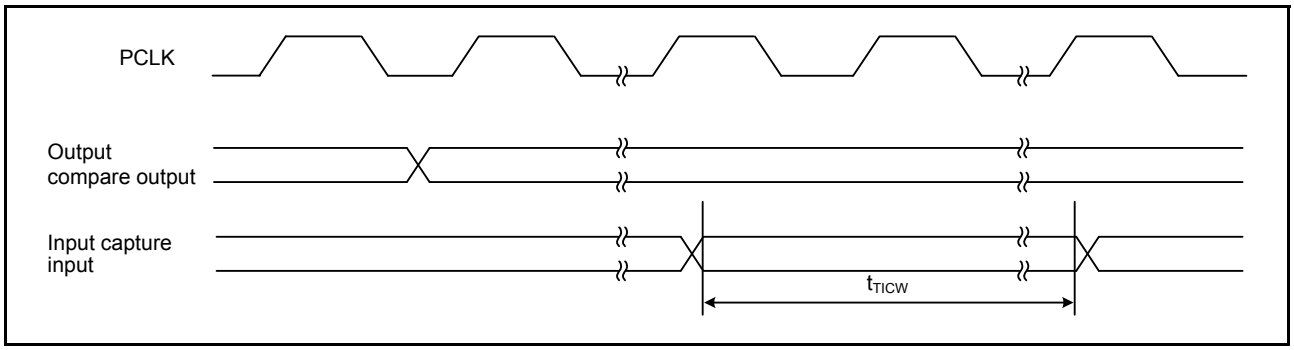


Figure 5.42 MTU Input/Output Timing

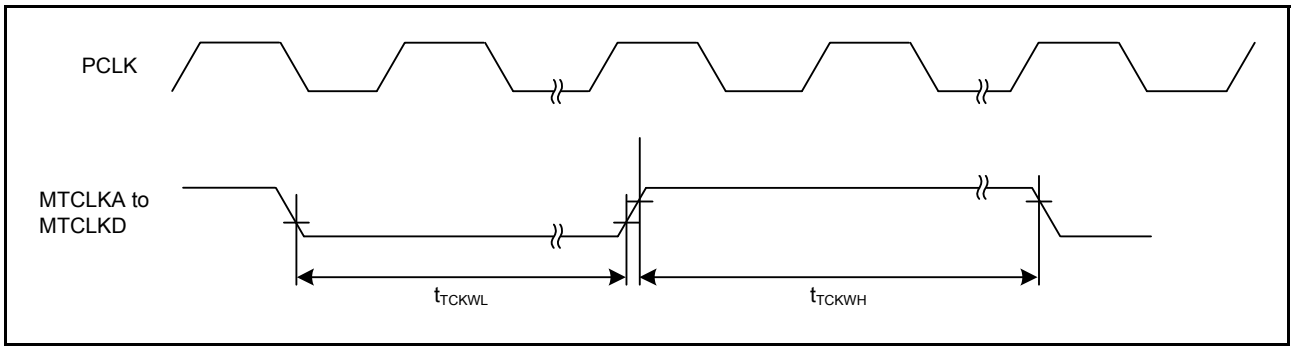


Figure 5.43 MTU Clock Input Timing

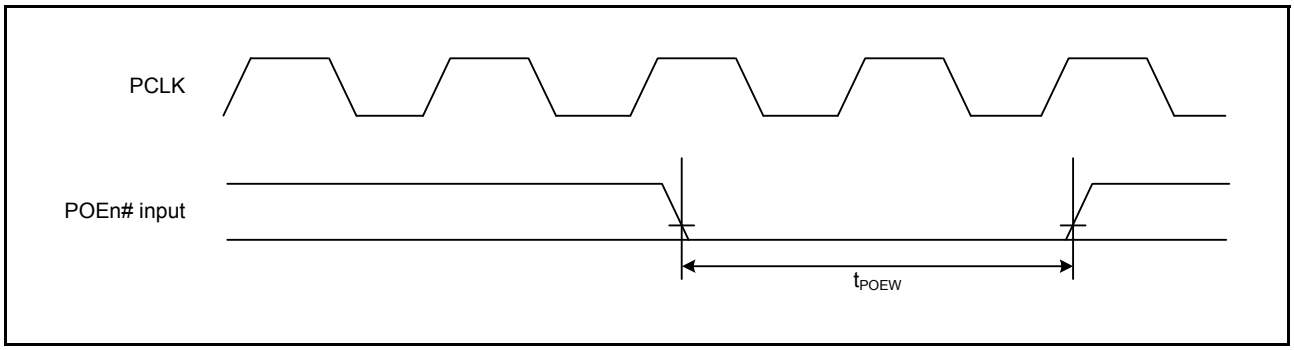
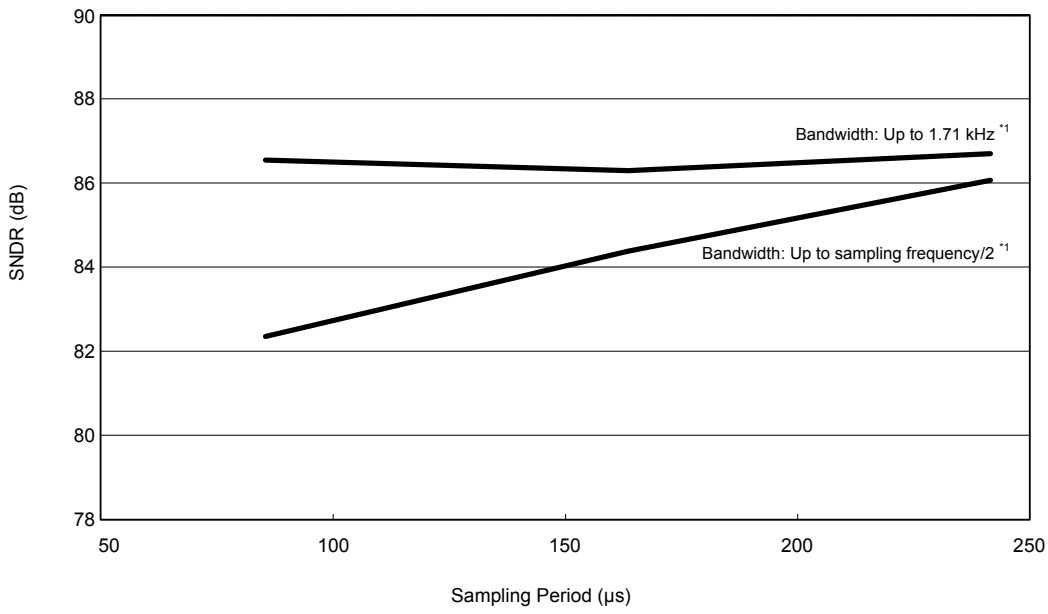
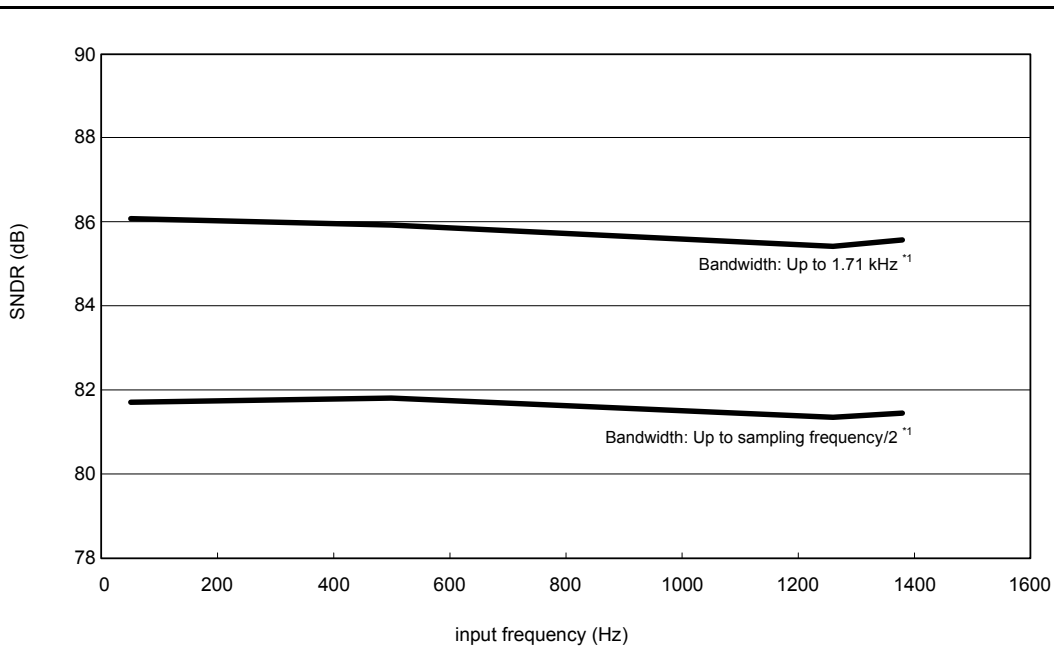


Figure 5.44 POE# Input Timing



Note 1. Gain: ×1, input frequency: 50 Hz, input amplitude: 500 mV

Figure 5.58 Sampling Period Dependency of SNDR (Reference Data)



Note 1. Gain: ×1, sampling period: 81.92 µs, input amplitude: 500 mV

Figure 5.59 Input Frequency Dependency of SNDR (Reference Data)

5.10 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	1.30	1.40	1.55	V	Figure 5.64 and Figure 5.65
		Low power consumption function enabled*2		1.00	1.20	1.45		
	Voltage detection circuit (LVD0)*3		V_{det0_1}	2.70	2.80	2.90	V	Figure 5.66
			V_{det0_2}	1.80	1.90	2.00		
	Voltage detection circuit (LVD1)*4		V_{det1_7}	2.95	3.10	3.25	V	Figure 5.67
			V_{det1_8}	2.85	2.95	3.05		
			V_{det1_9}	2.70	2.80	2.90		At falling edge VCC
			V_{det1_A}	2.55	2.65	2.75		
			V_{det1_B}	2.40	2.50	2.60		
			V_{det1_C}	2.25	2.35	2.45		
			V_{det1_D}	2.10	2.20	2.30		
			V_{det1_E}	1.95	2.05	2.15		
			V_{det1_F}	1.80	1.90	2.00		

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. When the CPU is in a mode other than software standby and deep software standby modes, when the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 0, or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 0.

Note 2. When the CPU transits to software standby mode with the FHSSBYCR.SOFTCUT[2] bit set to 1 or when the CPU transits to deep software standby mode with the DPSBYCR.DEEPCUT1 bit set to 1.

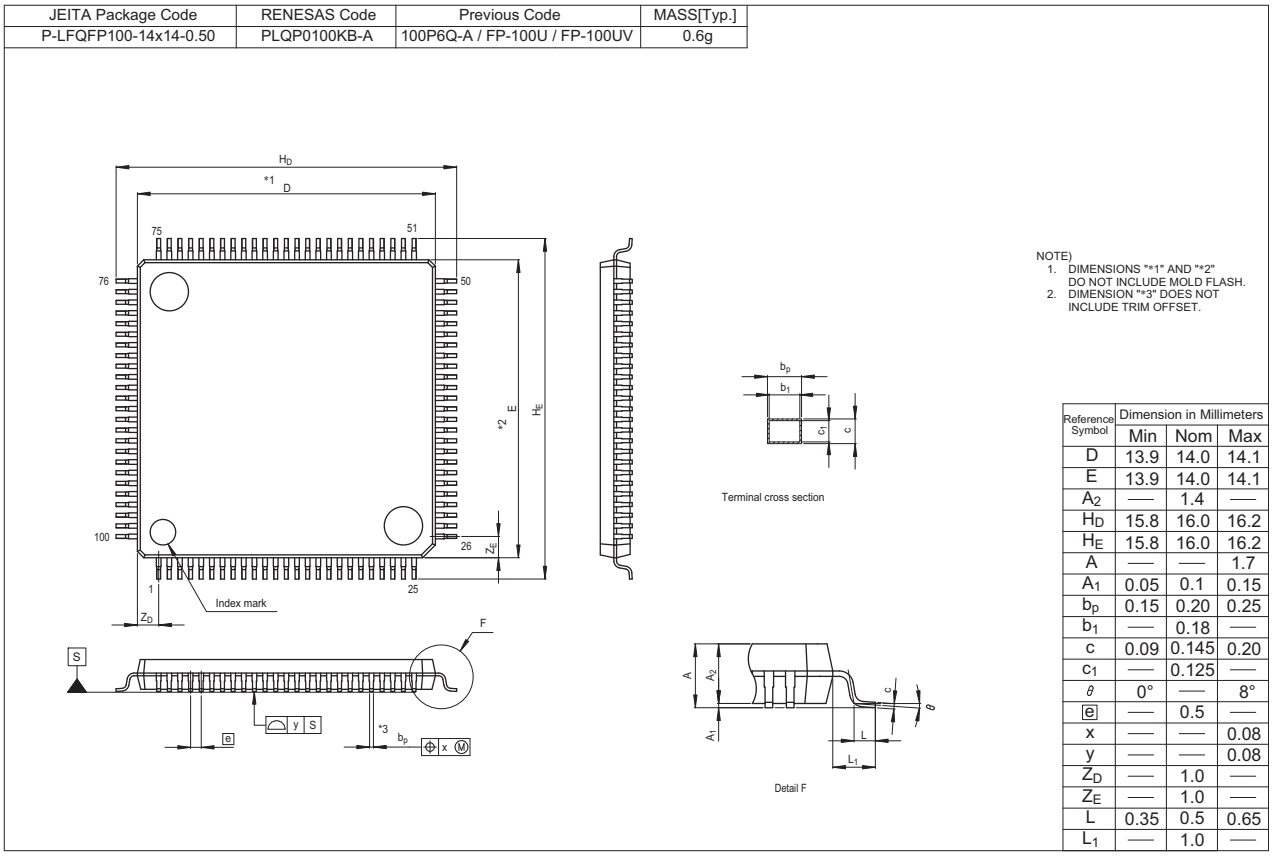
Note 3. # in the symbol Vdet0_# denotes the value of the LDSEL[1:0] bits.

Note 4. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

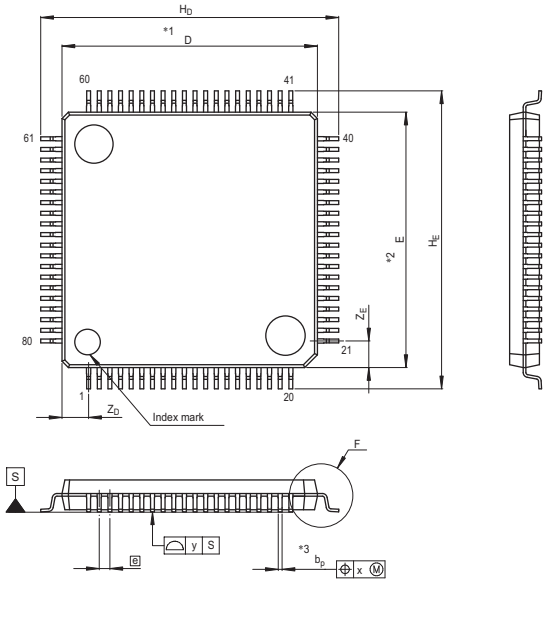
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 100-Pin LQFP (PLQP0100KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure B 80-Pin LQFP (PLQP0080KB-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	2014.08.28	Features		
		1	LGA package, added	TN-RX*-A072A/E
		1. Overview		
		5	Table 1.1 Outline of Specifications: Package added	TN-RX*-A072A/E
		5	Table 1.1 Outline of Specifications: Note 2 added	TN-RX*-A073A/E
		5	Table 1.1 Outline of Specifications: Note 3 added	
		5	Table 1.2 Comparison of Functions for Different Packages, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note 1 added	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note, Note 2 added	
		7	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed	TN-RX*-A072A/E
		9	Table 1.4 Pin Functions: Realtime clock changed	
		15	Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View), added	TN-RX*-A072A/E
		23 to 25	Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA), added	TN-RX*-A072A/E
		3. Address Space		
		29	Figure 3.1 Memory Map, changed	
		4. I/O Registers		
		54 to 55	Table 4.1 List of I/O Registers (Address Order): FEFF FAC0h to FEFF FBD3h added	
		5. Electrical Characteristics		
		57	Table 5.3 DC Characteristics (2)	TN-RX*-A074A/E
		58	Table 5.4 DC Characteristics (3), changed	TN-RX*-A074A/E
		59	Table 5.6 DC Characteristics (5), changed	TN-RX*-A074A/E
		60	Table 5.7 DC Characteristics (6), changed	TN-RX*-A074A/E
		68	Table 5.9 DC Characteristics (8), added	TN-RX*-A074A/E
		68	Table 5.10 DC Characteristics (9), changed	
		68	Table 5.11 DC Characteristics (10), changed	
		69	Table 5.14 DC Characteristics (13), changed	TN-RX*-A074A/E
		69	Table 5.15 Permissible Output Currents (1), changed Table 5.16 Permissible Output Currents (2), added	TN-RX*-A074A/E
		70	Table 5.18 Output Values of Voltage (2), changed	TN-RX*-A074A/E
		82	Table 5.26 Clock Timing, changed	TN-RX*-A097A/E
		83	Table 5.26 Clock Timing: Note 5 changed	TN-RX*-A105A/E
		83	Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		87	Figure 5.35 Reset Input Timing at Power-On, changed	TN-RX*-A074A/E
		94	Table 5.33 Timing of On-Chip Peripheral Modules (4), changed	TN-RX*-A074A/E
		103	Table 5.36 ΔΣ A/D Conversion Characteristics, changed	TN-RX*-A105A/E
		104	Figure 5.55 Differential Input Amplitude, changed	
		108	Table 5.37 A/D Conversion Characteristics (1), changed	TN-RX*-A074A/E
		108	Figure 5.61 AVCC to VREFH0 Voltage Range, added	TN-RX*-A074A/E
		109	Table 5.39 A/D Conversion Characteristics (2), changed	TN-RX*-A074A/E
		111	Differential nonlinearity error (DNL), description changed	TN-RX*-A073A/E
		115	Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1): Note1, Note2 changed	TN-RX*-A074A/E
		Appendix 1. Package Dimensions		
		128	Figure D. 100-Pin TFLGA (PTLG0100JA-A), added	TN-RX*-A072A/E

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.