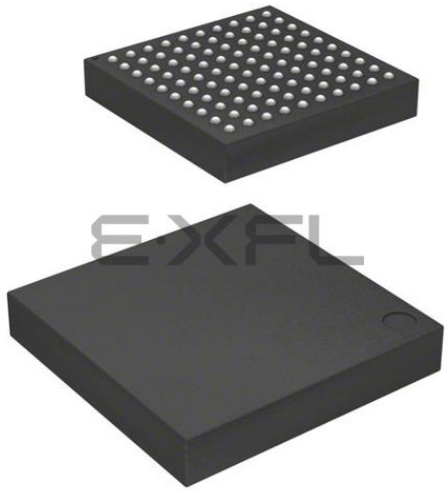

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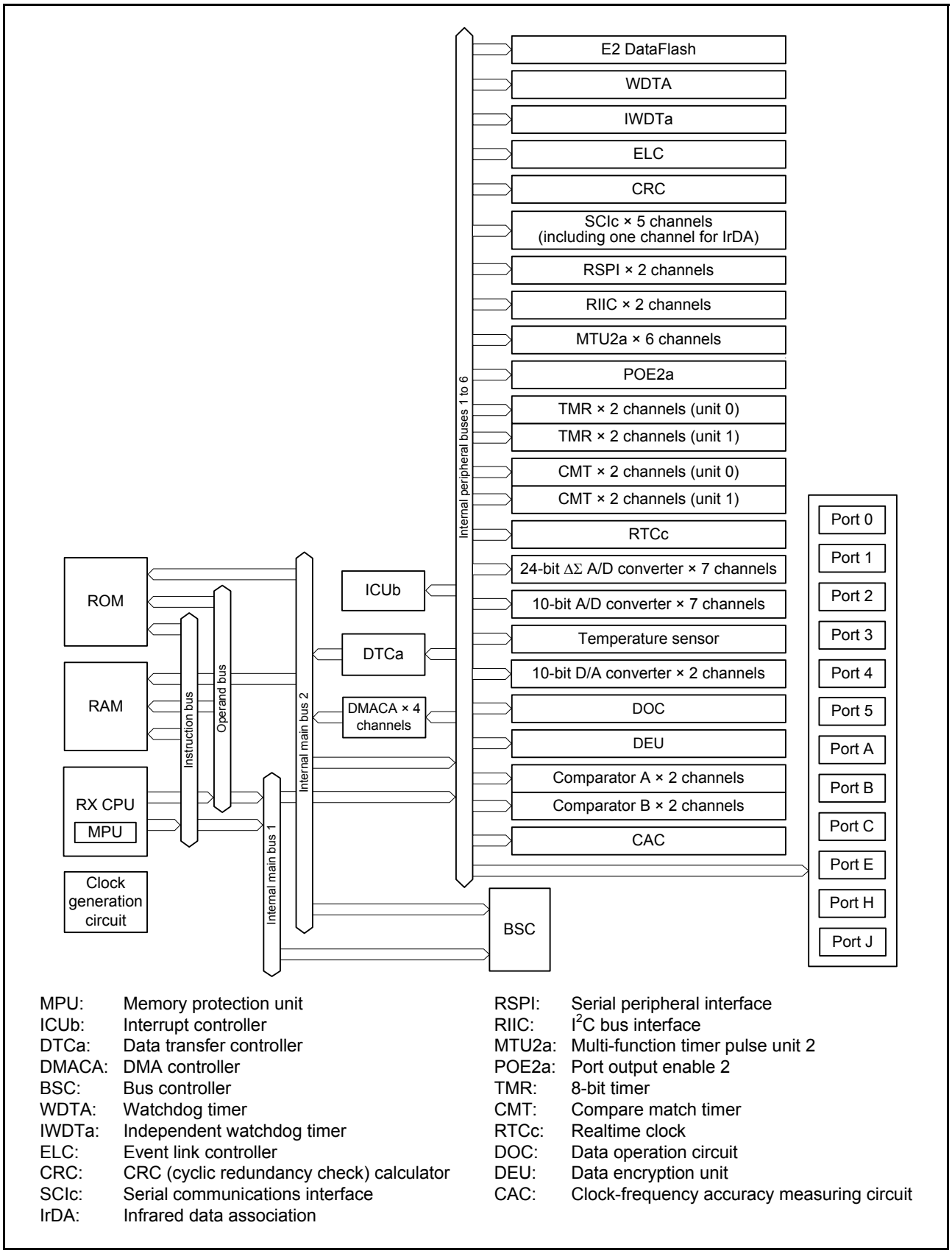
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a7bdlj-u0

1.3 Block Diagram

Figure 1.2 shows a block diagram (100-pin package).



MPU: Memory protection unit
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIc: Serial communications interface
IrDA: Infrared data association

RSPI: Serial peripheral interface
RIIC: I^2C bus interface
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
TMR: 8-bit timer
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
DEU: Data encryption unit
CAC: Clock-frequency accuracy measuring circuit

Figure 1.2 Block Diagram (100-Pin Package)

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
42		P52		SSLB3	
43		P51		SSLB2	
44		P50		SSLB1	
45		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	
51		PC1	MTIOC3A	SCK5/SSLA2	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
56		PB4		CTS9#/RTS9#/SS9#	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
58		PB2		CTS6#/RTS6#/SS6#	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC				
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
62	VSS				
63		PA7		MISOA	
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
65		PA5		RSPCKA	
66		PA4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
71		PE7		MISOB	IRQ7-DS
72		PE6		MOSIB	IRQ6
73	BGR_BO				
74					ANDS0N
75					ANDS0P
76					ANDS1N
77					ANDS1P
78					ANDS2N

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
1	VREFH				
2		P03			AN4/DA0
3	VREFL				
4	VCL				
5		PJ1	MTIOC3A		
6	MD				FINED
7	XCIN				
8	XCOUT				
9	RES#				
10	XTAL	P37			
11	VSS				
12	EXTAL	P36			
13	VCC				
14		P35			NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/ RTCIC2
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/MISOB	IRQ0-DS/RTCIC0
19		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/MOSIB	
21		P21	MTIOC1B/TMCI0	SCL1	
22		P20	MTIOC1A/TMRI0	SDA1	
23		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
24		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0-DS	IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
27		P13	MTIOC0B/TMO3	SDA0	IRQ3
28		P12	TMCI1	SCL0	IRQ2
29		PH3	TMCI0		
30		PH2	TMRI0		IRQ1
31		PH1	TMO0		IRQ0
32		PH0			CACREF
33		P55	MTIOC4D/TMO3		
34		P54	MTIOC4B/TMCI1		
35		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/MISOA	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	
37		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	
41		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	

Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (3 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
J2		P21	MTIOC1B/TMCI0	SCL1	
J3		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA0-DS	IRQ7
J4		P13	MTIOC0B/TMO3	SDA0	IRQ3
J5		PH0			CACREF
J6		PH3	TMCI0		
J7		P50		SSLB1	
J8		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
J9		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
J10		PC1	MTIOC3A	SCK5/SSLA2	
K1		P23	MTIOC3D/MTCLKD		
K2		P22	MTIOC3B/MTCLKC/TMO0		
K3		P20	MTIOC1A/TMRI0	SDA1	
K4		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
K5		PH2	TMRI0		IRQ1
K6		PH1	TMO0		IRQ0
K7		P51		SSLB2	
K8		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
K9		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
K10		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5	

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory map.

Table 4.1 List of I/O Registers (Address Order) (6 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8		2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8		2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8		2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8		2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8		2 ICLK
0008 716Bh	ICU	DTC activation enable register 107	DTCER107	8	8		2 ICLK
0008 716Ch	ICU	DTC activation enable register 108	DTCER108	8	8		2 ICLK
0008 716Dh	ICU	DTC activation enable register 109	DTCER109	8	8		2 ICLK
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8		2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8		2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8		2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8		2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8		2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8		2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8		2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8		2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8		2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8		2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8		2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8		2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8		2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8		2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8		2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8		2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8		2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8		2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8		2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8		2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8		2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8		2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8		2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8		2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8		2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8		2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8		2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8		2 ICLK
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8		2 ICLK
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8		2 ICLK
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8		2 ICLK
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8		2 ICLK
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8		2 ICLK
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8		2 ICLK
0008 71D1h	ICU	DTC activation enable register 209	DTCER209	8	8		2 ICLK
0008 71D2h	ICU	DTC activation enable register 210	DTCER210	8	8		2 ICLK
0008 71D3h	ICU	DTC activation enable register 211	DTCER211	8	8		2 ICLK
0008 71D4h	ICU	DTC activation enable register 212	DTCER212	8	8		2 ICLK
0008 71D5h	ICU	DTC activation enable register 213	DTCER213	8	8		2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8		2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8		2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8		2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8		2 ICLK
0008 71E4h	ICU	DTC activation enable register 228	DTCER228	8	8		2 ICLK
0008 71E7h	ICU	DTC activation enable register 231	DTCER231	8	8		2 ICLK
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8		2 ICLK
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8		2 ICLK
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8		2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8		2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8		2 ICLK
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8		2 ICLK
0008 71FCh	ICU	DTC activation enable register 252	DTCER252	8	8		2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8		2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8		2 ICLK
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8		2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8		2 ICLK
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8		2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8		2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8		2 ICLK
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8		2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8		2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8		2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8		2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8		2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8		2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8		2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8		2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8		2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8		2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8		2 ICLK
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8		2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8		2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8		2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8		2 ICLK
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8		2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8		2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8		2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8		2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16		2 ICLK
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8		2 ICLK
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8		2 ICLK
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8		2 ICLK
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8		2 ICLK
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8		2 ICLK
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8		2 ICLK
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8		2 ICLK
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8		2 ICLK
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8		2 ICLK
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8		2 ICLK
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8		2 ICLK
0008 732Ch	ICU	Interrupt source priority register 044	IPR044	8	8		2 ICLK
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8		2 ICLK
0008 7339h	ICU	Interrupt source priority register 057	IPR057	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8320h	RIIC1	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8321h	RIIC1	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8322h	RIIC1	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8323h	RIIC1	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8324h	RIIC1	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8325h	RIIC1	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8326h	RIIC1	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8327h	RIIC1	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8328h	RIIC1	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8329h	RIIC1	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8330h	RIIC1	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8331h	RIIC1	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8332h	RIIC1	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8333h	RIIC1	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

Note 2. When specifying the main clock oscillator stabilization time, load MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 3. Sum of the main clock oscillation stabilization time and the PLL oscillation stabilization time.
Note 4. The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 5. When specifying the sub-clock oscillation stabilization time, load SOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.

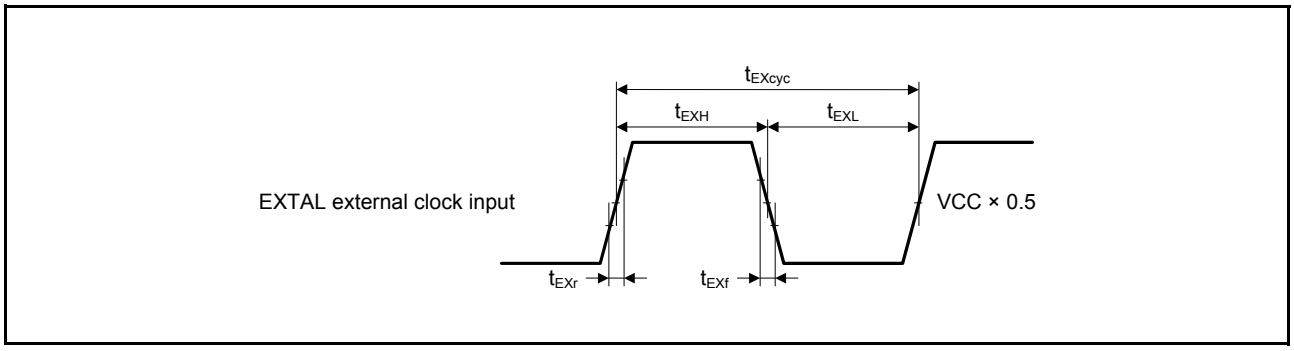


Figure 5.25 EXTAL External Clock Input Timing

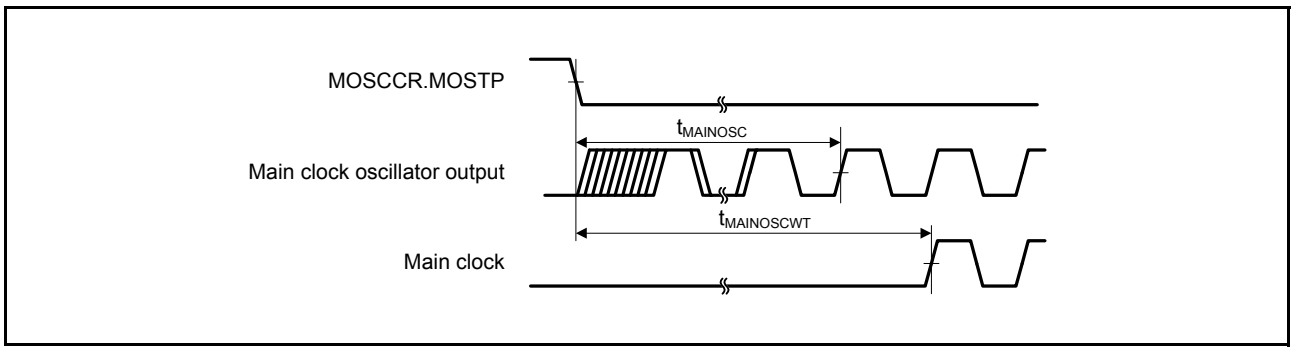


Figure 5.26 Main Clock Oscillation Start Timing

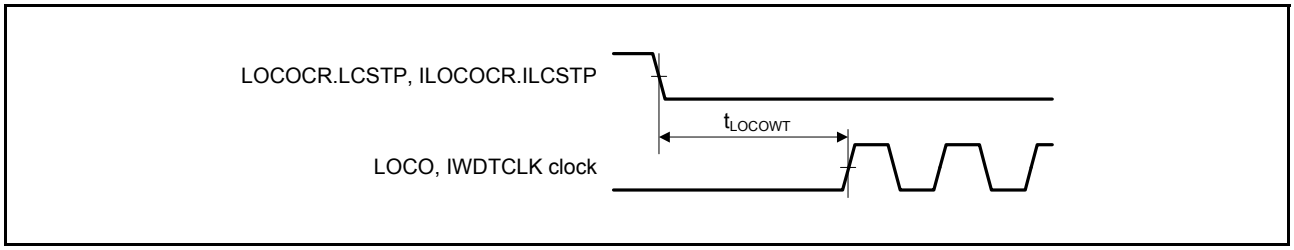


Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing

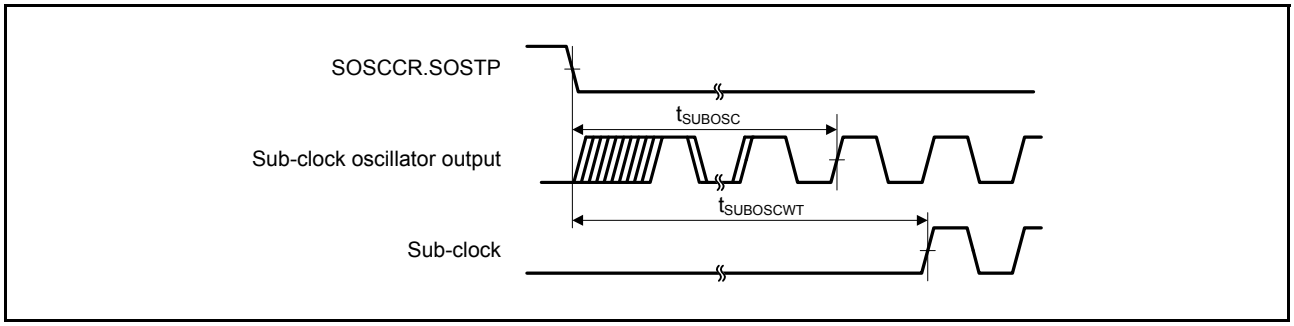


Figure 5.34 Sub-clock Oscillation Start Timing

5.4.1 Reset Timing

Table 5.27 Reset Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	8	—	—	ms	Figure 5.35
	Deep software standby mode	t_{RESWD}	8	—	—	ms	Figure 5.36
	Software standby mode, low-speed operating modes 1 and 2	t_{RESWS}	1	—	—	ms	
	Programming or erasure of the ROM or E2 DataFlash memory or blank checking of the E2 DataFlash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Wait time after RES# cancellation		t_{RESWT}	—	—	912	µs	Figure 5.35
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	—	—	1.4	ms	

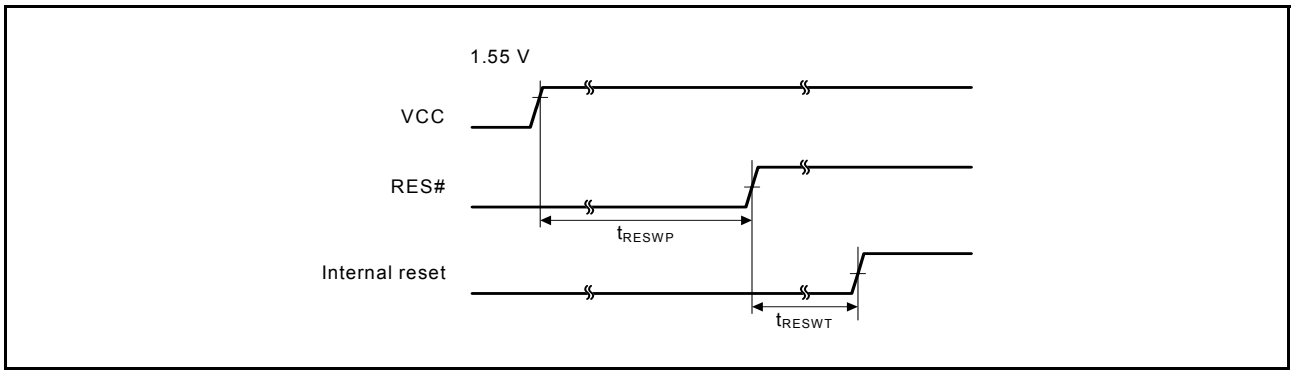


Figure 5.35 Reset Input Timing at Power-On

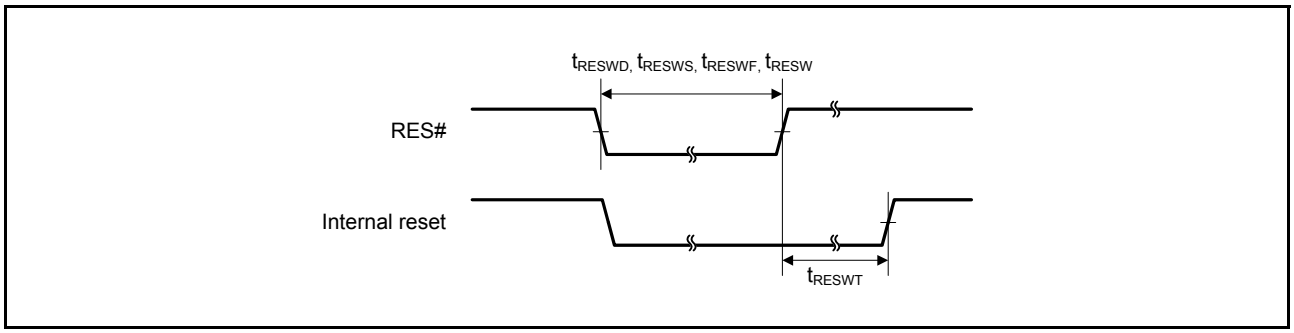


Figure 5.36 Reset Input Timing

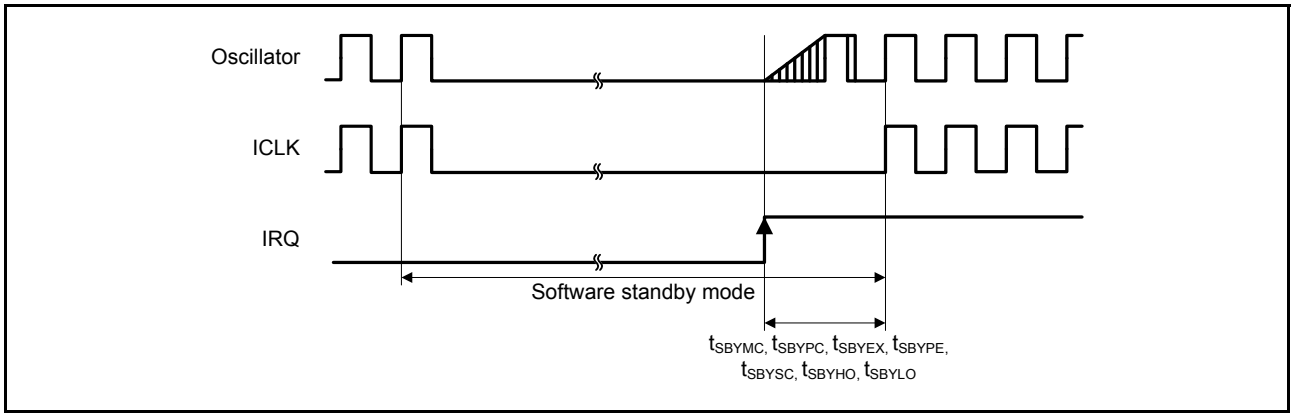


Figure 5.37 Software Standby Mode Cancellation Timing

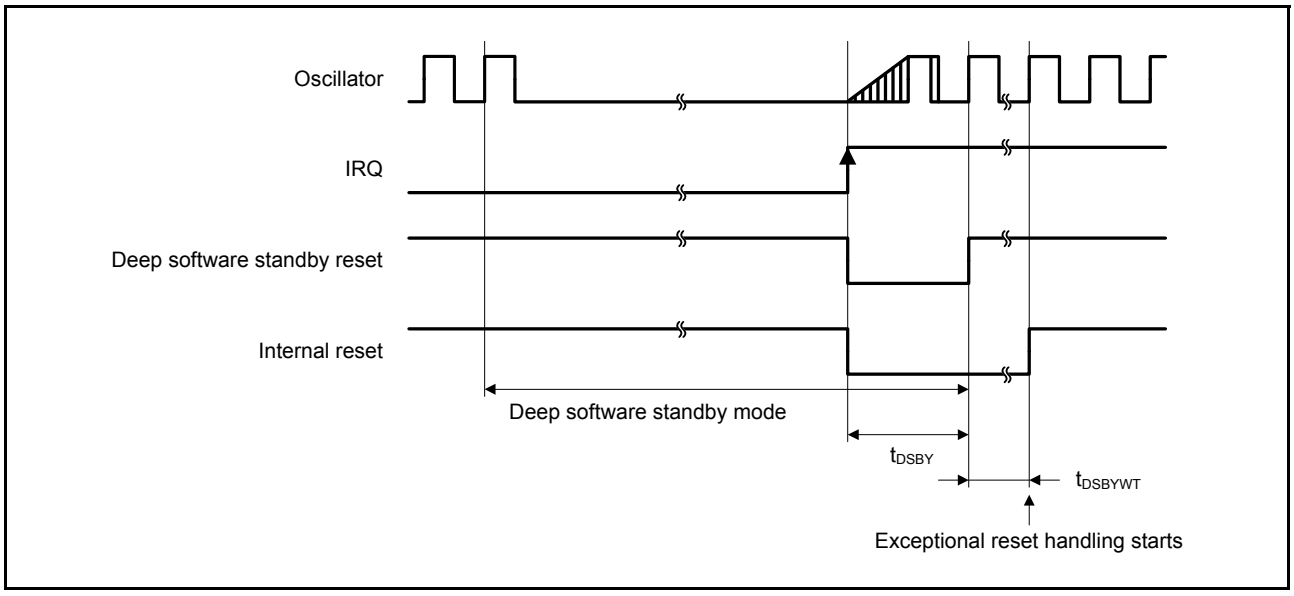


Figure 5.38 Deep Software Standby Mode Cancellation Timing

5.5 ΔΣ A/D Conversion Characteristics

Table 5.36 ΔΣ A/D Conversion Characteristics

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, fPCLKC = 25 MHz, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	24	24	24	Bit	
Reference voltage (VREFDSH)	590	600	610	mV	EXREF = 0
BGR_BO pin applied voltage	—	1220	—	mV	EXREF = 1
BGR_BO pin voltage to reference voltage conversion coefficient	—	0.492	—	—	EXREF = 1
BGR_BO pin impedance	135	—	—	kΩ	EXREF = 1
Reference voltage temperature coefficient	—	—	30	ppm/°C	
Gain (×1)	—	1.00	—	—	
Gain (×2)	—	2.00	—	—	
Gain (×4)	—	4.00	—	—	
Gain (×8)	—	8.00	—	—	
Gain (×16)	—	16.00	—	—	
Gain (×32)	—	32.00	—	—	
Gain (×64)	—	64.00	—	—	
Differential input voltage (ANDSiP - ANDSiN) (i = 0 to 3)	–500.0	—	500.0	mV	GAIN = 000b, Figure 5.55
	–250.0	—	250.0	mV	GAIN = 001b
	–125.0	—	125.0	mV	GAIN = 010b
	–62.5	—	62.5	mV	GAIN = 011b
	–31.2	—	31.2	mV	GAIN = 100b
	–14.4	—	14.4	mV	GAIN = 101b
	–5.0	—	5.0	mV	GAIN = 110b
Differential input Common mode voltage	—	700.0	—	mV	
Single-ended input voltage	–500.0	—	500.0	mV	GAIN = 00b, Figure 5.56
	–250.0	—	250.0	mV	GAIN = 01b
	–125.0	—	125.0	mV	GAIN = 10b
Conversion with the ΔΣ modulator only Differential input voltage	–500.0	—	500.0	mV	GAIN = 000b, 001b, 010b, 011b, 100b (DSADGSR0 to 3) GAIN = 00b, 01b, 10b (DSADGSR4 to 6)
	–250.0	—	250.0	mV	GAIN = 101b (DSADGSR0 to 3)
	–125.0	—	125.0	mV	GAIN = 110b (DSADGSR0 to 3)
Conversion with the ΔΣ modulator only Common mode input voltage	—	700.0	—	mV	
PGA input pin bias voltage	—	700.0	—	mV	
PGA output common mode voltage	—	700.0	—	mV	
Reference voltage startup time	—	1	5	ms	
PGA and ΔΣ modulator startup time	—	—	0.1	ms	
Input pull-up resistor	120	200	—	kΩ	
Input impedance for differential input (×1, ×2, ×4, ×8)	40	66	—	kΩ	
Input impedance for differential input (×16, ×32, ×64)	30	50	—	kΩ	
Input impedance for single-ended input (×1)	48	80	—	kΩ	
Input impedance for single-ended input (×2)	51	86	—	kΩ	

5.8 Temperature Sensor Characteristics

Table 5.42 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCCA = VREFH0 = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	AVCC0 = 3.6		—	13.98	—		PGAGAIN = 10b
Output voltage (@25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.63
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	

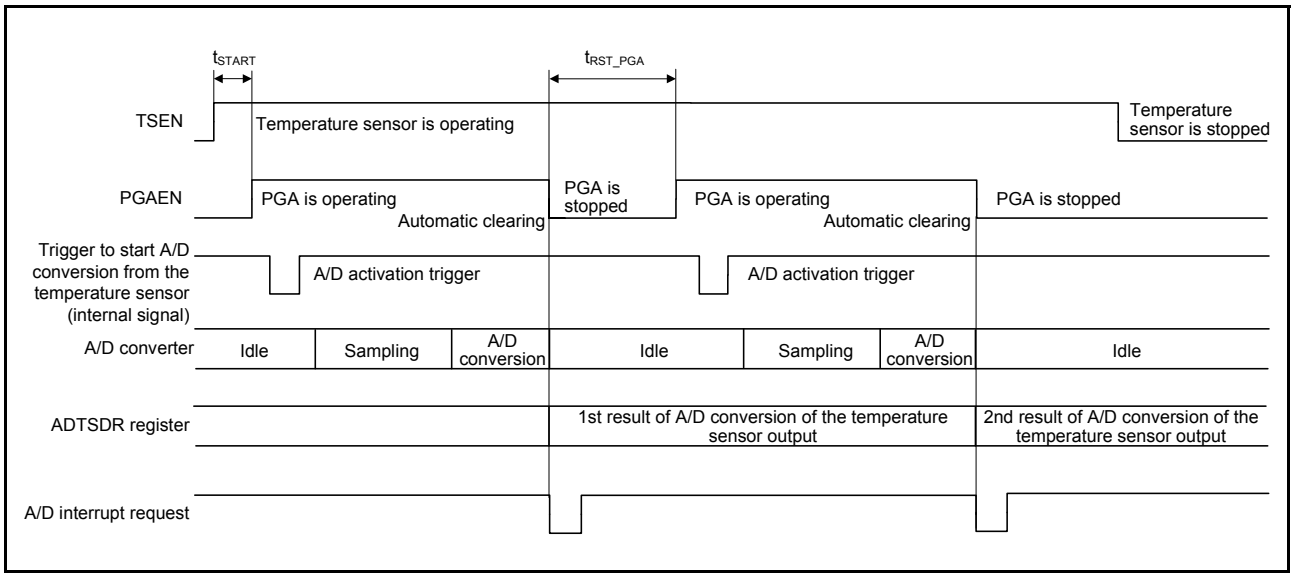


Figure 5.63 A/D Conversion Timing Example of the Temperature Sensor (Two Conversions Performed)

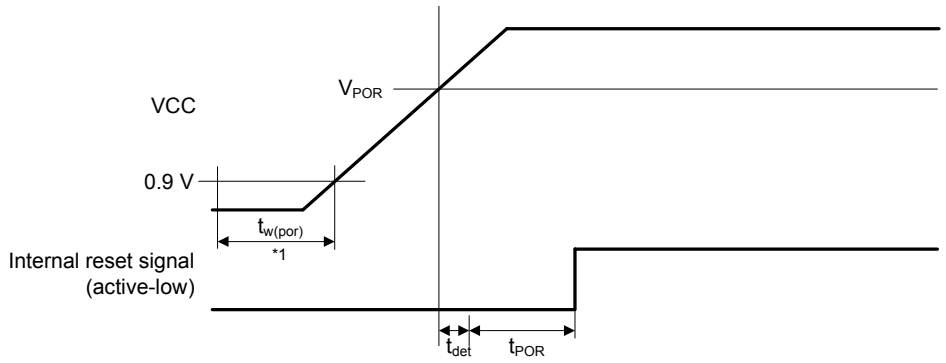
5.9 Comparator Characteristics

Table 5.43 Comparator Characteristics

Conditions: VCC = AVCC0 = AVCCA =1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Comparator A	External reference voltage input range	LVREF	1.4	—	VCC	V	
	External comparison voltage (CMPA1, CMPA2) input range	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±50	±150	mV	
	Comparator output delay time*1	—	—	3	—	µs	At falling edge VI = LVREF – 110 mV
			—	2	—	µs	At falling edge VI < LVREF – 1 V
			—	3	—	µs	At rising edge VI = LVREF + 160 mV
			—	1.5	—	µs	At rising edge VI > LVREF + 1 V
	Comparator operating current	ICMPA	—	0.5	—	µA	VCC = 3.3 V
Comparator B	Input reference voltage for CVREFB0, CVREFB1	VREF	0	—	VCC – 1.4	V	
	Input voltage for CMPB0, CMPB1	VI	–0.3	—	VCC + 0.3	V	
	Offset	—	—	±10	±100	mV	
	Comparator output delay time	t_d	—	—	1	µs	VI = VREF + 100 mV
	Comparator operating current	ICMPB	—	75	150	µA	VCC = 3.3 V For total two channels

Note 1. When the digital filter is disabled.



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.65 Power-on Reset Timing

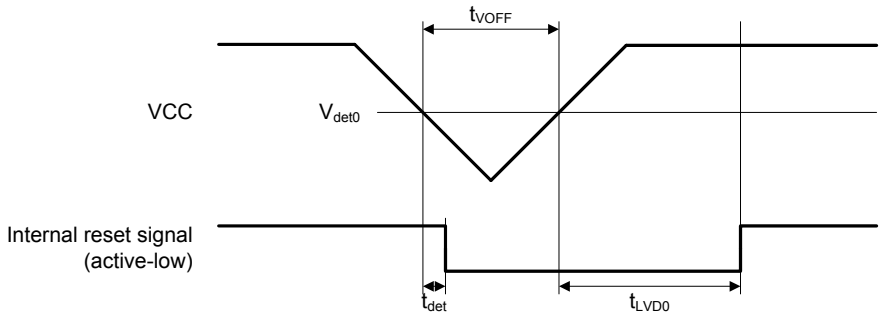


Figure 5.66 Voltage Detection Circuit Timing (V_{det0})

5.13 E2 DataFlash Characteristics

Table 5.50 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	—	—	Times	
Data hold time	After 100000 times of N_{DPEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This result is obtained from reliability testing.

Table 5.51 E2 DataFlash Characteristics (2)
: high-speed operating mode, medium-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.1	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.14	2.3	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.1	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.4	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8.8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.1	13.3	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	38	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	3.0	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.804	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.804	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.804	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.804	ms

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.