# Renesas Electronics America Inc - R5F521A8BDFM#30 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 3x24b, 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a8bdfm-30 |

**Table 1.1 Outline of Specifications (3 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Serial communications interfaces (SCIc) | • 5 channels (channel 1, 5, 6, 8, 9) (including one channel for IrDA)<br>• Serial communications modes:<br>Asynchronous, clock synchronous, and smart-card interface<br>• On-chip baud rate generator allows selection of the desired bit rate<br>• Choice of LSB-first or MSB-first transfer<br>• Average transfer rate clock can be input from TMR timers (SCI5 and SCI6)<br>• Simple IIC<br>• Simple SPI |
| | IrDA interface (IRDA) | • 1 channel (SCI5 is used)<br>• Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0 |
| | $I^2C$ bus interface (RIIC) | • 2 channels<br>• Communications formats:<br>$I^2C$ bus format/SMBus format<br>• Master/slave selectable<br>• Supports the fast mode |
| | Serial peripheral interface (RSPI) | • 2 channels<br>• Transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>• Capable of handling serial transfer as a master or slave<br>• Data formats<br>• Choice of LSB-first or MSB-first transfer<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Double buffers for both transmission and reception |
| 24-bit ΔΣ A/D converter (DSAD) | | • 7 channels: 4-channel differential input for current; 3-channel single-ended input for voltage<br>• x 1 to x 64 PGA for differential input side for current and x 1 to x 4 PGA for single-ended input side for voltage<br>• Minimum conversion time: 81.92 µs (A/D conversion clock: 25 MHz) |
| 10-bit A/D converter (AD) | | • 10 bits (7 channels x 1 unit)<br>• 10-bit resolution<br>• Conversion time: 2.0 µs per channel (A/D conversion clock: 25 MHz)<br>• Operating modes<br>Scan mode (single scan mode and continuous scan mode)<br>• Sample-and-hold function<br>• Self-diagnosis for the A/D converter<br>• Assistance in detecting disconnected analog inputs<br>• A/D conversion start conditions<br>Conversion can be started by software, a conversion start trigger from a timer (MTU), an external trigger signal, a temperature sensor or ELC. |
| Temperature sensor (TEMPSa) | | • Outputs the voltage that changes depending on the temperature<br>• PGA gain switchable: Three levels according to the voltage range |
| D/A converter (DA) | | • 2 channels<br>• 10-bit resolution<br>• Output voltage: 0 V to VREFH |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Data encryption unit (DEU)*1 | | • Encryption and decryption of AES<br>• 128-, 192-, or 256-bit key length<br>• ECB or CBC mode |
| Comparator A (CMPA) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Comparator B (CMPB) | | • 2 channels<br>• Comparison of reference voltage and analog input voltage |
| Data operating circuit (DOC) | | Comparison, addition, and subtraction of 16-bit data |
| Power supply voltage/ Operating frequency | | VCC = 1.8 to 3.6 V: 25 MHz, VCC = 2.7 to 3.6 V: 50 MHz |
| Supply current | | 8.6mA@50MHz (typ) |
| Operating temperature | | D version: –40 to +85°C, G version: –40 to +105°C*2, *3 |

**Table 1.1 Outline of Specifications (4 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Package | | 100-pin LQFP (PLQP0100KB-A) 14 x 14 mm, 0.5-mm pitch<br>80-pin LQFP (PLQP0080KB-A) 12 x 12mm, 0.5-mm pitch<br>64-pin LQFP (PLQP0064KB-A) 10 x 10mm, 0.5-mm pitch<br>100-pin TFLGA (PTLG0100JA-A) 7 × 7 mm, 0.65-mm pitch |
| On-chip debugging system | | E1 emulator (FINE interfaces) |

Note 1. Contact a Renesas Electronics sales office for more information.
Note 2. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.
Note 3. The unique ID specification and the calibration functions of the temperature sensor and the 24-Bit ΔΣ A/D converter of these products differ from other products. For details, see following sections in the *RX21A Group User's Manual: Hardware*.
Section 34.2.11, ΔΣ A/D Input Impedance Calibration Data Register (DSADIIC)
Section 34.2.12, ΔΣ A/D Gain Calibration Data Registers (DSADGmXn) (m = 0 to 6, n = 1, 2, 4, 8, 16, and 32)
Section 37.2.2, Temperature Sensor Calibration Data Registers (TSCDRn) (n = 0,1,3)
Section 37.3, Using the Temperature Sensor
Section 42.2.15, Unique ID Registers (UIDRn) (n = 0 to 3)

**Table 1.2 Comparison of Functions for Different Packages**

| Module/Functions | | RX21A Group | | |
|---|---|---|---|---|
| | | 100 Pins | 80 Pins | 64 Pins |
| Interrupt | External interrupts | NMI, IRQ0 to IRQ7 | | NMI, IRQ0 to IRQ2, IRQ4 to IRQ7 |
| DMA | DMA controller | 4 channels (DMAC0 to DMAC3) | | |
| | Data transfer controller | Supported | | |
| Timers | Multi-function timer pulse unit 2 | 6 channels (MTU0 to MTU5) | | |
| | Port output enable 2 | POE0# to POE3#, POE8# | | |
| | 8-bit timer | 2 channels × 2 units | | |
| | Compare match timer | 2 channels × 2 units | | |
| | Realtime clock | Supported | | |
| | Watchdog timer | Supported | | |
| | Independent watchdog timer | Supported | | |
| Communication function | Serial communications interface | 5 channels (SCI1, 5, 6, 8, 9) (including one channel for IrDA) | | |
| | $I^2C$ bus interface | 2 channels | | 1 channel |
| | Serial peripheral interface | 2 channels | | |
| 24-bit ΔΣ A/D converter | | 7 channels | 4 channels | 3 channels |
| 10-bit A/D converter | | 7 channels (AN0 to AN6) | | 4 channels (AN0, AN1, AN4, AN5) |
| Temperature sensor | | Supported | | |
| D/A converter | | 2 channels | | — |
| CRC calculator | | Supported | | |
| Data encryption unit | | Supported | | |
| Event link controller | | Supported | | |
| Comparator A | | 2 channels | | 1 channel |
| Comparator B | | 2 channels | | |
| Package | | 100-pin LQFP<br>100-pin TFLGA | 80-pin LQFP | 64-pin LQFP |

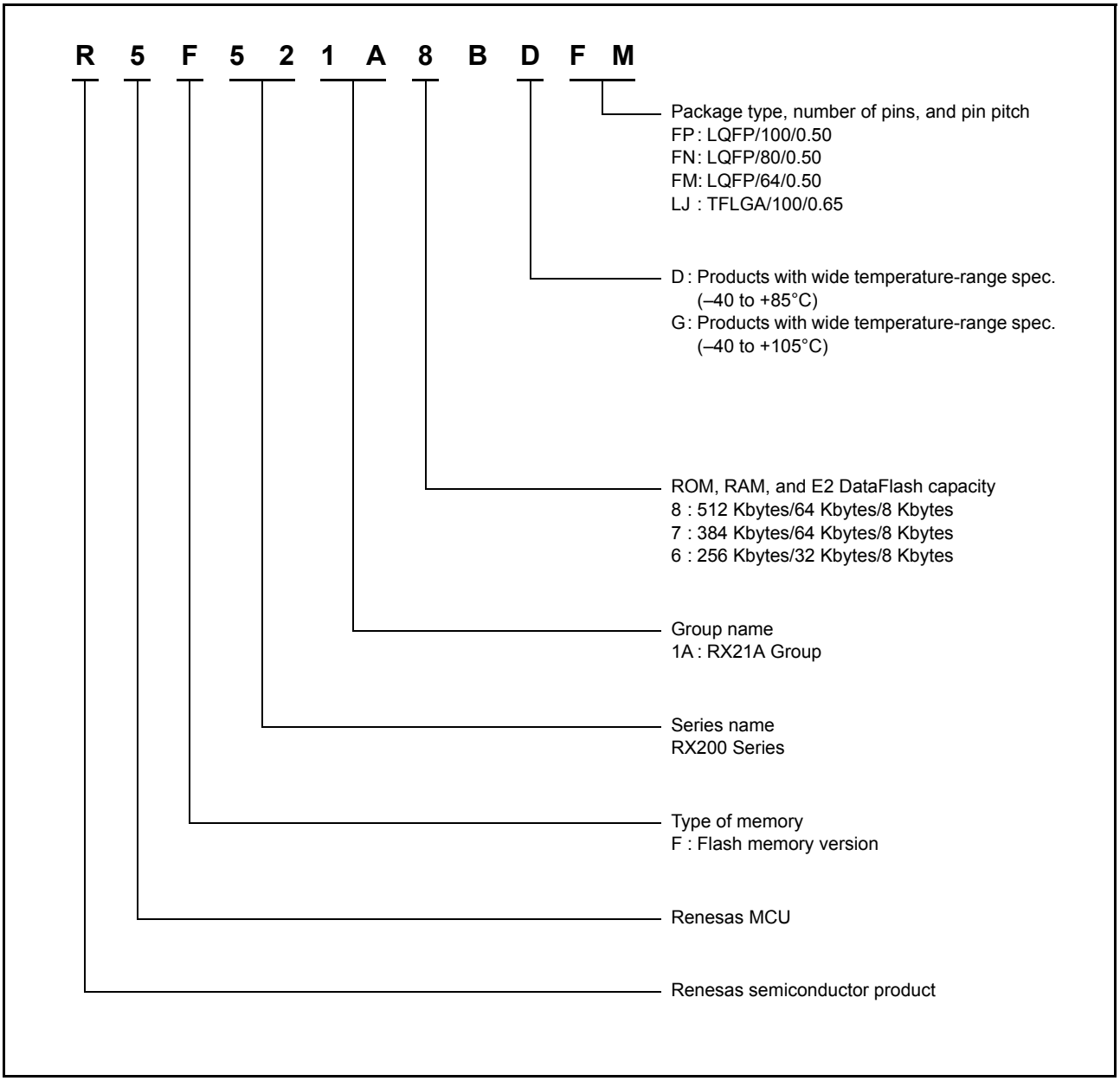
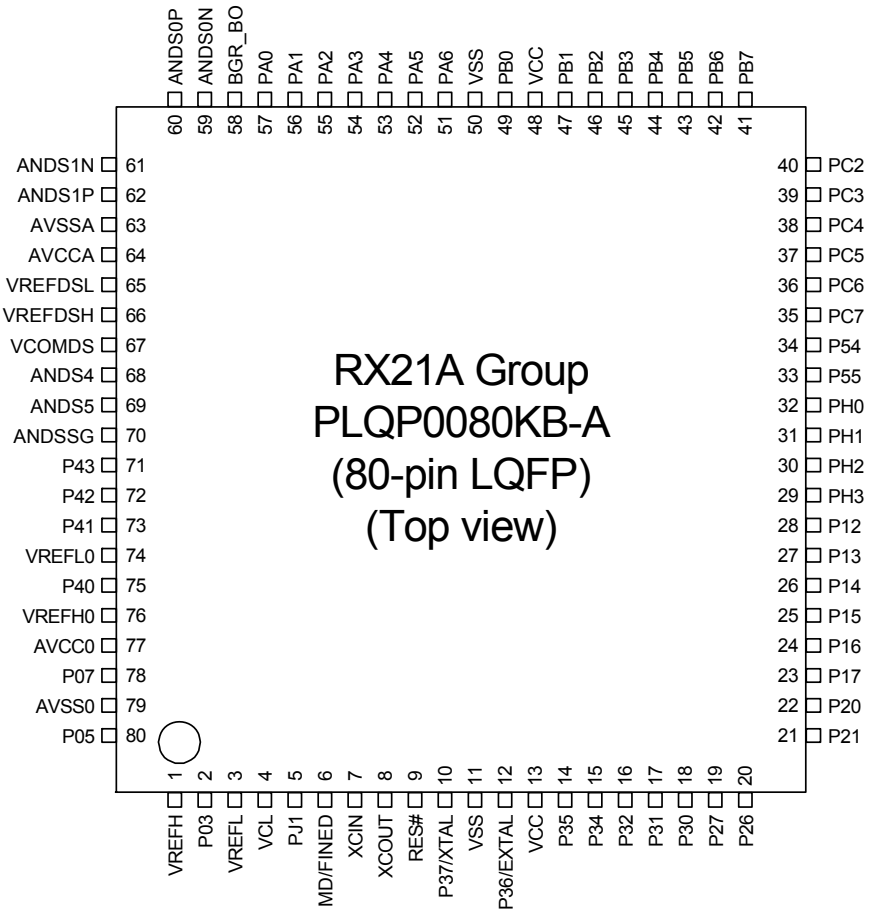



**Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type**




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LQFP)”.

**Figure 1.4 Pin Assignments of the 80-Pin LQFP**

**Table 1.7 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communication (SCIc, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 1 | | P03 | | | AN4 |
| 2 | VCL | | | | |
| 3 | MD | | | | FINED |
| 4 | XCIN | | | | |
| 5 | XCOUT | | | | |
| 6 | RES# | | | | |
| 7 | XTAL | P37 | | | |
| 8 | VSS | | | | |
| 9 | EXTAL | P36 | | | |
| 10 | VCC | | | | |
| 11 | | P35 | | | NMI |
| 12 | | P32 | MTIOC0C/TMO3 | TXD6/SMOSI6/SSDA6 | IRQ2-DS/RTCOUT/ RTCIC2 |
| 13 | | P31 | MTIOC4D/TMCI2 | CTS1#/RTS1#/SS1#/SSLB0 | IRQ1-DS/RTCIC1 |
| 14 | | P30 | MTIOC4B/TMRI3/POE8# | RXD1/SMISO1/SSCL1/ MISOB | IRQ0-DS/RTCIC0 |
| 15 | | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB | |
| 16 | | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1/ MOSIB | |
| 17 | | P17 | MTIOC3A/MTIOC3B/TMO1/ POE8# | SCK1/MISOA/SDA0-DS | IRQ7 |
| 18 | | P16 | MTIOC3C/MTIOC3D/TMO2 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL0-DS | IRQ6/RTCOUT/ ADTRG0# |
| 19 | | P15 | MTIOC0B/MTCLKB/TMCI2 | RXD1/SMISO1/SSCL1 | IRQ5 |
| 20 | | P14 | MTIOC3A/MTCLKA/TMRI2 | CTS1#/RTS1#/SS1# | IRQ4 |
| 21 | | PH3 | TMCI0 | | |
| 22 | | PH2 | TMRI0 | | IRQ1 |
| 23 | | PH1 | TMO0 | | IRQ0 |
| 24 | | PH0 | | | CACREF |
| 25 | | P55 | MTIOC4D/TMO3 | | |
| 26 | | P54 | MTIOC4B/TMCI1 | | |
| 27 | | PC7 | MTIOC3A/TMO2/ MTCLKB | TXD8/SMOSI8/SSDA8/ MISOA | CACREF |
| 28 | | PC6 | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/ MOSIA | |
| 29 | | PC5 | MTIOC3B/MTCLKD/TMRI2 | SCK8/RSPCKA | |
| 30 | | PC4 | MTIOC3D/MTCLKC/TMCI1/ POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0 | |
| 31 | | PC3 | MTIOC4D | TXD5/SMOSI5/SSDA5/ IRTXD5 | |
| 32 | | PC2 | MTIOC4B | RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3 | |
| 33 | | PB7/PC1 | MTIOC3B | TXD9/SMOSI9/SSDA9 | |
| 34 | | PB6/PC0 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| 35 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| 36 | | PB3 | MTIOC0A/MTIOC4A/ TMO0/POE3# | SCK6 | |

**Table 4.1 List of I/O Registers (Address Order) (5 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 70CFh | ICU | Interrupt request register 207 | IR207 | 8 | 8 | | 2 ICLK |
| 0008 70D0h | ICU | Interrupt request register 208 | IR208 | 8 | 8 | | 2 ICLK |
| 0008 70D1h | ICU | Interrupt request register 209 | IR209 | 8 | 8 | | 2 ICLK |
| 0008 70D2h | ICU | Interrupt request register 210 | IR210 | 8 | 8 | | 2 ICLK |
| 0008 70D3h | ICU | Interrupt request register 211 | IR211 | 8 | 8 | | 2 ICLK |
| 0008 70D4h | ICU | Interrupt request register 212 | IR212 | 8 | 8 | | 2 ICLK |
| 0008 70D5h | ICU | Interrupt request register 213 | IR213 | 8 | 8 | | 2 ICLK |
| 0008 70DAh | ICU | Interrupt request register 218 | IR218 | 8 | 8 | | 2 ICLK |
| 0008 70DBh | ICU | Interrupt request register 219 | IR219 | 8 | 8 | | 2 ICLK |
| 0008 70DCh | ICU | Interrupt request register 220 | IR220 | 8 | 8 | | 2 ICLK |
| 0008 70DDh | ICU | Interrupt request register 221 | IR221 | 8 | 8 | | 2 ICLK |
| 0008 70DEh | ICU | Interrupt request register 222 | IR222 | 8 | 8 | | 2 ICLK |
| 0008 70DFh | ICU | Interrupt request register 223 | IR223 | 8 | 8 | | 2 ICLK |
| 0008 70E0h | ICU | Interrupt request register 224 | IR224 | 8 | 8 | | 2 ICLK |
| 0008 70E1h | ICU | Interrupt request register 225 | IR225 | 8 | 8 | | 2 ICLK |
| 0008 70E2h | ICU | Interrupt request register 226 | IR226 | 8 | 8 | | 2 ICLK |
| 0008 70E3h | ICU | Interrupt request register 227 | IR227 | 8 | 8 | | 2 ICLK |
| 0008 70E4h | ICU | Interrupt request register 228 | IR228 | 8 | 8 | | 2 ICLK |
| 0008 70E5h | ICU | Interrupt request register 229 | IR229 | 8 | 8 | | 2 ICLK |
| 0008 70E6h | ICU | Interrupt request register 230 | IR230 | 8 | 8 | | 2 ICLK |
| 0008 70E7h | ICU | Interrupt request register 231 | IR231 | 8 | 8 | | 2 ICLK |
| 0008 70E8h | ICU | Interrupt request register 232 | IR232 | 8 | 8 | | 2 ICLK |
| 0008 70E9h | ICU | Interrupt request register 233 | IR233 | 8 | 8 | | 2 ICLK |
| 0008 70EAh | ICU | Interrupt request register 234 | IR234 | 8 | 8 | | 2 ICLK |
| 0008 70EBh | ICU | Interrupt request register 235 | IR235 | 8 | 8 | | 2 ICLK |
| 0008 70ECh | ICU | Interrupt request register 236 | IR236 | 8 | 8 | | 2 ICLK |
| 0008 70EDh | ICU | Interrupt request register 237 | IR237 | 8 | 8 | | 2 ICLK |
| 0008 70F6h | ICU | Interrupt request register 246 | IR246 | 8 | 8 | | 2 ICLK |
| 0008 70F7h | ICU | Interrupt request register 247 | IR247 | 8 | 8 | | 2 ICLK |
| 0008 70F8h | ICU | Interrupt request register 248 | IR248 | 8 | 8 | | 2 ICLK |
| 0008 70F9h | ICU | Interrupt request register 249 | IR249 | 8 | 8 | | 2 ICLK |
| 0008 70FAh | ICU | Interrupt request register 250 | IR250 | 8 | 8 | | 2 ICLK |
| 0008 70FBh | ICU | Interrupt request register 251 | IR251 | 8 | 8 | | 2 ICLK |
| 0008 70FCh | ICU | Interrupt request register 252 | IR252 | 8 | 8 | | 2 ICLK |
| 0008 70FDh | ICU | Interrupt request register 253 | IR253 | 8 | 8 | | 2 ICLK |
| 0008 711Bh | ICU | DTC activation enable register 027 | DTCER027 | 8 | 8 | | 2 ICLK |
| 0008 711Ch | ICU | DTC activation enable register 028 | DTCER028 | 8 | 8 | | 2 ICLK |
| 0008 711Dh | ICU | DTC activation enable register 029 | DTCER029 | 8 | 8 | | 2 ICLK |
| 0008 711Eh | ICU | DTC activation enable register 030 | DTCER030 | 8 | 8 | | 2 ICLK |
| 0008 711Fh | ICU | DTC activation enable register 031 | DTCER031 | 8 | 8 | | 2 ICLK |
| 0008 712Dh | ICU | DTC activation enable register 045 | DTCER045 | 8 | 8 | | 2 ICLK |
| 0008 712Eh | ICU | DTC activation enable register 046 | DTCER046 | 8 | 8 | | 2 ICLK |
| 0008 7131h | ICU | DTC activation enable register 049 | DTCER049 | 8 | 8 | | 2 ICLK |
| 0008 7132h | ICU | DTC activation enable register 050 | DTCER050 | 8 | 8 | | 2 ICLK |
| 0008 713Ah | ICU | DTC activation enable register 058 | DTCER058 | 8 | 8 | | 2 ICLK |
| 0008 713Bh | ICU | DTC activation enable register 059 | DTCER059 | 8 | 8 | | 2 ICLK |
| 0008 7140h | ICU | DTC activation enable register 064 | DTCER064 | 8 | 8 | | 2 ICLK |
| 0008 7141h | ICU | DTC activation enable register 065 | DTCER065 | 8 | 8 | | 2 ICLK |
| 0008 7142h | ICU | DTC activation enable register 066 | DTCER066 | 8 | 8 | | 2 ICLK |
| 0008 7143h | ICU | DTC activation enable register 067 | DTCER067 | 8 | 8 | | 2 ICLK |
| 0008 7144h | ICU | DTC activation enable register 068 | DTCER068 | 8 | 8 | | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (9 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 73E2h | ICU | Interrupt source priority register 226 | IPR226 | 8 | 8 | | 2 ICLK |
| 0008 73E6h | ICU | Interrupt source priority register 230 | IPR230 | 8 | 8 | | 2 ICLK |
| 0008 73EAh | ICU | Interrupt source priority register 234 | IPR234 | 8 | 8 | | 2 ICLK |
| 0008 73F6h | ICU | Interrupt source priority register 246 | IPR246 | 8 | 8 | | 2 ICLK |
| 0008 73F7h | ICU | Interrupt source priority register 247 | IPR247 | 8 | 8 | | 2 ICLK |
| 0008 73F8h | ICU | Interrupt source priority register 248 | IPR248 | 8 | 8 | | 2 ICLK |
| 0008 73F9h | ICU | Interrupt source priority register 249 | IPR249 | 8 | 8 | | 2 ICLK |
| 0008 73FAh | ICU | Interrupt source priority register 250 | IPR250 | 8 | 8 | | 2 ICLK |
| 0008 73FBh | ICU | Interrupt source priority register 251 | IPR251 | 8 | 8 | | 2 ICLK |
| 0008 73FCh | ICU | Interrupt source priority register 252 | IPR252 | 8 | 8 | | 2 ICLK |
| 0008 73FDh | ICU | Interrupt source priority register 253 | IPR253 | 8 | 8 | | 2 ICLK |
| 0008 7400h | ICU | DMAC activation request select register 0 | DMRSR0 | 8 | 8 | | 2 ICLK |
| 0008 7404h | ICU | DMAC activation request select register 1 | DMRSR1 | 8 | 8 | | 2 ICLK |
| 0008 7408h | ICU | DMAC activation request select register 2 | DMRSR2 | 8 | 8 | | 2 ICLK |
| 0008 740Ch | ICU | DMAC activation request select register 3 | DMRSR3 | 8 | 8 | | 2 ICLK |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | | 2 ICLK |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | | 2 ICLK |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | | 2 ICLK |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | | 2 ICLK |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | | 2 ICLK |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | | 2 ICLK |
| 0008 7510h | ICU | IRQ pin digital filter enable register 0 | IRQFLTE0 | 8 | 8 | | 2 ICLK |
| 0008 7514h | ICU | IRQ pin digital filter setting register 0 | IRQFLTC0 | 16 | 16 | | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | | 2 ICLK |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | | 2 ICLK |
| 0008 7590h | ICU | NMI pin digital filter enable register | NMIFLTE | 8 | 8 | | 2 ICLK |
| 0008 7594h | ICU | NMI pin digital filter setting register | NMIFLTC | 8 | 8 | | 2 ICLK |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8020h | WDT | WDT refresh register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8022h | WDT | WDT control register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8024h | WDT | WDT status register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8026h | WDT | WDT reset control register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (11 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 830Dh | RIIC0 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Eh | RIIC0 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Fh | RIIC0 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8310h | RIIC0 | I2C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8311h | RIIC0 | I2C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8312h | RIIC0 | I2C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8313h | RIIC0 | I2C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8320h | RIIC1 | I2C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8321h | RIIC1 | I2C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8322h | RIIC1 | I2C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8323h | RIIC1 | I2C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8324h | RIIC1 | I2C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8325h | RIIC1 | I2C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8326h | RIIC1 | I2C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8327h | RIIC1 | I2C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8328h | RIIC1 | I2C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8329h | RIIC1 | I2C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Ah | RIIC1 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Ah | RIIC1 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Bh | RIIC1 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Bh | RIIC1 | Timeout internal counter U | TMOCNTU | 8 | 8*2 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Ch | RIIC1 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Dh | RIIC1 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Eh | RIIC1 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 832Fh | RIIC1 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8330h | RIIC1 | I2C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8331h | RIIC1 | I2C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8332h | RIIC1 | I2C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8333h | RIIC1 | I2C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8380h | RSPI0 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8381h | RSPI0 | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8382h | RSPI0 | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8383h | RSPI0 | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8384h | RSPI0 | RSPI data register | SPDR | 32 | 16, 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 8388h | RSPI0 | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8389h | RSPI0 | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Ah | RSPI0 | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Bh | RSPI0 | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Ch | RSPI0 | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Dh | RSPI0 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Eh | RSPI0 | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 838Fh | RSPI0 | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8390h | RSPI0 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8392h | RSPI0 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8394h | RSPI0 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8396h | RSPI0 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8398h | RSPI0 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Ah | RSPI0 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Ch | RSPI0 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 839Eh | RSPI0 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 83A0h | RSPI1 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (13 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 8630h | MTU | Timer interrupt skipping set register | TITCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8631h | MTU | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8632h | MTU | Timer buffer transfer set register | TBTER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8634h | MTU | Timer dead time enable register | TDER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8636h | MTU | Timer output level buffer register | TOLBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8638h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8639h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8640h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8644h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8646h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8648h | MTU4 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 864Ah | MTU4 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8660h | MTU | Timer waveform control register | TWCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8680h | MTU | Timer start register | TSTR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8681h | MTU | Timer synchronous register | TSYR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8684h | MTU | Timer read/write enable register | TRWER | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8690h | MTU0 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8691h | MTU1 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8692h | MTU2 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8693h | MTU3 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8694h | MTU4 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8695h | MTU5 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8700h | MTU0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8701h | MTU0 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8702h | MTU0 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8703h | MTU0 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8704h | MTU0 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8705h | MTU0 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8706h | MTU0 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8708h | MTU0 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 870Ah | MTU0 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 870Ch | MTU0 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 870Eh | MTU0 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8720h | MTU0 | Timer general register E | TGRE | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8722h | MTU0 | Timer general register F | TGRF | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8724h | MTU0 | Timer interrupt enable register 2 | TIER2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8726h | MTU0 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8780h | MTU1 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8781h | MTU1 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8782h | MTU1 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8784h | MTU1 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8785h | MTU1 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8786h | MTU1 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8788h | MTU1 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 878Ah | MTU1 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8790h | MTU1 | Timer input capture control register | TICCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8800h | MTU2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8801h | MTU2 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8802h | MTU2 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8804h | MTU2 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8805h | MTU2 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (14 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 8806h | MTU2 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8808h | MTU2 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 880Ah | MTU2 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8880h | MTU5 | Timer counter U | TCNTU | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8882h | MTU5 | Timer general register U | TGRU | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8884h | MTU5 | Timer control register U | TCRU | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8886h | MTU5 | Timer I/O control register U | TIORU | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8890h | MTU5 | Timer counter V | TCNTV | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8892h | MTU5 | Timer general register V | TGRV | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8894h | MTU5 | Timer control register V | TCRV | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8896h | MTU5 | Timer I/O control register V | TIORV | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 88A0h | MTU5 | Timer counter W | TCNTW | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 88A2h | MTU5 | Timer general register W | TGRW | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 88A4h | MTU5 | Timer control register W | TCRW | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 88A6h | MTU5 | Timer I/O control register W | TIORW | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 88B2h | MTU5 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 88B4h | MTU5 | Timer start register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 88B6h | MTU5 | Timer compare match clear register | TCNTCMPCLR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8900h | POE | Input level control/status register 1 | ICSR1 | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8902h | POE | Output level control/status register 1 | OCSR1 | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8908h | POE | Input level control/status register 2 | ICSR2 | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 890Ah | POE | Software port output enable register | SPOER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 890Bh | POE | Port output enable control register 1 | POECR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 890Ch | POE | Port output enable control register 2 | POECR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 890Eh | POE | Input level control/status register 3 | ICSR3 | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9800h | AD | A/D control register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9804h | AD | A/D channel select register A | ADANSA | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9808h | AD | A/D-converted value addition mode select register | ADADS | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 980Ch | AD | A/D-converted value addition count select register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 980Eh | AD | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9810h | AD | A/D start trigger select register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9812h | AD | A/D-converted extended input control register | ADEXICR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 981Ah | AD | A/D temperature sensor data register | ADTSDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 981Ch | AD | A/D internal reference voltage data register | ADOCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 981Eh | AD | A/D self-diagnosis data register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9820h | AD | A/D data register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9822h | AD | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9824h | AD | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9826h | AD | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9828h | AD | A/D data register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 982Ah | AD | A/D data register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 982Ch | AD | A/D data register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 9860h | AD | A/D sampling state register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9870h | AD | A/D sampling state register T | ADSSTRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9871h | AD | A/D sampling state register O | ADSSTRO | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9873h | AD | A/D sampling state register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9874h | AD | A/D sampling state register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9875h | AD | A/D sampling state register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9876h | AD | A/D sampling state register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9877h | AD | A/D sampling state register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 9878h | AD | A/D sampling state register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (20 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 C0C0h | PORT0 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0C1h | PORT1 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0C2h | PORT2 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0C3h | PORT3 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0C4h | PORT4 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0C5h | PORT5 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0CAh | PORTA | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0CBh | PORTB | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0CCh | PORTC | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0CEh | PORTE | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0D1h | PORTH | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0D2h | PORTJ | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0E1h | PORT1 | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0E2h | PORT2 | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0E3h | PORT3 | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0E5h | PORT5 | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0EAh | PORTA | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0EBh | PORTB | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0ECh | PORTC | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0EEh | PORTE | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0F1h | PORTH | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C0F2h | PORTJ | Drive capacity control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C11Fh | MPC | Write-protect register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C121h | PORT | Port switching register A | PSRA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C143h | MPC | P03 pin function control register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C145h | MPC | P05 pin function control register | P05PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C147h | MPC | P07 pin function control register | P07PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Ah | MPC | P12 pin function control register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Bh | MPC | P13 pin function control register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Ch | MPC | P14 pin function control register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Dh | MPC | P15 pin function control register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Eh | MPC | P16 pin function control register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C14Fh | MPC | P17 pin function control register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C150h | MPC | P20 pin function control register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C151h | MPC | P21 pin function control register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C152h | MPC | P22 pin function control register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C153h | MPC | P23 pin function control register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C154h | MPC | P24 pin function control register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C155h | MPC | P25 pin function control register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C156h | MPC | P26 pin function control register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C157h | MPC | P27 pin function control register | P27PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C158h | MPC | P30 pin function control register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C159h | MPC | P31 pin function control register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C15Ah | MPC | P32 pin function control register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C15Bh | MPC | P33 pin function control register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C15Ch | MPC | P34 pin function control register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C160h | MPC | P40 pin function control register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C161h | MPC | P41 pin function control register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C162h | MPC | P42 pin function control register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C163h | MPC | P43 pin function control register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C168h | MPC | P50 pin function control register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 5.8 DC Characteristics (7)**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | | | Symbol | Typ.*3 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Software standby mode*2 | Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b) | $T_a$ = 25°C | $I_{CC}$ | 10 | 20 | µA | |
| | | | $T_a$ = 55°C | | 12 | 41 | | |
| | | | $T_a$ = 85°C | | 18 | 113 | | |
| | | | $T_a$ = 105°C | | 29 | 233 | | |
| | | Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b) | $T_a$ = 25°C | | 1.7 | 7.9 | | |
| | | | $T_a$ = 55°C | | 2.7 | 25 | | |
| | | | $T_a$ = 85°C | | 7.0 | 86 | | |
| | | | $T_a$ = 105°C | | 16 | 189 | | |
| | Deep software standby mode*2 | Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled | $T_a$ = 25°C | | 0.3 | 0.8 | | |
| | | | $T_a$ = 55°C | | 0.4 | 1.1 | | |
| | | | $T_a$ = 85°C | | 0.8 | 2.2 | | |
| | | | $T_a$ = 105°C | | 1.3 | 4.7 | | |
| | Increments produced by running voltage detection circuits and disabling the POR low power consumption function | | | | 1.2 | — | | |
| | Increment for RTC operation (low CL) | | | | 0.6 | — | | |
| | Increment for RTC operation (standard CL) | | | | 1.4 | — | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

**Table 5.17 Output Values of Voltage (1)**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 2.7 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output mode | $V_{OL}$ | — | 0.4 | V | $I_{OL}$ = 0.5 mA |
| | | High-drive output mode | | — | 0.4 | | $I_{OL}$ = 1.0 mA |
| Output high | All output pins | Normal output mode | $V_{OH}$ | VCC – 0.4 | — | V | $I_{OL}$ = –0.5 mA |
| | | High-drive output mode | | VCC – 0.4 | — | | $I_{OL}$ = –1.0 mA |

**Table 5.18 Output Values of Voltage (2)**

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL =0 V,
$T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output mode | $V_{OL}$ | — | 1.0 | V | $I_{OL}$ = 3.0 mA |
| | | High-drive output mode | | — | 1.0 | | $I_{OL}$ = 5.0 mA |
| | RIIC pins | | | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| Output high | All output pins | Normal output mode | $V_{OH}$ | VCC – 1.0 | — | V | $I_{OL}$ = –3.0 mA |
| | | High-drive output mode | | VCC – 1.0 | — | | $I_{OL}$ = –5.0 mA |

### 5.2.3 RIIC Pin Output Characteristics

Figure 5.21 to Figure 5.24 show the output characteristics of the RIIC pin.

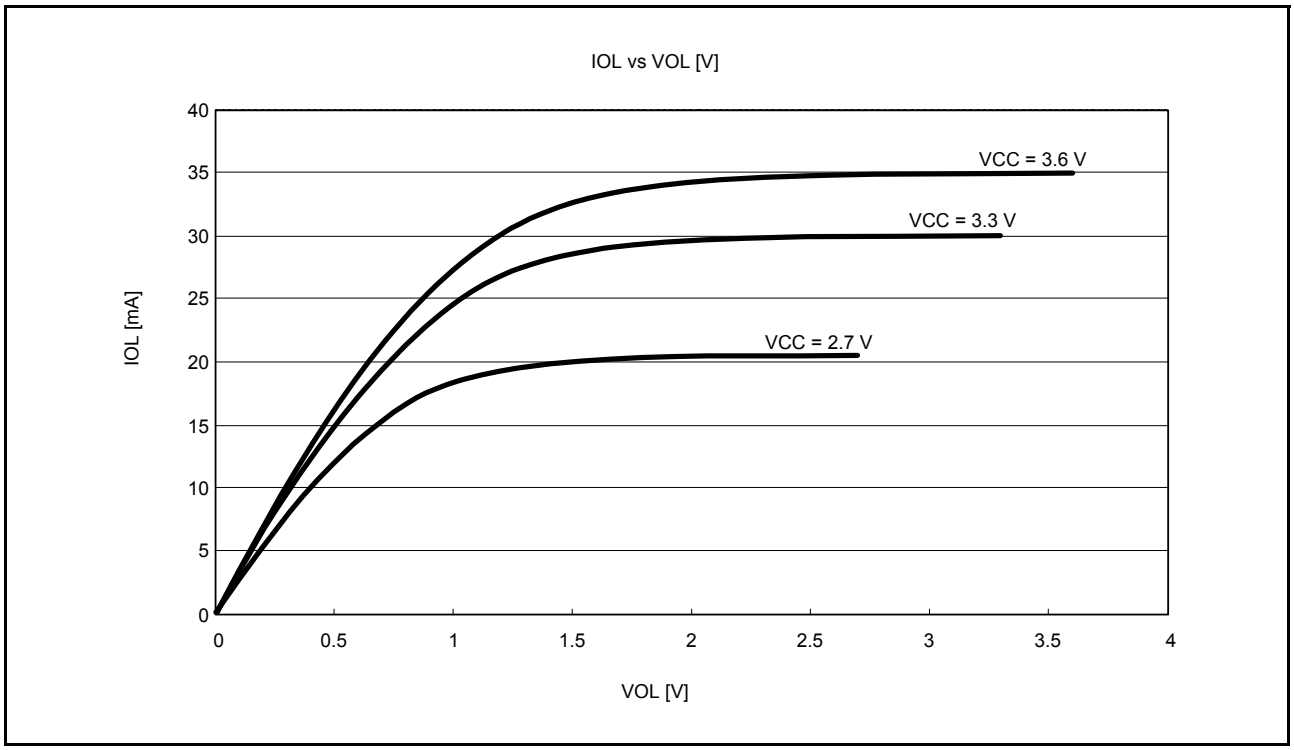



**Figure 5.21 VOH and IOL Voltage Characteristics of RIIC Output Pin at Ta = 25°C (Reference Data)**

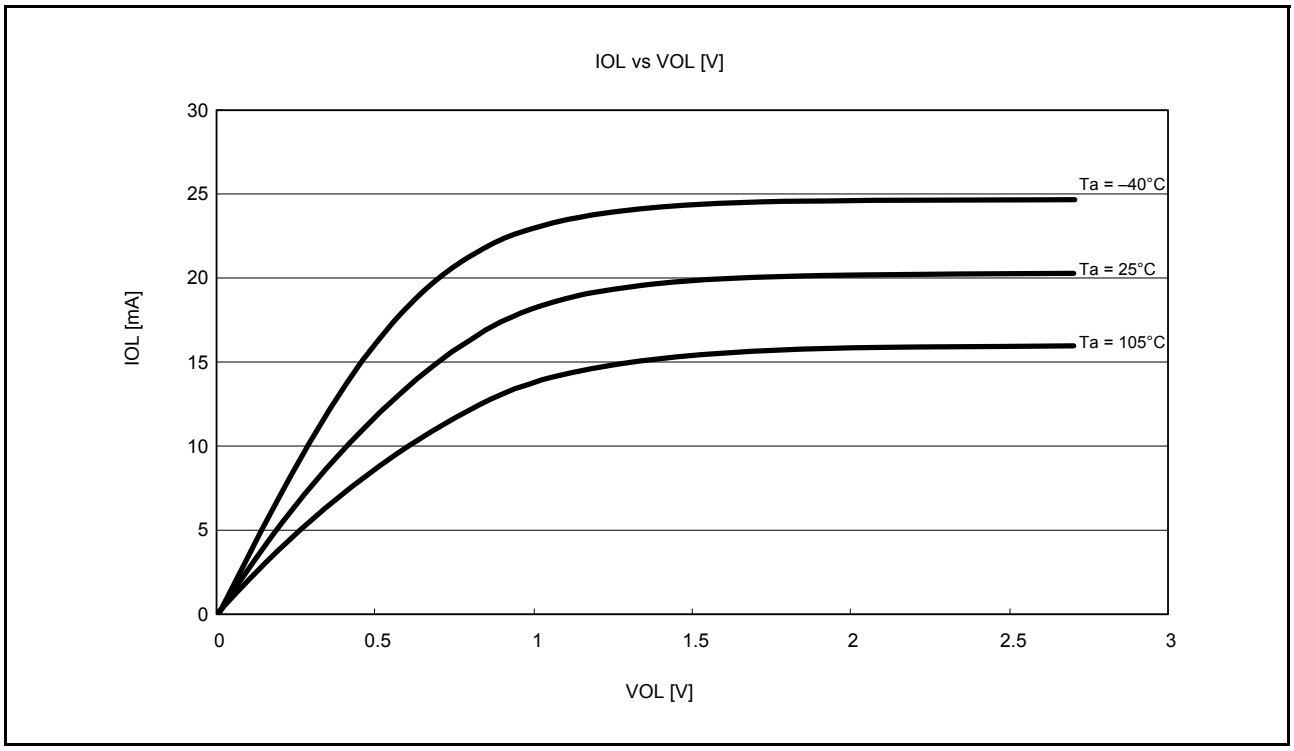



**Figure 5.22 VOH and IOL Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)**

## 5.4.2 Timing of Recovery from Low Power Consumption Modes

**Table 5.28 Timing of Recovery from Low Power Consumption Modes**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1 | Crystal resonator connected to main clock oscillator*2 | Main clock oscillator operating | $t_{SBYMC}$ | — | 3 | — | ms | Figure 5.37 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | — | 3.5 | — | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | 10 | — | — | µs | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | 0.5 | — | — | ms | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | 2*3 | — | — | s | |
| | HOCO clock oscillator operating | | $t_{SBYHO}$ | — | — | 500 | µs | |
| | LOCO clock oscillator operating | | $t_{SBYLO}$ | — | — | 90 | µs | |
| Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1 | Crystal resonator connected to main clock oscillator*2 | Main clock oscillator operating | $t_{SBYMC}$ | — | 3 | — | ms | Figure 5.37 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | — | 3.5 | — | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | 40 | — | — | µs | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | 0.5 | — | — | ms | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | 2*3 | — | — | s | |
| | HOCO clock oscillator operating | | $t_{SBYHO}$ | — | — | 1.2 | ms | |
| | LOCO clock oscillator operating | | $t_{SBYLO}$ | — | — | 90 | µs | |
| Recovery time after cancellation of deep software standby mode | | | $t_{DSBY}$ | — | — | 8 | ms | Figure 5.38 |
| Wait time after cancellation of deep software standby mode | | | $t_{DSBYWT}$ | — | — | 0.8 | ms | |

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.

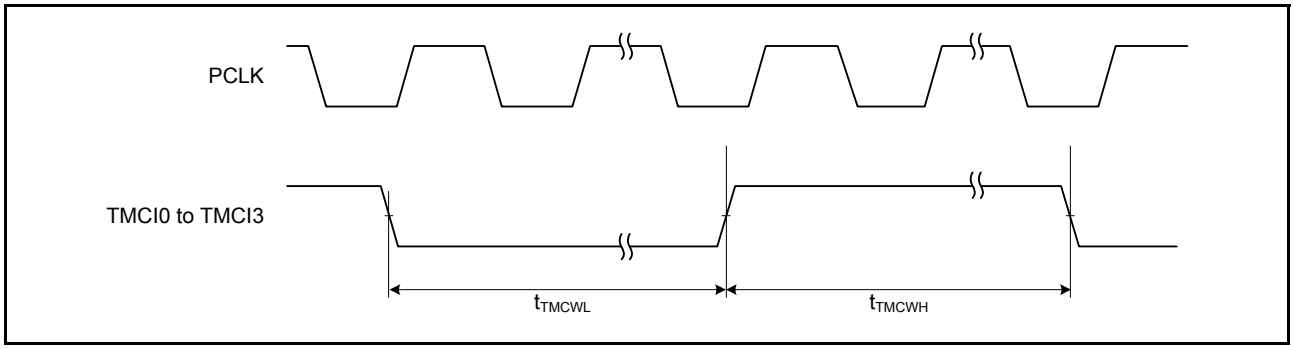



**Figure 5.45 8-Bit Timer Clock Input Timing**

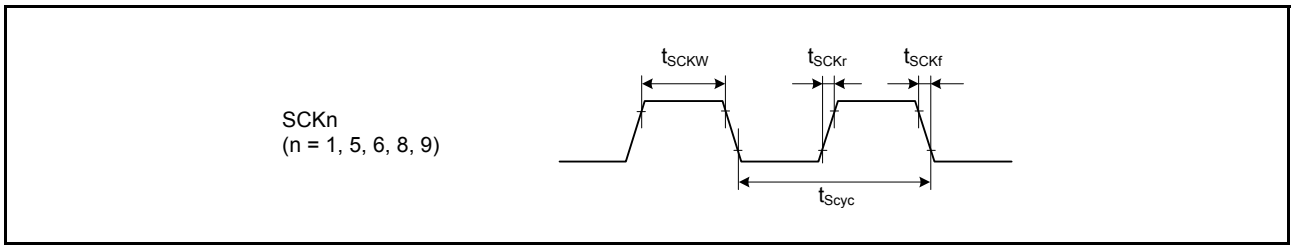



**Figure 5.46 SCK Clock Input Timing**

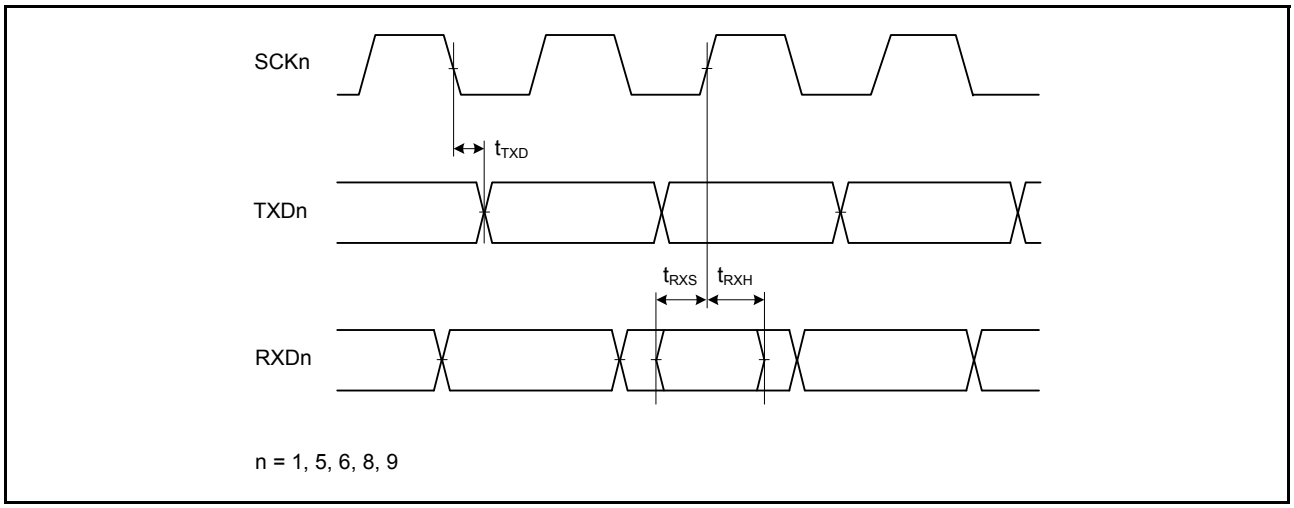



**Figure 5.47 SCI Input/Output Timing: Clock Synchronous Mode**

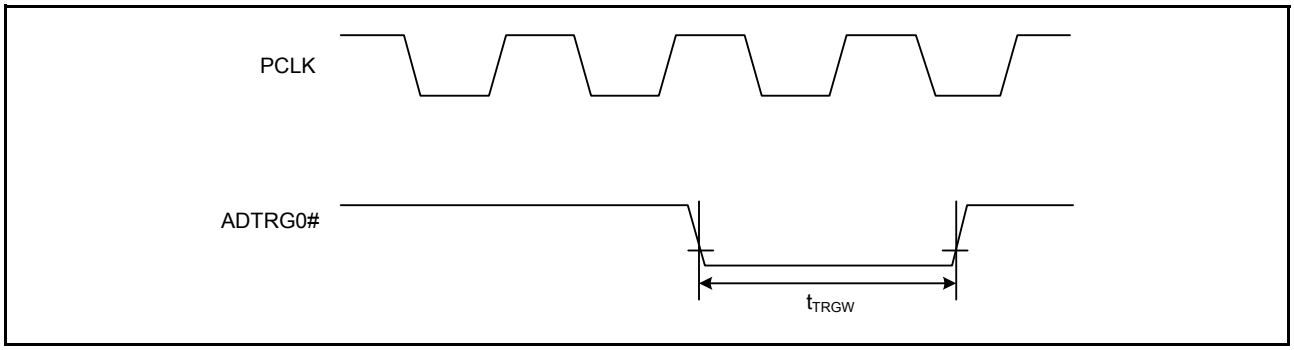



**Figure 5.48 A/D Converter External Trigger Input Timing**

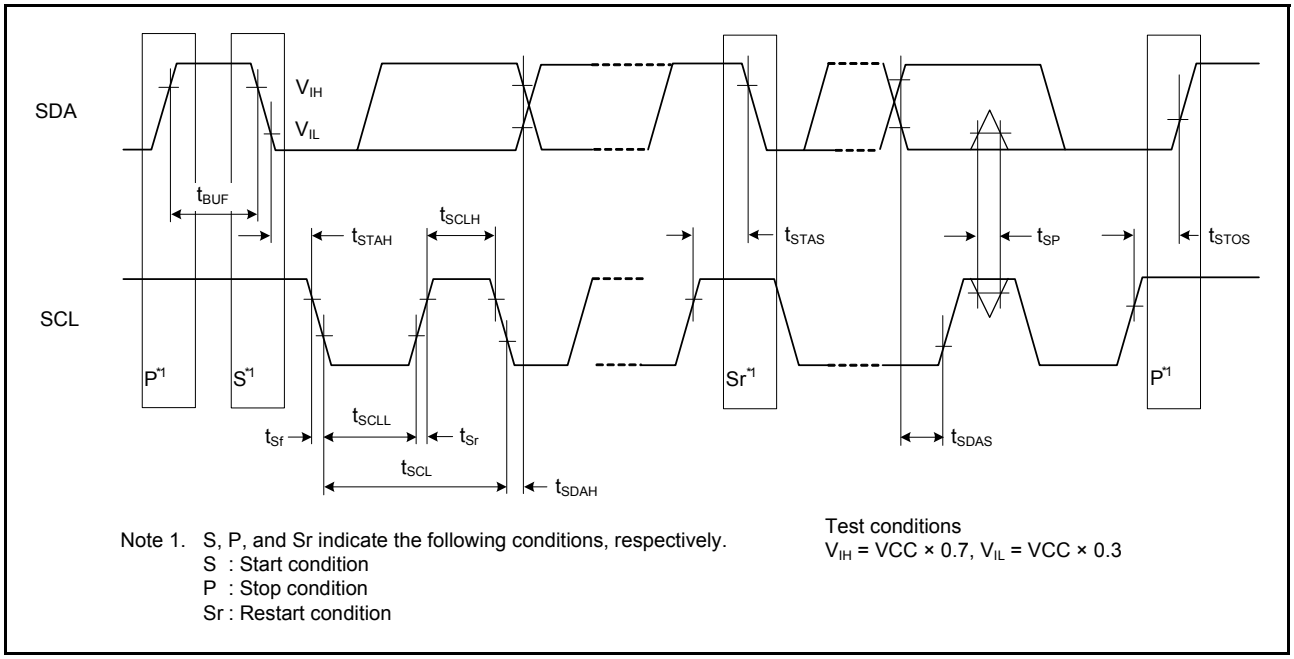
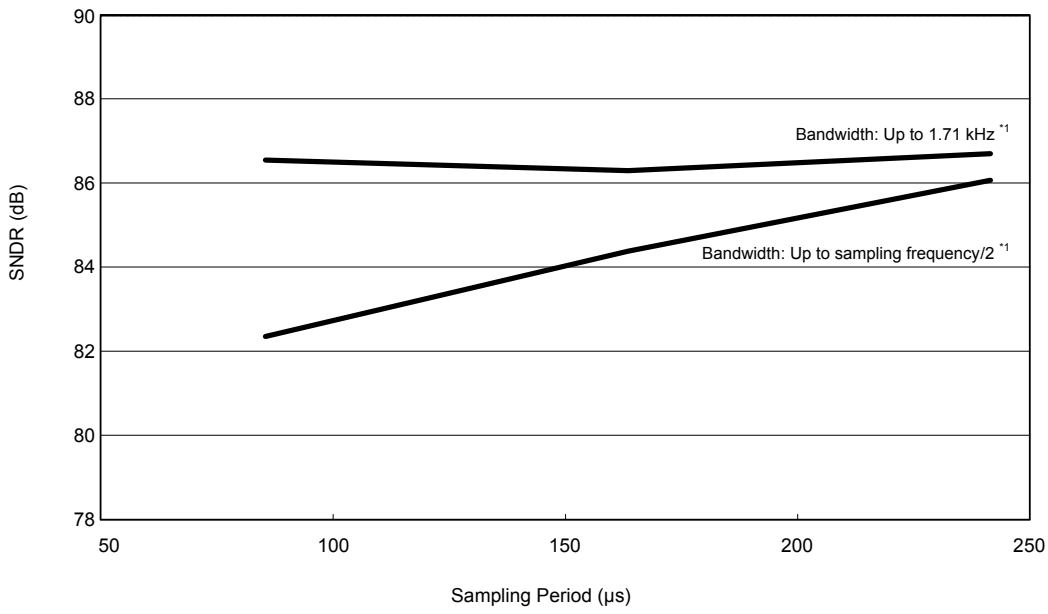
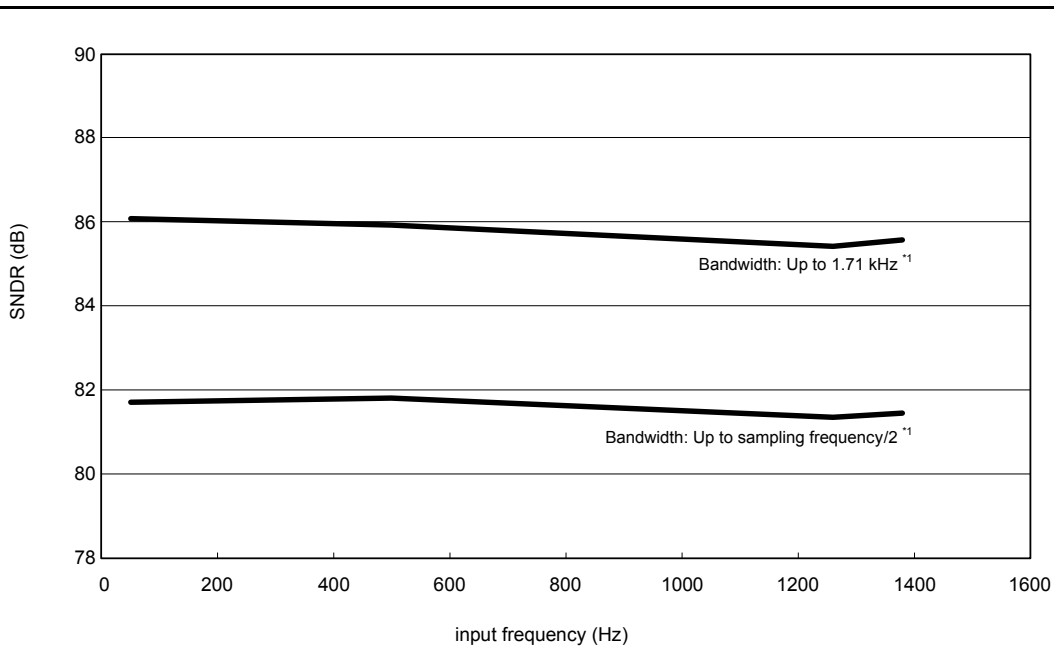



**Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing**




Note 1. Gain: ×1, input frequency: 50 Hz, input amplitude: 500 mV

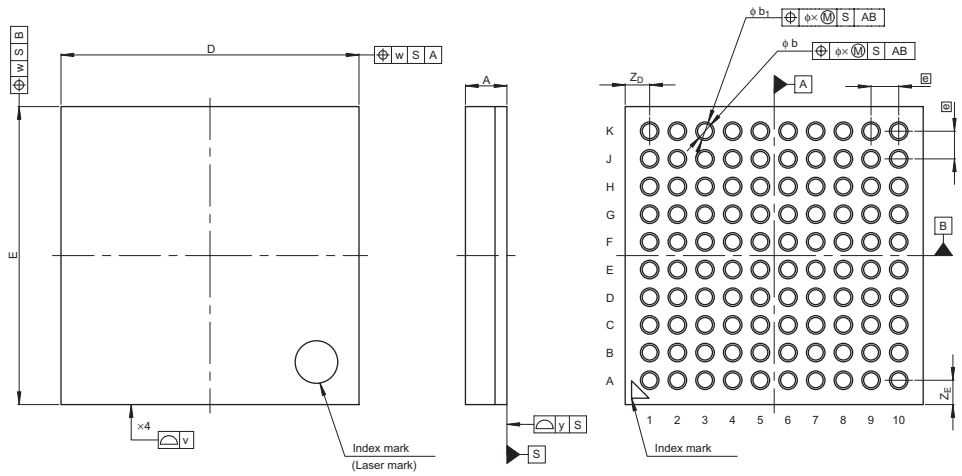
**Figure 5.58 Sampling Period Dependency of SNDR (Reference Data)**




Note 1. Gain: ×1, sampling period: 81.92 µs, input amplitude: 500 mV

**Figure 5.59 Input Frequency Dependency of SNDR (Reference Data)**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

Figure D 100-Pin TFLGA (PTLG0100JA-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.10 | 2014.08.28 | Features | | |
| | | 1 | LGA package, added | TN-RX*-A072A/E |
| | | 1. Overview | | |
| | | 5 | Table 1.1 Outline of Specifications: Package added | TN-RX*-A072A/E |
| | | 5 | Table 1.1 Outline of Specifications: Note 2 added | TN-RX*-A073A/E |
| | | 5 | Table 1.1 Outline of Specifications: Note 3 added | |
| | | 5 | Table 1.2 Comparison of Functions for Different Packages, changed | TN-RX*-A072A/E |
| | | 6 | Table 1.3 List of Products, changed | TN-RX*-A072A/E |
| | | 6 | Table 1.3 List of Products: Note 1 added | TN-RX*-A072A/E |
| | | 6 | Table 1.3 List of Products: Note, Note 2 added | |
| | | 7 | Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed | TN-RX*-A072A/E |
| | | 9 | Table 1.4 Pin Functions: Realtime clock changed | |
| | | 15 | Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View), added | TN-RX*-A072A/E |
| | | 23 to 25 | Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA), added | TN-RX*-A072A/E |
| | | 3. Address Space | | |
| | | 29 | Figure 3.1 Memory Map, changed | |
| | | 4. I/O Registers | | |
| | | 54 to 55 | Table 4.1 List of I/O Registers (Address Order): FEFF FAC0h to FEFF FBD3h added | |
| | | 5. Electrical Characteristics | | |
| | | 57 | Table 5.3 DC Characteristics (2) | TN-RX*-A074A/E |
| | | 58 | Table 5.4 DC Characteristics (3), changed | TN-RX*-A074A/E |
| | | 59 | Table 5.6 DC Characteristics (5), changed | TN-RX*-A074A/E |
| | | 60 | Table 5.7 DC Characteristics (6), changed | TN-RX*-A074A/E |
| | | 68 | Table 5.9 DC Characteristics (8), added | TN-RX*-A074A/E |
| | | 68 | Table 5.10 DC Characteristics (9), changed | |
| | | 68 | Table 5.11 DC Characteristics (10), changed | |
| | | 69 | Table 5.14 DC Characteristics (13), changed | TN-RX*-A074A/E |
| | | 69 | Table 5.15 Permissible Output Currents (1), changed<br>Table 5.16 Permissible Output Currents (2), added | TN-RX*-A074A/E |
| | | 70 | Table 5.18 Output Values of Voltage (2), changed | TN-RX*-A074A/E |
| | | 82 | Table 5.26 Clock Timing, changed | TN-RX*-A097A/E |
| | | 83 | Table 5.26 Clock Timing: Note 5 changed | TN-RX*-A105A/E |
| | | 83 | Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing, changed | TN-RX*-A097A/E |
| | | 87 | Figure 5.35 Reset Input Timing at Power-On, changed | TN-RX*-A074A/E |
| | | 94 | Table 5.33 Timing of On-Chip Peripheral Modules (4), changed | TN-RX*-A074A/E |
| | | 103 | Table 5.36 ΔΣ A/D Conversion Characteristics, changed | TN-RX*-A105A/E |
| | | 104 | Figure 5.55 Differential Input Amplitude, changed | |
| | | 108 | Table 5.37 A/D Conversion Characteristics (1), changed | TN-RX*-A074A/E |
| | | 108 | Figure 5.61 AVCC to VREFH0 Voltage Range, added | TN-RX*-A074A/E |
| | | 109 | Table 5.39 A/D Conversion Characteristics (2), changed | TN-RX*-A074A/E |
| | | 111 | Differential nonlinearity error (DNL), description changed | TN-RX*-A073A/E |
| | | 115 | Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1): Note1, Note2 changed | TN-RX*-A074A/E |
| | | Appendix 1. Package Dimensions | | |
| | | 128 | Figure D. 100-Pin TFLGA (PTLG0100JA-A), added | TN-RX*-A072A/E |