Renesas Electronics America Inc - R5F521A8BDFN#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a8bdfn-30

Table 1.1 Outline of Specifications (3 / 4)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (SCIc)	• 5 channels (channel 1, 5, 6, 8, 9) (including one channel for IrDA) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Average transfer rate clock can be input from TMR timers (SCI5 and SCI6) • Simple IIC • Simple SPI
	IrDA interface (IRDA)	• 1 channel (SCI5 is used) • Supports encoding/decoding the waveforms conforming to the IrDA specification version 1.0
	I^2C bus interface (RIIC)	• 2 channels • Communications formats: I^2C bus format/SMBus format • Master/slave selectable • Supports the fast mode
	Serial peripheral interface (RSPI)	• 2 channels • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
24-bit ΔΣ A/D converter (DSAD)		• 7 channels: 4-channel differential input for current; 3-channel single-ended input for voltage • x 1 to x 64 PGA for differential input side for current and x 1 to x 4 PGA for single-ended input side for voltage • Minimum conversion time: 81.92 µs (A/D conversion clock: 25 MHz)
10-bit A/D converter (AD)		• 10 bits (7 channels x 1 unit) • 10-bit resolution • Conversion time: 2.0 µs per channel (A/D conversion clock: 25 MHz) • Operating modes Scan mode (single scan mode and continuous scan mode) • Sample-and-hold function • Self-diagnosis for the A/D converter • Assistance in detecting disconnected analog inputs • A/D conversion start conditions Conversion can be started by software, a conversion start trigger from a timer (MTU), an external trigger signal, a temperature sensor or ELC.
Temperature sensor (TEMPSa)		• Outputs the voltage that changes depending on the temperature • PGA gain switchable: Three levels according to the voltage range
D/A converter (DA)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Data encryption unit (DEU)*1		• Encryption and decryption of AES • 128-, 192-, or 256-bit key length • ECB or CBC mode
Comparator A (CMPA)		• 2 channels • Comparison of reference voltage and analog input voltage
Comparator B (CMPB)		• 2 channels • Comparison of reference voltage and analog input voltage
Data operating circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltage/ Operating frequency		VCC = 1.8 to 3.6 V: 25 MHz, VCC = 2.7 to 3.6 V: 50 MHz
Supply current		8.6mA@50MHz (typ)
Operating temperature		D version: –40 to +85°C, G version: –40 to +105°C*2, *3

Table 1.4 Pin Functions (3 / 3)

Classifications	Pin Name	I/O	Description
Comparator A	CMPA1	Input	Input pin for the comparator A1 analog signals.
	CMPA2	Input	Input pin for the comparator A2 analog signals.
	CVREFA	Input	Input pin for the comparator reference voltage.
Comparator B	CMPB0	Input	Input pin for the comparator B0 analog signals.
	CVREFB0	Input	Input pin for the comparator B0 reference voltage.
	CMPB1	Input	Input pin for the comparator B1 analog signals.
	CVREFB1	Input	Input pin for the comparator B1 reference voltage.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH0	Input	Reference voltage supply pin for the 10-bit A/D converter. Connect this pin to VCC if the 10-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 10-bit A/D converter. Connect this pin to VSS if the 10-bit A/D converter is not to be used.
	VREFH	Input	Analog voltage supply pin for the D/A converter. Connect this pin to VCC if the D/A converter is not to be used.
	VREFL	Input	Analog ground pin for the D/A converter. Connect this pin to VSS if the D/A converter is not to be used.
	AVCCA	Input	Analog voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VCC if the 24-bit ΔΣ A/D converter is not to be used.
	AVSSA	Input	Analog ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSH	—	Reference voltage supply pin for the 24-bit ΔΣ A/D converter. Connect this pin to the VREFDSL pin via a 1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	VREFDSL	Input	Reference voltage ground pin for the 24-bit ΔΣ A/D converter. Connect this pin to VSS if the 24-bit ΔΣ A/D converter is not to be used.
	VCOMDS	—	Common mode voltage pin for the 24-bit ΔΣ A/D converter. Connect this pin to the AVSSA pin via a 0.1μF capacitor. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
	BGR_BO	Input	Internal reference voltage input pin for the 24-bit ΔΣ A/D converter. Leave this pin open if the 24-bit ΔΣ A/D converter is not to be used.
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 input pins)
	P40 to P43	I/O	4-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PE6, PE7	I/O	2-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3	I/O	2-bit input/output pins.

Table 4.1 List of I/O Registers (Address Order) (9 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8		2 ICLK
0008 73E6h	ICU	Interrupt source priority register 230	IPR230	8	8		2 ICLK
0008 73EAh	ICU	Interrupt source priority register 234	IPR234	8	8		2 ICLK
0008 73F6h	ICU	Interrupt source priority register 246	IPR246	8	8		2 ICLK
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8		2 ICLK
0008 73F8h	ICU	Interrupt source priority register 248	IPR248	8	8		2 ICLK
0008 73F9h	ICU	Interrupt source priority register 249	IPR249	8	8		2 ICLK
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8		2 ICLK
0008 73FBh	ICU	Interrupt source priority register 251	IPR251	8	8		2 ICLK
0008 73FCh	ICU	Interrupt source priority register 252	IPR252	8	8		2 ICLK
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8		2 ICLK
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8		2 ICLK
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8		2 ICLK
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8		2 ICLK
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8		2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8		2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8		2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8		2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8		2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8		2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8		2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8		2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8		2 ICLK
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8		2 ICLK
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16		2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8		2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8		2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8		2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8		2 ICLK
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8		2 ICLK
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	8	8		2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK

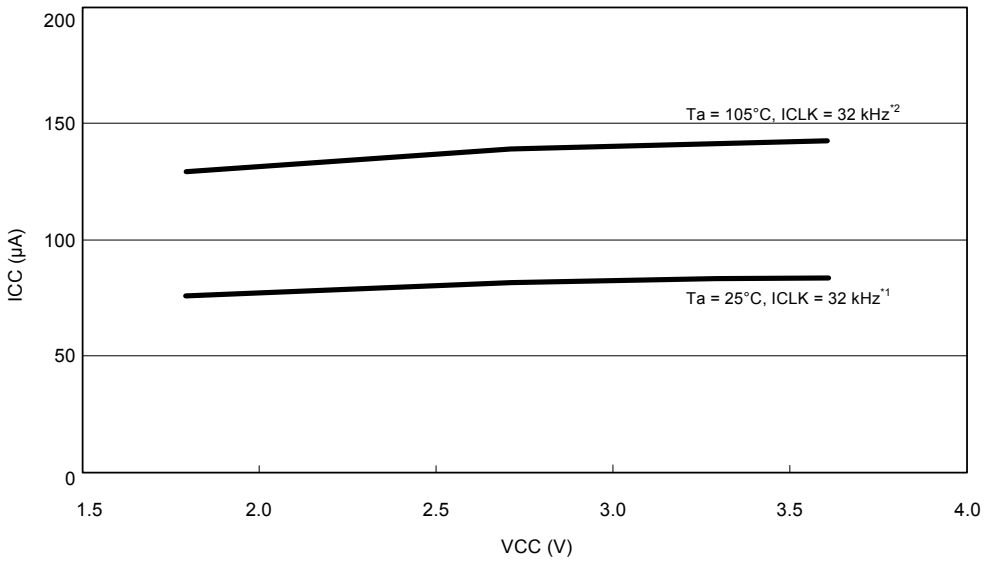
Table 4.1 List of I/O Registers (Address Order) (11 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8310h	RIIC0	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8311h	RIIC0	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8312h	RIIC0	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8313h	RIIC0	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8320h	RIIC1	I2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK
0008 8321h	RIIC1	I2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8322h	RIIC1	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK
0008 8323h	RIIC1	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK
0008 8324h	RIIC1	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK
0008 8325h	RIIC1	I2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK
0008 8326h	RIIC1	I2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK
0008 8327h	RIIC1	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK
0008 8328h	RIIC1	I2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK
0008 8329h	RIIC1	I2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK
0008 832Ah	RIIC1	Timeout internal counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK
0008 832Bh	RIIC1	Timeout internal counter U	TMOCNTU	8	8*2	2, 3 PCLKB	2 ICLK
0008 832Ch	RIIC1	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK
0008 832Dh	RIIC1	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK
0008 832Eh	RIIC1	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK
0008 832Fh	RIIC1	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK
0008 8330h	RIIC1	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK
0008 8331h	RIIC1	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK
0008 8332h	RIIC1	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK
0008 8333h	RIIC1	I2C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
FEFF FB74h	DSAD	ΔΣA/D gain calibration data register 1 X4*3	DSADG1X4	32	32		1ICLK
FEFF FB78h	DSAD	ΔΣA/D gain calibration data register 2 X4*3	DSADG2X4	32	32		1ICLK
FEFF FB7Ch	DSAD	ΔΣA/D gain calibration data register 3 X4*3	DSADG3X4	32	32		1ICLK
FEFF FB80h	DSAD	ΔΣA/D gain calibration data register 4 X4*3	DSADG4X4	32	32		1ICLK
FEFF FB84h	DSAD	ΔΣA/D gain calibration data register 5 X4*3	DSADG5X4	32	32		1ICLK
FEFF FB88h	DSAD	ΔΣA/D gain calibration data register 6 X4*3	DSADG6X4	32	32		1ICLK
FEFF FB90h	DSAD	ΔΣA/D gain calibration data register 0 X8*3	DSADG0X8	32	32		1ICLK
FEFF FB94h	DSAD	ΔΣA/D gain calibration data register 1 X8*3	DSADG1X8	32	32		1ICLK
FEFF FB98h	DSAD	ΔΣA/D gain calibration data register 2 X8*3	DSADG2X8	32	32		1ICLK
FEFF FB9Ch	DSAD	ΔΣA/D gain calibration data register 3 X8*3	DSADG3X8	32	32		1ICLK
FEFF FBA0h	DSAD	ΔΣA/D gain calibration data register 0 X16*3	DSADG0X16	32	32		1ICLK
FEFF FBA4h	DSAD	ΔΣA/D gain calibration data register 1 X16*3	DSADG1X16	32	32		1ICLK
FEFF FBA8h	DSAD	ΔΣA/D gain calibration data register 2 X16*3	DSADG2X16	32	32		1ICLK
FEFF FBACh	DSAD	ΔΣA/D gain calibration data register 3 X16*3	DSADG3X16	32	32		1ICLK
FEFF FBB0h	DSAD	ΔΣA/D gain calibration data register 0 X32*3	DSADG0X32	32	32		1ICLK
FEFF FBB4h	DSAD	ΔΣA/D gain calibration data register 1 X32*3	DSADG1X32	32	32		1ICLK
FEFF FBB8h	DSAD	ΔΣA/D gain calibration data register 2 X32*3	DSADG2X32	32	32		1ICLK
FEFF FBBCh	DSAD	ΔΣA/D gain calibration data register 3 X32*3	DSADG3X32	32	32		1ICLK
FEFF FBD0h	DSAD	ΔΣA/D input impedance calibration data register*3	DSADIIC	32	32		1ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 24.4 lists register allocation for 16-bit access.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register. Table 31.3 lists register allocation for 16-bit access.
Note 3. Only G version products have these registers.



Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.5 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data)

Table 5.8 DC Characteristics (7)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T_a = 25°C	I_{CC}	10	20	µA	
			T_a = 55°C		12	41		
			T_a = 85°C		18	113		
			T_a = 105°C		29	233		
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T_a = 25°C		1.7	7.9		
			T_a = 55°C		2.7	25		
			T_a = 85°C		7.0	86		
			T_a = 105°C		16	189		
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled	T_a = 25°C		0.3	0.8		
			T_a = 55°C		0.4	1.1		
			T_a = 85°C		0.8	2.2		
			T_a = 105°C		1.3	4.7		
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.2	—		
	Increment for RTC operation (low CL)				0.6	—		
	Increment for RTC operation (standard CL)				1.4	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 3.3 V.

5.3 AC Characteristics

Table 5.19 Operation Frequency Value (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC	Unit
			2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	50	MHz
	FlashIF clock (FCLK)*1		25	
	Peripheral module clock (PCLKA)		50	
	Peripheral module clock (PCLKB)		25	
	Peripheral module clock (PCLKC)*2		25	
	Peripheral module clock (PCLKD)*3		25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.20 Operation Frequency Value (Medium-Speed Operating Mode 1A)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	25	25	MHz
	FlashIF clock (FCLK)*1		25	25	
	Peripheral module clock (PCLKA)		25	25	
	Peripheral module clock (PCLKB)		25	25	
	Peripheral module clock (PCLKC)*2		25	25	
	Peripheral module clock (PCLKD)*3		25	25	

Note 1. The VCC is 2.7 to 3.6 V and the lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.21 Operation Frequency Value (Medium-Speed Operating Mode 1B)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	25	25	MHz
	FlashIF clock (FCLK)*1		25	25	
	Peripheral module clock (PCLKA)		25	25	
	Peripheral module clock (PCLKB)		25	25	
	Peripheral module clock (PCLKC)*2		25	25	
	Peripheral module clock (PCLKD)*3		25	25	

Note 1. The lower-limit frequency of FCLK is 4 MHz during programming or erasing of the flash memory.
Note 2. The frequency of PCLKC is 25 MHz when the ΔΣ A/D converter is in use.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

5.4.2 Timing of Recovery from Low Power Consumption Modes

Table 5.28 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode (flash memory, HOCO power supplied) (SOFTCUT[2:0] bits = 000b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	10	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	500	µs	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of software standby mode (flash memory power supplied, HOCO power not supplied) (SOFTCUT[2:0] bits = 110b)*1	Crystal resonator connected to main clock oscillator*2	Main clock oscillator operating	t_{SBYMC}	—	3	—	ms	Figure 5.37
		Main clock oscillator and PLL circuit operating	t_{SBYPC}	—	3.5	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}	40	—	—	µs	
		Main clock oscillator and PLL circuit operating	t_{SBYPE}	0.5	—	—	ms	
	Sub-clock oscillator operating		t_{SBYSC}	2*3	—	—	s	
	HOCO clock oscillator operating		t_{SBYHO}	—	—	1.2	ms	
	LOCO clock oscillator operating		t_{SBYLO}	—	—	90	µs	
Recovery time after cancellation of deep software standby mode			t_{DSBY}	—	—	8	ms	Figure 5.38
Wait time after cancellation of deep software standby mode			t_{DSBYWT}	—	—	0.8	ms	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source, and depends on the time set in the wait control registers corresponding to the oscillators.
Note 2. The indicated value is measured for an 8 MHz crystal resonator.
Note 3. When RCR3.RTCEN = 1, the time will be the time set in the SOSCWTCR register minus 2 s.

5.4.3 Control Signal Timing

Table 5.29 Control Signal Timing

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.39
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.39
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c(PCLKB)}$ × 2 ≤ 200 ns, Figure 5.40
		$t_{c(PCLKB)}$ × 2	—	—	ns	$t_{c(PCLKB)}$ × 2 > 200 ns, Figure 5.40

Note: • 200 ns minimum in deep software standby and software standby modes.

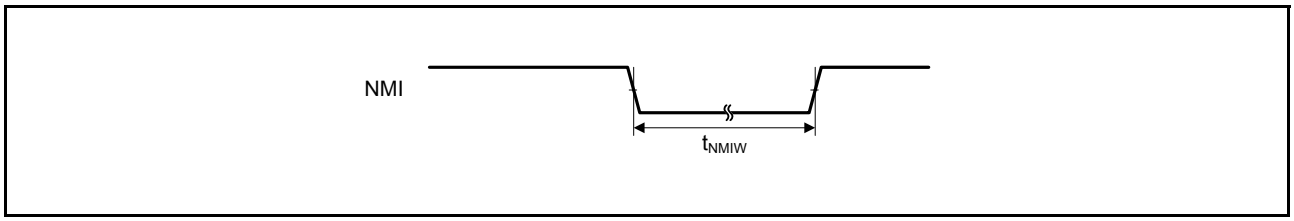


Figure 5.39 NMI Interrupt Input Timing

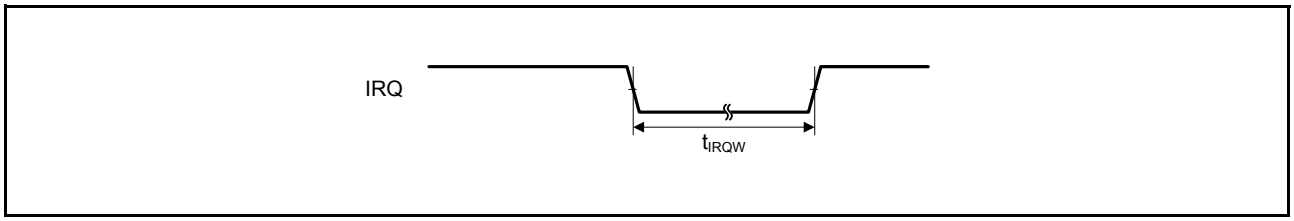


Figure 5.40 IRQ Interrupt Input Timing

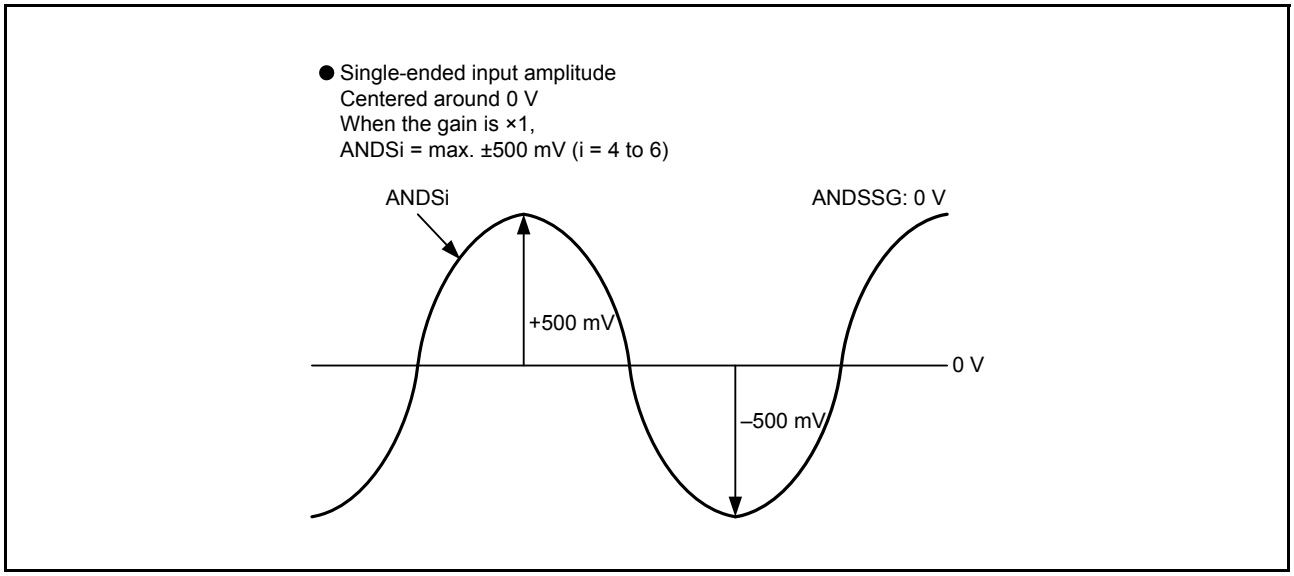


Figure 5.56 Single-ended Input Amplitude

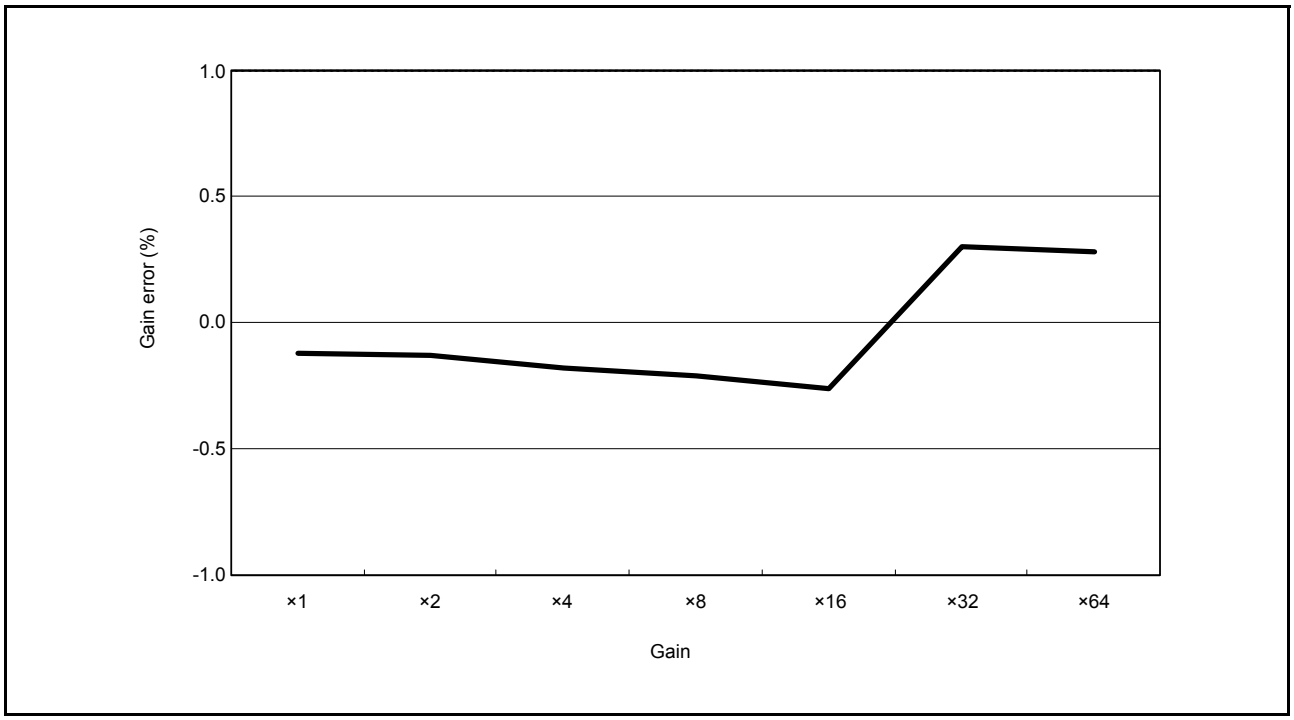
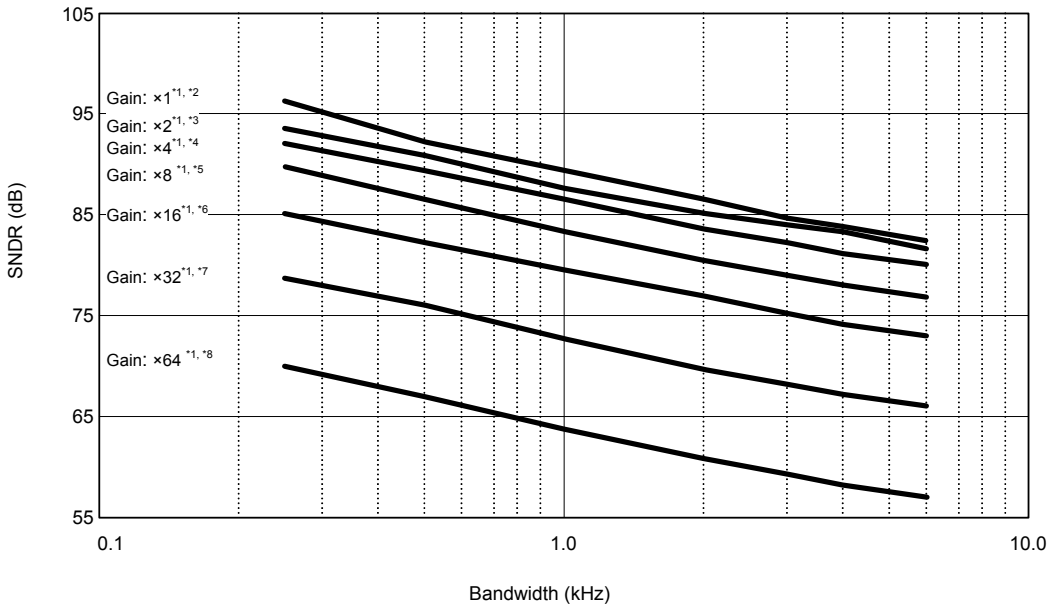


Figure 5.57 Gain Error (Reference Data)



Note 1. Input frequency: 50 Hz, sampling period: 81.92 µs
Note 2. Input amplitude: 500.0 mV
Note 3. Input amplitude: 250.0 mV
Note 4. Input amplitude: 125.0 mV
Note 5. Input amplitude: 62.5 mV
Note 6. Input amplitude: 31.2 mV
Note 7. Input amplitude: 14.4 mV
Note 8. Input amplitude: 5.0 mV

Figure 5.60 Bandwidth Dependency of SNDR (Reference Data)

Table 5.45 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_7}	2.95	3.10	3.25	V	Figure 5.68
		V_{det2_8}	2.85	2.95	3.05		At falling edge VCC
		V_{det2_9}	2.70	2.80	2.90		
		V_{det2_A}	2.55	2.65	2.75		
		V_{det2_B}	2.40	2.50	2.60		
		V_{det2_C}	2.25	2.35	2.45		
		V_{det2_D}	2.10	2.20	2.30		
		V_{det2_E}	1.95	2.05	2.15		
		V_{det2_F}	1.80	1.90	2.00		
		V_{CMPA2}	1.18	1.33	1.48		EXVCCINP2 = 1
Internal reset time	Power-on reset time	t_{POR}	—	9	—	ms	Figure 5.65
	Voltage monitoring 0 reset time	t_{LVD0}	—	9	—		Figure 5.66
	Voltage monitoring 1 reset time	t_{LVD1}	—	1.4	—		Figure 5.67
	Voltage monitoring 2 reset time	t_{LVD2}	—	1.4	—		Figure 5.68
Minimum VCC down time*2		t_{VOFF}	200	—	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	200	µs	Figure 5.65
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	15	µs	Figure 5.67 and Figure 5.68
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.65 VCC = 0.9 V or lower
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_7.
			—	50	—		When selection is from among VdetX_8 to F.

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/ LVD.

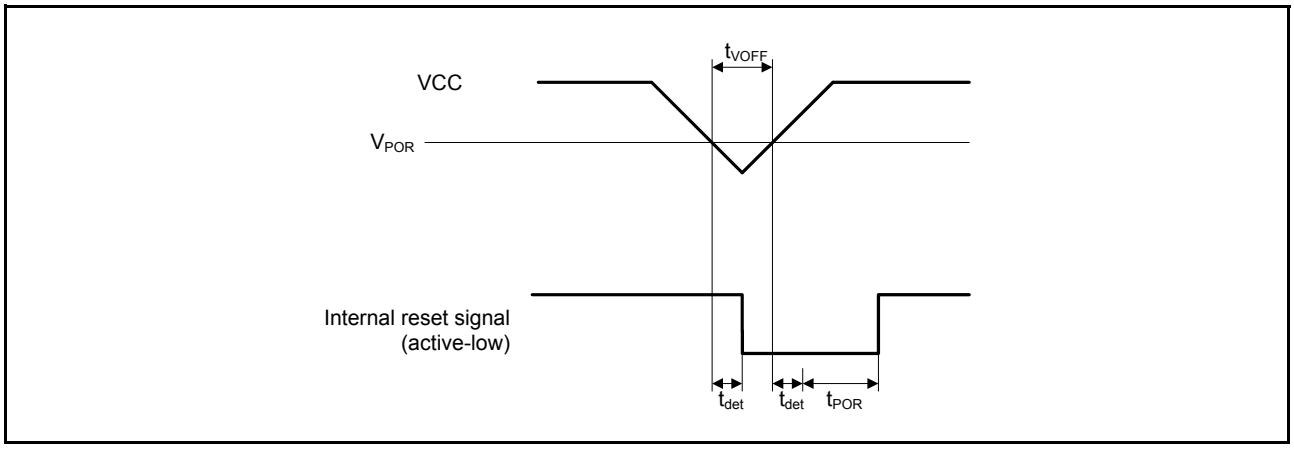
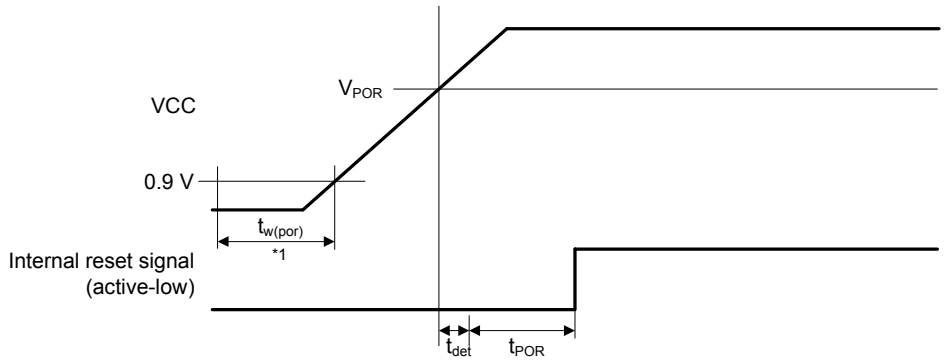


Figure 5.64 Voltage Detection Reset Timing



Note 1. $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.9 V).
When VCC turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.65 Power-on Reset Timing

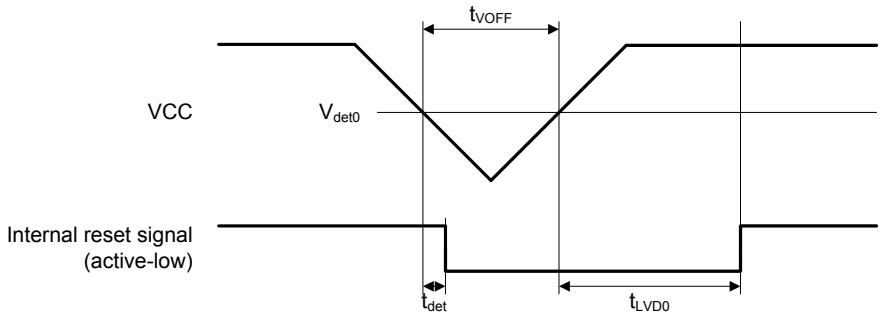


Figure 5.66 Voltage Detection Circuit Timing (V_{det0})

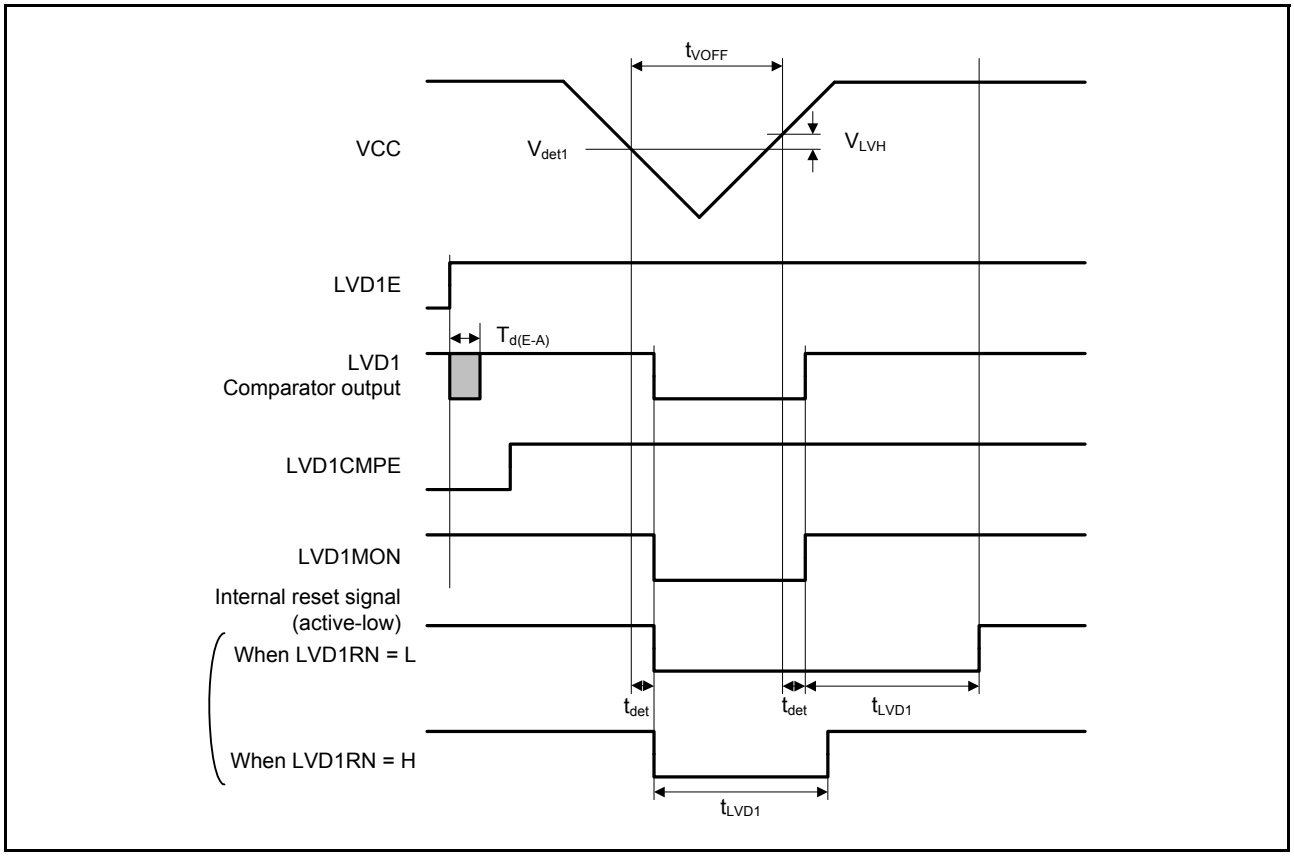


Figure 5.67 Voltage Detection Circuit Timing (V_{det1})

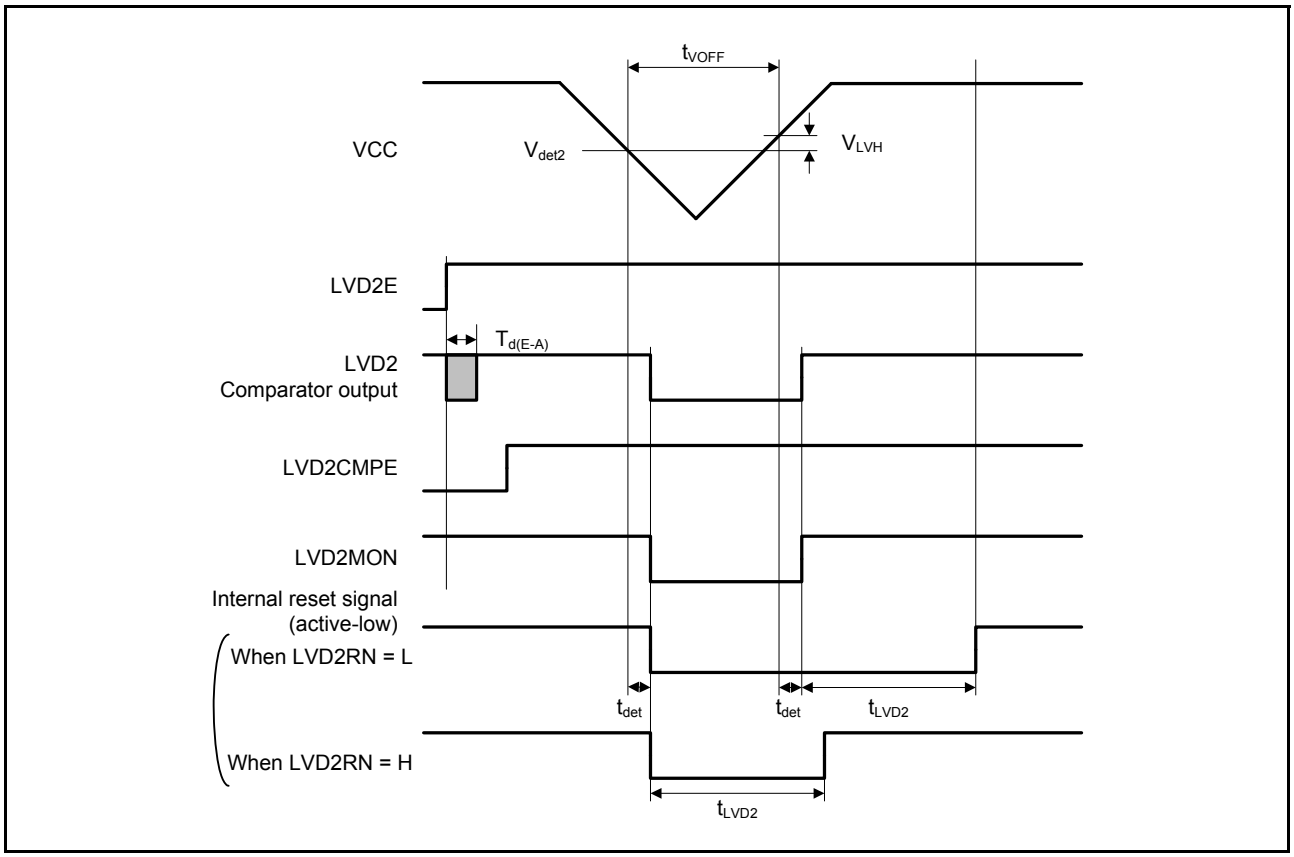


Figure 5.68 Voltage Detection Circuit Timing (V_{det2})

5.12 ROM (Flash Memory for Code Storage) Characteristics

Table 5.47 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{PEC}	10000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C
	After 10000 times of N_{PEC}		1*2	—	—		

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This result is obtained from reliability testing.

Table 5.48 ROM (Flash Memory for Code Storage) Characteristics (2) : high-speed operating mode, medium-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.19	4.3	—	0.12	2.1	ms
	8 bytes	t_{P8}	—	0.19	4.4	—	0.12	2.1	
	128 bytes	t_{P128}	—	0.67	10.7	—	0.42	5.0	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.23	5.3	—	0.15	2.6	ms
	8 bytes	t_{P8}	—	0.23	5.4	—	0.15	2.6	
	128 bytes	t_{P128}	—	0.80	13.2	—	0.50	6.3	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	13.0	92.8	—	10.6	31.6	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	15.9	176.9	—	13.0	64.7	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	0.9	—	—	0.804	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	0.9	—	—	0.804	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	0.9	—	—	0.804	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	0.9	—	—	0.804	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

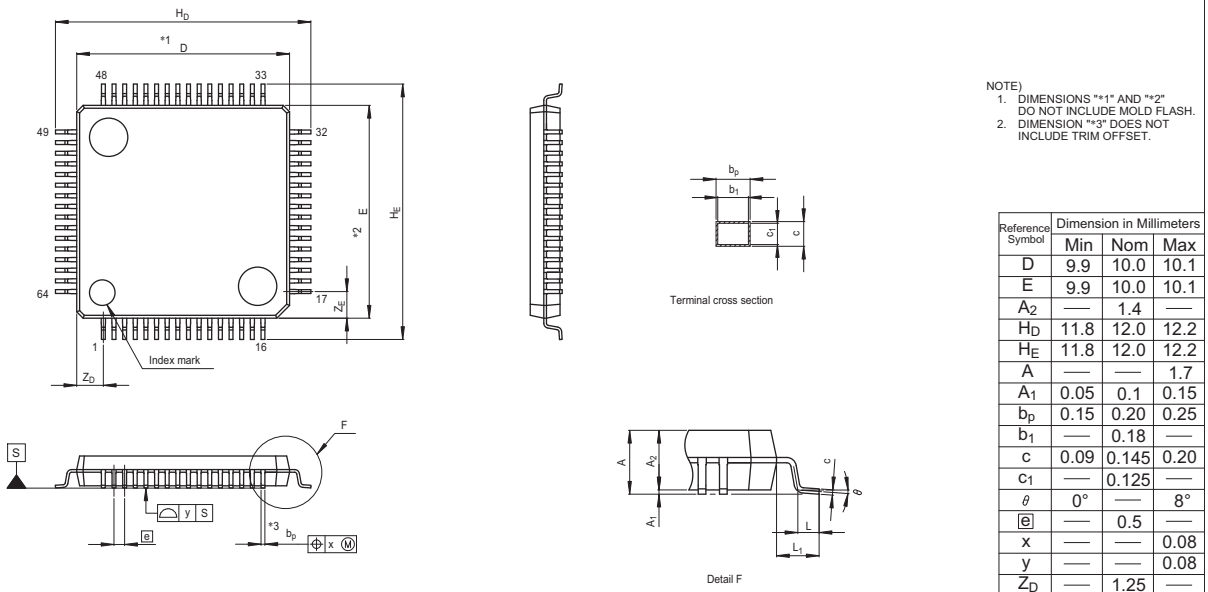
Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (3) : medium-speed operating modes 1B and 2B

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz*1			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{PEC} ≤ 100 times	2 bytes	t_{P2}	—	0.25	5.0	—	0.21	2.9	ms
	8 bytes	t_{P8}	—	0.25	5.3	—	0.21	3.1	
	128 bytes	t_{P128}	—	0.92	14.0	—	0.66	8.5	
Programming time when N_{PEC} > 100 times	2 bytes	t_{P2}	—	0.31	6.2	—	0.26	3.6	ms
	8 bytes	t_{P8}	—	0.31	6.6	—	0.26	3.8	
	128 bytes	t_{P128}	—	1.09	17.5	—	0.78	10.3	
Erasure time when N_{PEC} ≤ 100 times	2 Kbytes	t_{E2K}	—	21.0	113.6	—	18.6	48.7	ms
Erasure time when N_{PEC} > 100 times	2 Kbytes	t_{E2K}	—	25.6	220.6	—	22.7	94.5 (1000 times ≥ N_{PEC} > 100 times), 102.9 (10000 times ≥ N_{PEC} > 1000 times)	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{SPD}	—	—	1.7	—	—	1.604	ms
First suspend delay time during programming (in suspend priority mode)		t_{SPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{SPSD2}	—	—	1.7	—	—	1.604	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{SED}	—	—	1.7	—	—	1.604	ms
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.604	ms
FCU reset time		t_{FCUR}	20 µs or longer and FCLK × 6 or greater	—	—	20 µs or longer and FCLK × 6 or greater	—	—	µs

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 64-Pin LQFP (PLQP0064KB-A)

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	2014.08.28	Features		
		1	LGA package, added	TN-RX*-A072A/E
		1. Overview		
		5	Table 1.1 Outline of Specifications: Package added	TN-RX*-A072A/E
		5	Table 1.1 Outline of Specifications: Note 2 added	TN-RX*-A073A/E
		5	Table 1.1 Outline of Specifications: Note 3 added	
		5	Table 1.2 Comparison of Functions for Different Packages, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products, changed	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note 1 added	TN-RX*-A072A/E
		6	Table 1.3 List of Products: Note, Note 2 added	
		7	Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type, changed	TN-RX*-A072A/E
		9	Table 1.4 Pin Functions: Realtime clock changed	
		15	Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View), added	TN-RX*-A072A/E
		23 to 25	Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA), added	TN-RX*-A072A/E
		3. Address Space		
		29	Figure 3.1 Memory Map, changed	
		4. I/O Registers		
		54 to 55	Table 4.1 List of I/O Registers (Address Order): FEFF FAC0h to FEFF FBD3h added	
		5. Electrical Characteristics		
		57	Table 5.3 DC Characteristics (2)	TN-RX*-A074A/E
		58	Table 5.4 DC Characteristics (3), changed	TN-RX*-A074A/E
		59	Table 5.6 DC Characteristics (5), changed	TN-RX*-A074A/E
		60	Table 5.7 DC Characteristics (6), changed	TN-RX*-A074A/E
		68	Table 5.9 DC Characteristics (8), added	TN-RX*-A074A/E
		68	Table 5.10 DC Characteristics (9), changed	
		68	Table 5.11 DC Characteristics (10), changed	
		69	Table 5.14 DC Characteristics (13), changed	TN-RX*-A074A/E
		69	Table 5.15 Permissible Output Currents (1), changed Table 5.16 Permissible Output Currents (2), added	TN-RX*-A074A/E
		70	Table 5.18 Output Values of Voltage (2), changed	TN-RX*-A074A/E
		82	Table 5.26 Clock Timing, changed	TN-RX*-A097A/E
		83	Table 5.26 Clock Timing: Note 5 changed	TN-RX*-A105A/E
		83	Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing, changed	TN-RX*-A097A/E
		87	Figure 5.35 Reset Input Timing at Power-On, changed	TN-RX*-A074A/E
		94	Table 5.33 Timing of On-Chip Peripheral Modules (4), changed	TN-RX*-A074A/E
		103	Table 5.36 ΔΣ A/D Conversion Characteristics, changed	TN-RX*-A105A/E
		104	Figure 5.55 Differential Input Amplitude, changed	
		108	Table 5.37 A/D Conversion Characteristics (1), changed	TN-RX*-A074A/E
		108	Figure 5.61 AVCC to VREFH0 Voltage Range, added	TN-RX*-A074A/E
		109	Table 5.39 A/D Conversion Characteristics (2), changed	TN-RX*-A074A/E
		111	Differential nonlinearity error (DNL), description changed	TN-RX*-A073A/E
		115	Table 5.44 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (1): Note1, Note2 changed	TN-RX*-A074A/E
		Appendix 1. Package Dimensions		
		128	Figure D. 100-Pin TFLGA (PTLG0100JA-A), added	TN-RX*-A072A/E

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.