Renesas Electronics America Inc - R5F521A8BDFN#V0 Datasheet

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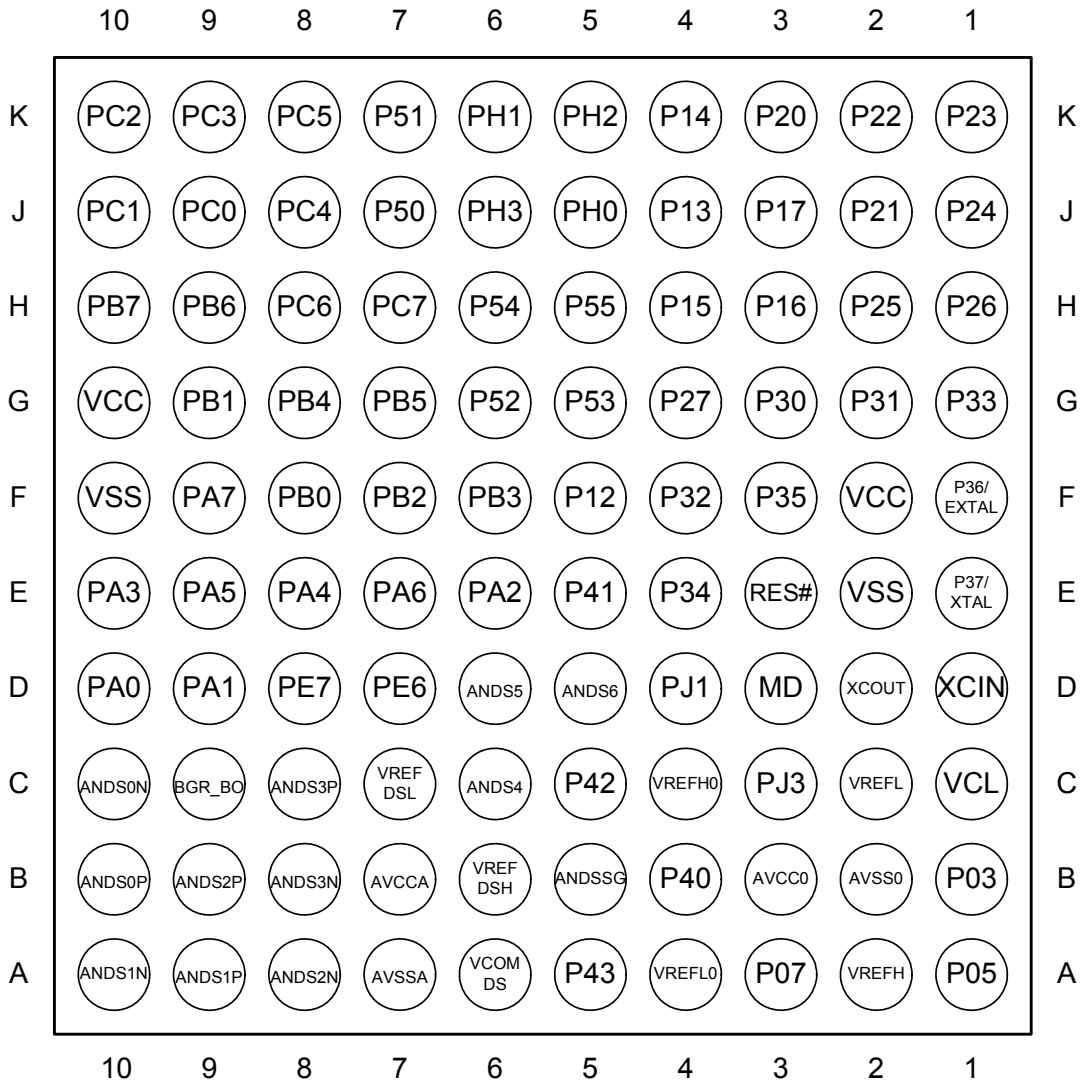
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a8bdfn-v0

RX21A Group
PTLG0100JA-A
(100-pin TFLGA)
(Upper perspective view)



Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.
Note: • For the position of A1 pin in the package, see “Package Dimensions”.

Figure 1.6 Pin Assignments of the 100-Pin TFLGA (Upper Perspective View)

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
42		P52		SSLB3	
43		P51		SSLB2	
44		P50		SSLB1	
45		PC7	MTIOC3A/TMO2/MTCLKB	TXD8/SMOSI8/SSDA8/ MISOA	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/ MOSIA	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/ IRTXD5	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	
51		PC1	MTIOC3A	SCK5/SSLA2	
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	
56		PB4		CTS9#/RTS9#/SS9#	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	
58		PB2		CTS6#/RTS6#/SS6#	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	IRQ4-DS
60	VCC				
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/ RSPCKA	CMPB0
62	VSS				
63		PA7		MISOA	
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
65		PA5		RSPCKA	
66		PA4	MTIC5U/MTCLKA/ TMRI0	TXD5/SMOSI5/SSDA5/ IRTXD5/SSLA0	IRQ5-DS/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/ IRRXD5	IRQ6-DS/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/ IRRXD5/SSLA3	CMPA2
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
70		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
71		PE7		MISOB	IRQ7-DS
72		PE6		MOSIB	IRQ6
73	BGR_BO				
74					ANDS0N
75					ANDS0P
76					ANDS1N
77					ANDS1P
78					ANDS2N

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.
When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DMAC or DTC).

Table 4.1 List of I/O Registers (Address Order) (2 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32		2 ICLK
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16		2 ICLK
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8		2 ICLK
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8		2 ICLK
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32		2 ICLK
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32		2 ICLK
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16		2 ICLK
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8		2 ICLK
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8		2 ICLK
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32		2 ICLK
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32		2 ICLK
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32		2 ICLK
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16		2 ICLK
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16		2 ICLK
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8		2 ICLK
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16		2 ICLK
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8		2 ICLK
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8		2 ICLK
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8		2 ICLK
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8		2 ICLK
0008 2200h	DMAC	DMA module activation register	DMAST	8	8		2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8		2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32		2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8		2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8		2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16		2 ICLK
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32		1 ICLK
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32		1 ICLK
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32		1 ICLK
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32		1 ICLK
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32		1 ICLK
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32		1 ICLK
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32		1 ICLK
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32		1 ICLK
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32		1 ICLK
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32		1 ICLK
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32		1 ICLK

Table 4.1 List of I/O Registers (Address Order) (4 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8		2 ICLK
0008 706Bh	ICU	Interrupt request register 107	IR107	8	8		2 ICLK
0008 706Ch	ICU	Interrupt request register 108	IR108	8	8		2 ICLK
0008 706Dh	ICU	Interrupt request register 109	IR109	8	8		2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8		2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8		2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8		2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8		2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8		2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8		2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8		2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8		2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8		2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8		2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8		2 ICLK
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8		2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8		2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8		2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8		2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8		2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8		2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8		2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8		2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8		2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8		2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8		2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8		2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8		2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8		2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8		2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8		2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8		2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8		2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8		2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8		2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8		2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8		2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8		2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8		2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8		2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8		2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8		2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8		2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8		2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8		2 ICLK
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8		2 ICLK
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8		2 ICLK
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8		2 ICLK
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8		2 ICLK
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8		2 ICLK
0008 70CEh	ICU	Interrupt request register 206	IR206	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 733Ah	ICU	Interrupt source priority register 058	IPR058	8	8		2 ICLK
0008 733Bh	ICU	Interrupt source priority register 059	IPR059	8	8		2 ICLK
0008 733Fh	ICU	Interrupt source priority register 063	IPR063	8	8		2 ICLK
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8		2 ICLK
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8		2 ICLK
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8		2 ICLK
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8		2 ICLK
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8		2 ICLK
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8		2 ICLK
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8		2 ICLK
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8		2 ICLK
0008 7358h	ICU	Interrupt source priority register 088	IPR088	8	8		2 ICLK
0008 7359h	ICU	Interrupt source priority register 089	IPR089	8	8		2 ICLK
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8		2 ICLK
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8		2 ICLK
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8		2 ICLK
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8		2 ICLK
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8		2 ICLK
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8		2 ICLK
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8		2 ICLK
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8		2 ICLK
0008 7376h	ICU	Interrupt source priority register 118	IPR118	8	8		2 ICLK
0008 7379h	ICU	Interrupt source priority register 121	IPR121	8	8		2 ICLK
0008 737Bh	ICU	Interrupt source priority register 123	IPR123	8	8		2 ICLK
0008 737Dh	ICU	Interrupt source priority register 125	IPR125	8	8		2 ICLK
0008 737Fh	ICU	Interrupt source priority register 127	IPR127	8	8		2 ICLK
0008 7381h	ICU	Interrupt source priority register 129	IPR129	8	8		2 ICLK
0008 7385h	ICU	Interrupt source priority register 133	IPR133	8	8		2 ICLK
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8		2 ICLK
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8		2 ICLK
0008 738Bh	ICU	Interrupt source priority register 139	IPR139	8	8		2 ICLK
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8		2 ICLK
0008 73ABh	ICU	Interrupt source priority register 171	IPR171	8	8		2 ICLK
0008 73AEh	ICU	Interrupt source priority register 174	IPR174	8	8		2 ICLK
0008 73B1h	ICU	Interrupt source priority register 177	IPR177	8	8		2 ICLK
0008 73B4h	ICU	Interrupt source priority register 180	IPR180	8	8		2 ICLK
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8		2 ICLK
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8		2 ICLK
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8		2 ICLK
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8		2 ICLK
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8		2 ICLK
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8		2 ICLK
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8		2 ICLK
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8		2 ICLK
0008 73D1h	ICU	Interrupt source priority register 209	IPR209	8	8		2 ICLK
0008 73D2h	ICU	Interrupt source priority register 210	IPR210	8	8		2 ICLK
0008 73D3h	ICU	Interrupt source priority register 211	IPR211	8	8		2 ICLK
0008 73D4h	ICU	Interrupt source priority register 212	IPR212	8	8		2 ICLK
0008 73D5h	ICU	Interrupt source priority register 213	IPR213	8	8		2 ICLK
0008 73DAh	ICU	Interrupt source priority register 218	IPR218	8	8		2 ICLK
0008 73DEh	ICU	Interrupt source priority register 222	IPR222	8	8		2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D1h	PORTH	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E1h	PORT1	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E2h	PORT2	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E3h	PORT3	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0E5h	PORT5	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EAh	PORTA	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EBh	PORTB	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0ECh	PORTC	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0EEh	PORTE	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F1h	PORTH	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C0F2h	PORTJ	Drive capacity control register	DSCR	8	8	2, 3 PCLKB	2 ICLK
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK
0008 C121h	PORT	Port switching register A	PSRA	8	8	2, 3 PCLKB	2 ICLK
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles: ICLK ≥ PCLK	Number of Access Cycles: ICLK < PCLK
FEFF FB74h	DSAD	ΔΣA/D gain calibration data register 1 X4*3	DSADG1X4	32	32		1ICLK
FEFF FB78h	DSAD	ΔΣA/D gain calibration data register 2 X4*3	DSADG2X4	32	32		1ICLK
FEFF FB7Ch	DSAD	ΔΣA/D gain calibration data register 3 X4*3	DSADG3X4	32	32		1ICLK
FEFF FB80h	DSAD	ΔΣA/D gain calibration data register 4 X4*3	DSADG4X4	32	32		1ICLK
FEFF FB84h	DSAD	ΔΣA/D gain calibration data register 5 X4*3	DSADG5X4	32	32		1ICLK
FEFF FB88h	DSAD	ΔΣA/D gain calibration data register 6 X4*3	DSADG6X4	32	32		1ICLK
FEFF FB90h	DSAD	ΔΣA/D gain calibration data register 0 X8*3	DSADG0X8	32	32		1ICLK
FEFF FB94h	DSAD	ΔΣA/D gain calibration data register 1 X8*3	DSADG1X8	32	32		1ICLK
FEFF FB98h	DSAD	ΔΣA/D gain calibration data register 2 X8*3	DSADG2X8	32	32		1ICLK
FEFF FB9Ch	DSAD	ΔΣA/D gain calibration data register 3 X8*3	DSADG3X8	32	32		1ICLK
FEFF FBA0h	DSAD	ΔΣA/D gain calibration data register 0 X16*3	DSADG0X16	32	32		1ICLK
FEFF FBA4h	DSAD	ΔΣA/D gain calibration data register 1 X16*3	DSADG1X16	32	32		1ICLK
FEFF FBA8h	DSAD	ΔΣA/D gain calibration data register 2 X16*3	DSADG2X16	32	32		1ICLK
FEFF FBACh	DSAD	ΔΣA/D gain calibration data register 3 X16*3	DSADG3X16	32	32		1ICLK
FEFF FBB0h	DSAD	ΔΣA/D gain calibration data register 0 X32*3	DSADG0X32	32	32		1ICLK
FEFF FBB4h	DSAD	ΔΣA/D gain calibration data register 1 X32*3	DSADG1X32	32	32		1ICLK
FEFF FBB8h	DSAD	ΔΣA/D gain calibration data register 2 X32*3	DSADG2X32	32	32		1ICLK
FEFF FBBCh	DSAD	ΔΣA/D gain calibration data register 3 X32*3	DSADG3X32	32	32		1ICLK
FEFF FBD0h	DSAD	ΔΣA/D input impedance calibration data register*3	DSADIIC	32	32		1ICLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 24.4 lists register allocation for 16-bit access.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register. Table 31.3 lists register allocation for 16-bit access.
Note 3. Only G version products have these registers.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Input voltage (except for ports for 5 V tolerant*1)	V_{in}	–0.3 to VCC + 0.3*3	V
Input voltage (ports for 5 V tolerant*1)	V_{in}	–0.3 to +6.5	V
Reference power supply voltage	VREFH, VREFH0	–0.3 to VCC + 0.3*3	V
Analog power supply voltage	AVCC0, AVCCA, BGR_BO*2	–0.3 to +6.5	V
A/D converter analog input voltage	V_{AN}	–0.3 to VCC + 0.3*3	V
ΔΣ A/D converter analog input voltage	V_{ANDS}	–0.6 to VCC + 0.3*3	V
Operating temperature	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, the AVCCA and AVSSA pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Connect the VCL pin to a VSS pin via a 0.1 µF (±20% accuracy) capacitor. The capacitor must be placed as close to the pin as possible.

Note 1. Ports 12, 13, 16, 17, 20, and 21 are 5 V tolerant.

Note 2. Set AVCC0 and AVCCA to the same potential as VCC. When neither the A/D converter, the D/A converter, nor ΔΣ A/D converter is in use, do not leave the AVCC0, VREFH, AVCCA, VREFH0, AVSS0, VREFL, AVSSA, and VREFL0 pins open. Connect the AVCC0, VREFH, AVCCA, and VREFH0 pins to VCC, and the AVSS0, VREFL, AVSSA, and VREFL0 pins to VSS, respectively.

Note 3. The maximum value is 6.5 V.

Table 5.4 DC Characteristics (3)

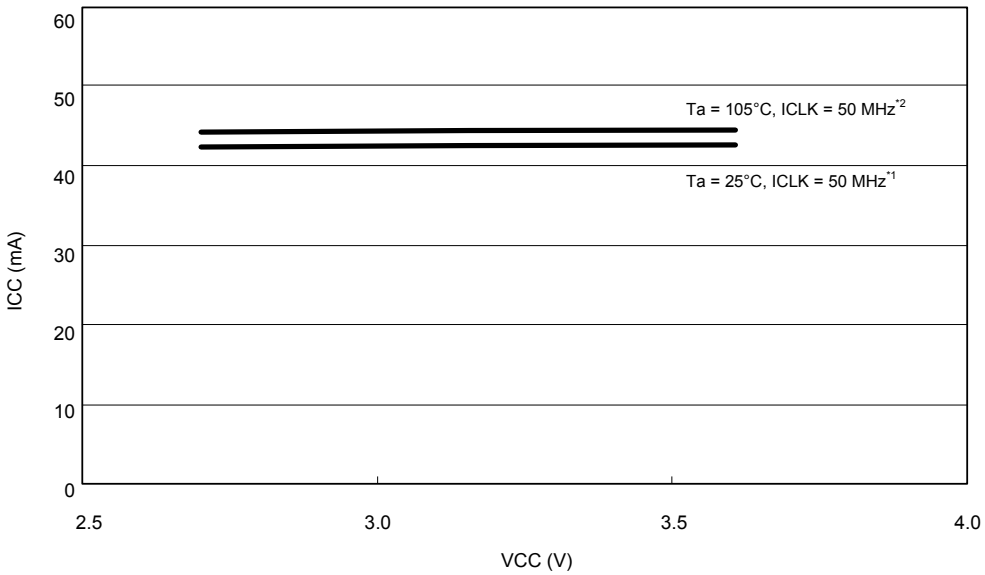
Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD pin, P35/NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
	Other pins except for ports for 5 V tolerant and port 4		—	—	0.2		
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins (except for ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 0, 12, 13, 16, 17, 20, 21, port 4, ports A0, A1, A2, A3, A4, A6, and port B0		—	—	30		

Table 5.5 DC Characteristics (4)

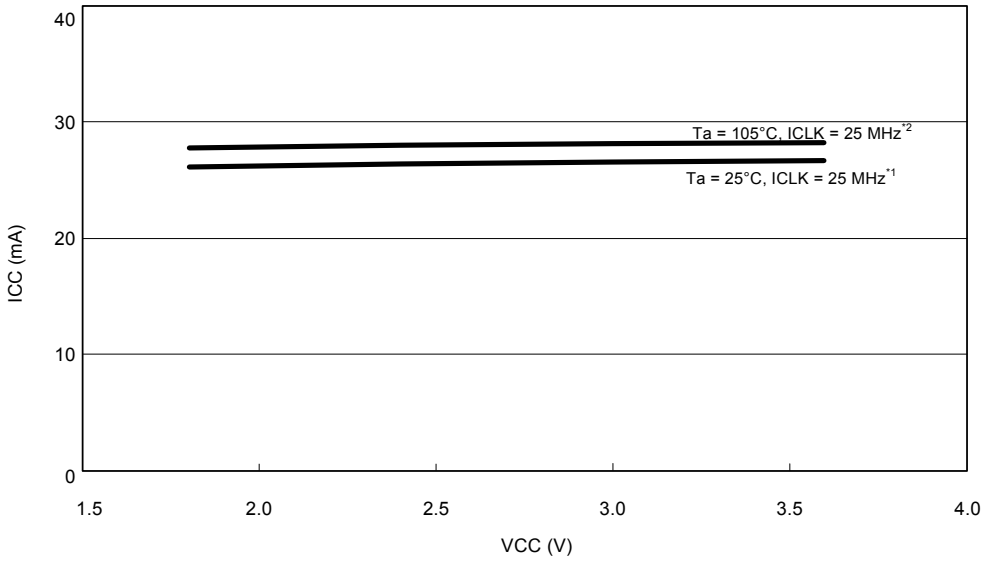
Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC				Unit	Test Conditions
			1.8 to 2.7 V		2.7 to 3.6 V			
			Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for port 35)	I_p	|5|	|150|	|10|	|200|	µA	V_{in} = 0 V



Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested middle samples during product evaluation.
Note 2. All peripheral operation is maximum. This does not include BGO operation. Average value of the tested upper-limit samples during product evaluation.

Figure 5.2 Voltage Dependency in Medium-Speed Operating Modes 1A and 1B (Reference Data)

Table 5.24 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	4	8	MHz
	FlashIF clock (FCLK)*1		4	8	
	Peripheral module clock (PCLKA)		4	8	
	Peripheral module clock (PCLKB)		4	8	
	Peripheral module clock (PCLKC)*2		4	8	
	Peripheral module clock (PCLKD)*3		4	8	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Table 5.25 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
T_a = –40 to +105°C

Item		Symbol	VCC		Unit
			1.8 to 2.7 V	2.7 to 3.6 V	
Maximum operating frequency	System clock (ICLK)	f_{max}	32.768	32.768	kHz
	FlashIF clock (FCLK)*1		32.768	32.768	
	Peripheral module clock (PCLKA)		32.768	32.768	
	Peripheral module clock (PCLKB)		32.768	32.768	
	Peripheral module clock (PCLKC)*2		32.768	32.768	
	Peripheral module clock (PCLKD)*3		32.768	32.768	

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The ΔΣ A/D converter cannot be used.
Note 3. The A/D converter cannot be used.

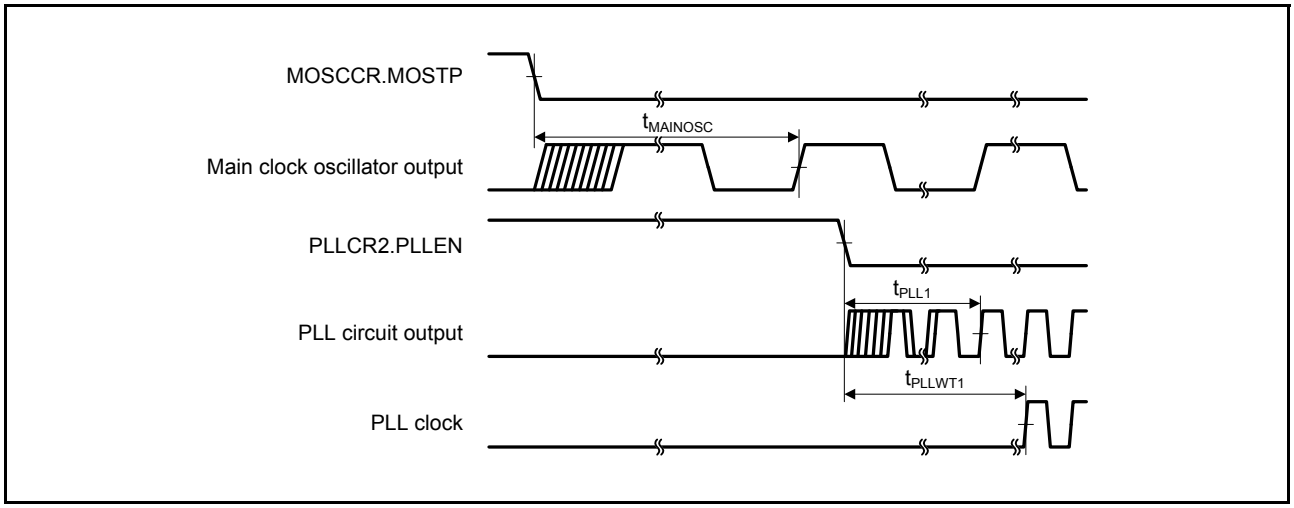


Figure 5.31 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

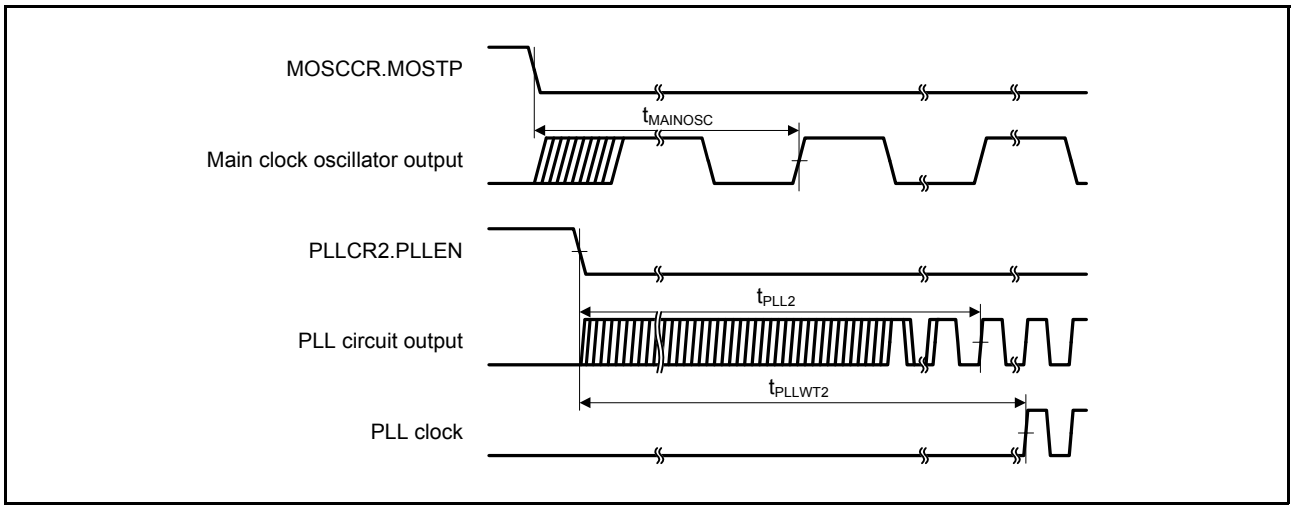


Figure 5.32 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

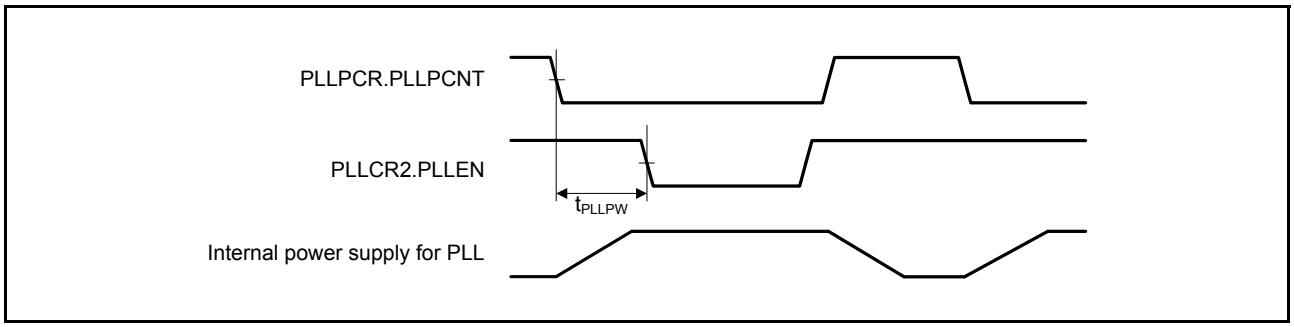


Figure 5.33 PLL Power Control Timing

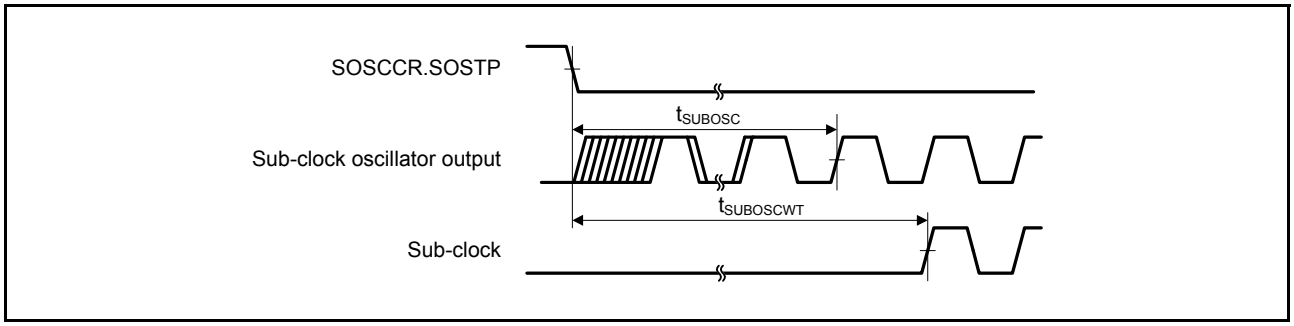


Figure 5.34 Sub-clock Oscillation Start Timing

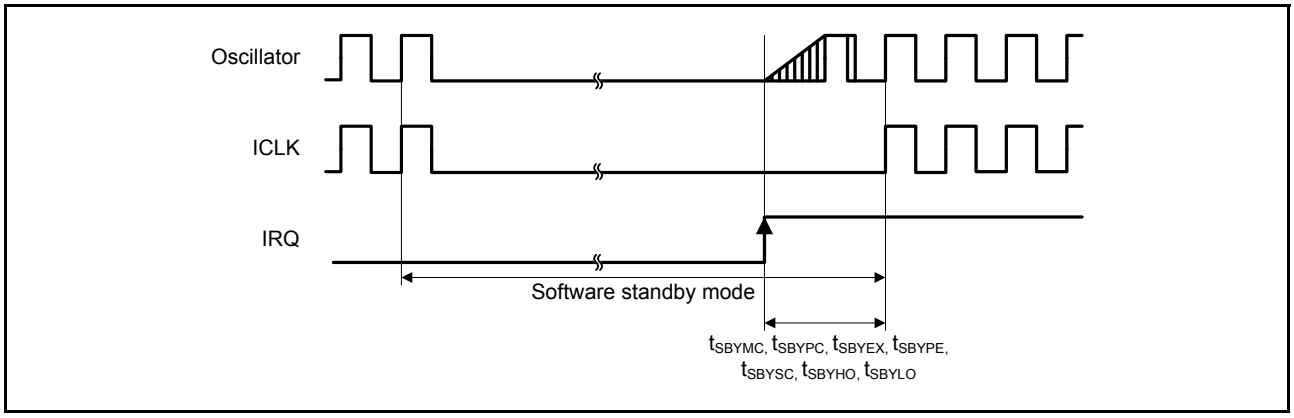


Figure 5.37 Software Standby Mode Cancellation Timing

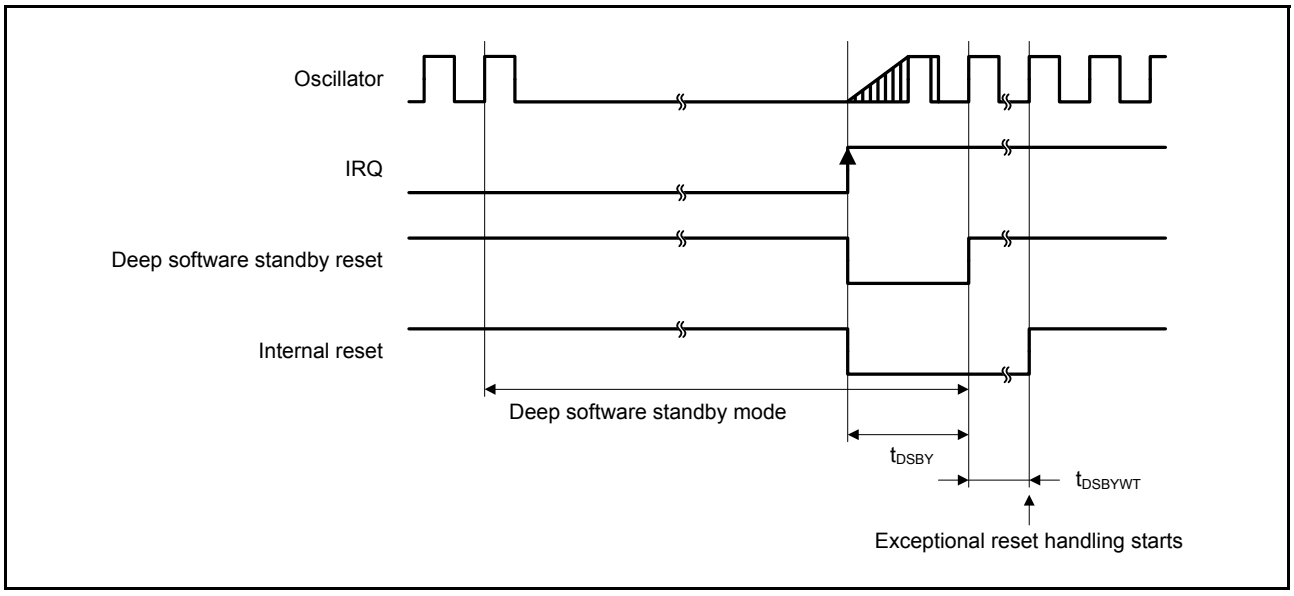


Figure 5.38 Deep Software Standby Mode Cancellation Timing

Table 5.38 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
Ta = –40 to +105

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.35	1.50	1.65	V	

Table 5.39 A/D Conversion Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, 1.8 V ≤ VREFH0 ≤ 2.7 V, AVCC0 –0.9 V ≤ VREFH0 ≤ AVCC0*3,
VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
A/D conversion clock frequency (fPCLKD)		1	—	12.5	MHz	
Resolution		—	—	10	Bit	
Conversion time*1 (Operation at fPCLKD = 12.5 MHz)	Permissible signal source impedance (Max.) = 1.5 kΩ	4.0 (2.0)*2	—	—	µs	Sampling in 25 states
Analog input capacitance		—	—	5	pF	
Offset error		—	±1.5	±3.0	LSB	
Full-scale error		—	±1.5	±3.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy*4		—	±2.0	±4.0	LSB	
DNL differential nonlinearity error*4		—	±0.5	±1.0	LSB	
INL integral nonlinearity error		—	±1.5	±3.0	LSB	

Note: • The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, fullscale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Note 3. When using the temperature sensor, use it when AVCC0 = VREFH0.

Note 4. The characteristics of the channel AN4 on a 64-pin LQFP may inferior to the values on this table; ±1.5 LSB in Absolute accuracy, ±0.5 LSB in DNL differential nonlinearity error.

5.8 Temperature Sensor Characteristics

Table 5.42 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCCA = VREFH0 = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy		—	—	±1.0	—	°C	
Temperature slope	1.8 ≤ AVCC0 < 2.7	—	—	7.27	—	mV/°C	PGAGAIN = 00b
	2.7 ≤ AVCC0 < 3.6		—	10.46	—		PGAGAIN = 01b
	AVCC0 = 3.6		—	13.98	—		PGAGAIN = 10b
Output voltage (@25°C)		—	—	1.375	—	V	VCC = 3.6 V
Temperature sensor start time		t_{START}	—	—	80	µs	Figure 5.63
Sampling time		—	30	72	300	µs	
PGA restart time		t_{RST_PGA}	—	—	40	µs	

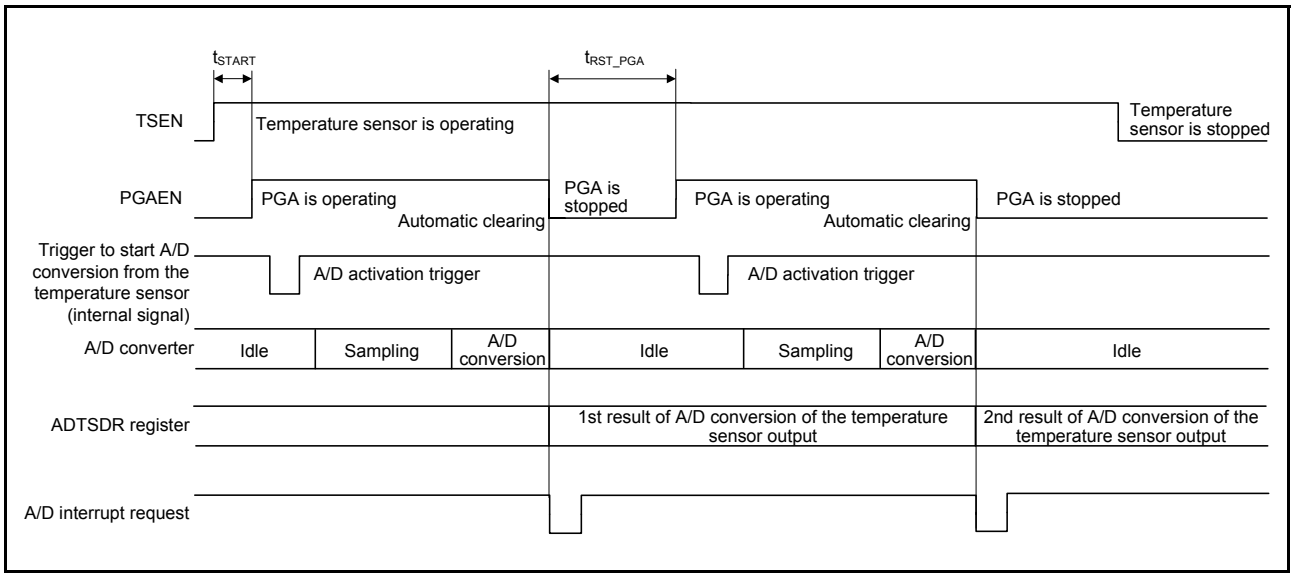


Figure 5.63 A/D Conversion Timing Example of the Temperature Sensor (Two Conversions Performed)

Table 5.45 Power-on Reset Circuit and Voltage Detection Circuit Characteristics (2)

Conditions: VCC = AVCC0 = AVCCA, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V_{det2_7}	2.95	3.10	3.25	V	Figure 5.68
		V_{det2_8}	2.85	2.95	3.05		At falling edge VCC
		V_{det2_9}	2.70	2.80	2.90		
		V_{det2_A}	2.55	2.65	2.75		
		V_{det2_B}	2.40	2.50	2.60		
		V_{det2_C}	2.25	2.35	2.45		
		V_{det2_D}	2.10	2.20	2.30		
		V_{det2_E}	1.95	2.05	2.15		
		V_{det2_F}	1.80	1.90	2.00		
		V_{CMPA2}	1.18	1.33	1.48		EXVCCINP2 = 1
Internal reset time	Power-on reset time	t_{POR}	—	9	—	ms	Figure 5.65
	Voltage monitoring 0 reset time	t_{LVD0}	—	9	—		Figure 5.66
	Voltage monitoring 1 reset time	t_{LVD1}	—	1.4	—		Figure 5.67
	Voltage monitoring 2 reset time	t_{LVD2}	—	1.4	—		Figure 5.68
Minimum VCC down time*2		t_{VOFF}	200	—	—	µs	Figure 5.65
Response delay time		t_{det}	—	—	200	µs	Figure 5.65
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	15	µs	Figure 5.67 and Figure 5.68
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 5.65 VCC = 0.9 V or lower
Hysteresis width (LVD1 and LVD2)		V_{LVH}	—	100	—	mV	When selection is from among VdetX_7.
			—	50	—		When selection is from among VdetX_8 to F.

Note: • These characteristics apply when noise is not superimposed on the power supply.

Note 1. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[3:0] bits.

Note 2. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/ LVD.

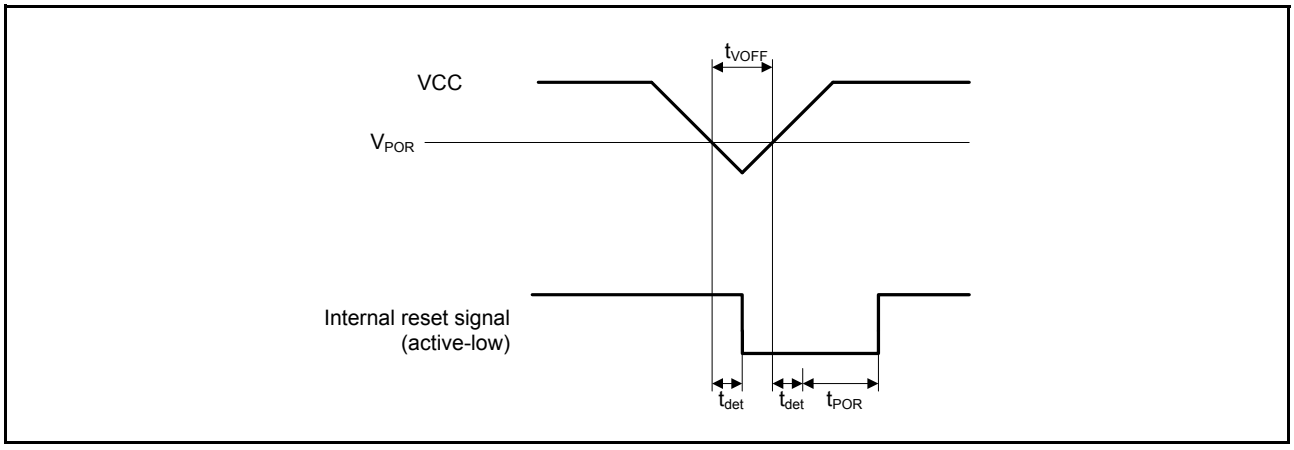


Figure 5.64 Voltage Detection Reset Timing

5.13 E2 DataFlash Characteristics

Table 5.50 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	—	—	Times	
Data hold time	After 100000 times of N_{DPEC}	t_{DRP}	30*2	—	—	Year	Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 16 times for different addresses in 128-byte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This result is obtained from reliability testing.

Table 5.51 E2 DataFlash Characteristics (2)
: high-speed operating mode, medium-speed operating modes 1A and 2A

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +105°C

Item		Symbol	FCLK = 4 MHz			FCLK = 25 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time when N_{DPEC} ≤ 100 times	2 bytes	t_{DP2}	—	0.19	4.4	—	0.13	2.1	ms
	8 bytes	t_{DP8}	—	0.24	5.1	—	0.14	2.3	
Programming time when N_{DPEC} > 100 times	2 bytes	t_{DP2}	—	0.25	6.4	—	0.17	3.1	ms
	8 bytes	t_{DP8}	—	0.32	7.5	—	0.18	3.4	
Erasure time when N_{DPEC} ≤ 100 times	128 bytes	t_{DE128}	—	3.3	27.1	—	2.5	8.8	ms
Erasure time when N_{DPEC} > 100 times	128 bytes	t_{DE128}	—	4.0	45.1	—	3.1	13.3	ms
Blank check time	2 bytes	t_{DBC2}	—	—	98	—	—	38	µs
	2 Kbytes	t_{DBC2K}	—	—	16	—	—	3.0	ms
Suspend delay time during programming (in programming/erasure priority mode)		t_{DSPD}	—	—	0.9	—	—	0.804	ms
First suspend delay time during programming (in suspend priority mode)		t_{DSPSD1}	—	—	220	—	—	124	µs
Second suspend delay time during programming (in suspend priority mode)		t_{DSPSD2}	—	—	0.9	—	—	0.804	ms
Suspend delay time during erasing (in programming/erasure priority mode)		t_{DSED}	—	—	0.9	—	—	0.804	ms
First suspend delay time during erasing (in suspend priority mode)		t_{DSESD1}	—	—	220	—	—	124	µs
Second suspend delay time during erasing (in suspend priority mode)		t_{DSESD2}	—	—	0.9	—	—	0.804	ms

REVISION HISTORY	RX21A Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 24, 2012	—	First edition, issued