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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x24b, 7x10b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f521a8bdlj-u0

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIc, RSPI, RIIC)	Others
1	VREFH				
2		P03			AN4/DA0
3	VREFL				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	
5	VCL				
6		PJ1	MTIOC3A		
7	MD				FINED
8	XCIN				
9	XCOUT				
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		P35			NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6	IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6	IRQ3-DS
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	IRQ2-DS/RTCOUT/RTCIC2
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#/SSLB0	IRQ1-DS/RTCIC1
20		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1/MISOB	IRQ0-DS/RTCIC0
21		P27	MTIOC2B/TMCI3	SCK1/RSPCKB	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/MOSIB	
23		P25	MTIOC4C/MTCLKB		ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1		
25		P23	MTIOC3D/MTCLKD		
26		P22	MTIOC3B/MTCLKC/TMO0		
27		P21	MTIOC1B/TMCI0	SCL1	
28		P20	MTIOC1A/TMRI0	SDA1	
29		P17	MTIOC3A/MTIOC3B/TMO1/POE8#	SCK1/MISOA/SDA0-DS	IRQ7
30		P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL0-DS	IRQ6/RTCOUT/ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	IRQ4
33		P13	MTIOC0B/TMO3	SDA0	IRQ3
34		P12	TMCI1	SCL0	IRQ2
35		PH3	TMCI0		
36		PH2	TMRI0		IRQ1
37		PH1	TMO0		IRQ0
38		PH0			CACREF
39		P55	MTIOC4D/TMO3		
40		P54	MTIOC4B/TMCI1		
41		P53			

Table 1.7 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communication (SCIc, RSPI, RIIC)	Others
37		PB1	MTIOC0C/MTIOC4C/TMC10	TXD6/SMOSI6/SSDA6	IRQ4-DS
38	VCC				
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	CMPB0
40	VSS				
41		PA6	MTIC5V/MTCLKB/TMC13/POE2#	CTS5#/RTS5#/SS5#/MOSIA	CVREFB0
42		PA4	MTIC5U/MTCLKA/TMR10	TXD5/SMOSI5/SSDA5/IRTXD5/SSLA0	IRQ5-DS/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5/IRRXD5	IRQ6-DS/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	CVREFA
45		PA0	MTIOC4A	SSLA1	CACREF/CMPA1
46	BGR_BO				
47					ANDS0N
48					ANDS0P
49					ANDS1N
50					ANDS1P
51	AVSSA				
52	AVCCA				
53	VREFDSL				
54	VREFDSH				
55	VCOMDS				
56					ANDS4
57	ANDSSG				
58		P41			AN1
59	VREFL0				
60		P40			AN0
61	VREFH0				
62	AVCC0				
63		P05			AN5
64	AVSS0				

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

Table 4.1 List of I/O Registers (Address Order) (12 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK
0008 8410h	IRDA	IrDA control register	IRCR	8	8	2, 3 PCLKB	2 ICLK
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK
0008 8622h	MTU	Timer cycle buffer register	TGBR	16	16	2, 3 PCLKB	2 ICLK
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 907Ah	AD	A/D disconnecting detection control register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK
0008 A020h	SCI1	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A021h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A022h	SCI1	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A023h	SCI1	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A024h	SCI1	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A025h	SCI1	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A026h	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A027h	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A028h	SCI1	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A029h	SCI1	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ah	SCI1	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A02Bh	SCI1	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A02Ch	SCI1	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0A9h	SCI5	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0AAh	SCI5	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0ABh	SCI5	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0ACh	SCI5	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A0C9h	SCI6	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A0CAh	SCI6	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A0CBh	SCI6	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A0CCh	SCI6	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 24)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles	
						ICLK $\geq$ PCLK	ICLK < PCLK
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A109h	SCI8	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ah	SCI8	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A10Bh	SCI8	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A10Ch	SCI8	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK
0008 A121h	SCI9	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK
0008 A122h	SCI9	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK
0008 A123h	SCI9	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK
0008 A124h	SCI9	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK
0008 A125h	SCI9	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK
0008 A126h	SCI9	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK
0008 A127h	SCI9	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK
0008 A128h	SCI9	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK
0008 A129h	SCI9	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ah	SCI9	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK
0008 A12Bh	SCI9	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK
0008 A12Ch	SCI9	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK
0008 A12Dh	SCI9	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK
0008 B000h	CAC	CAC control register 0	CACR0	8	8	2, 3 PCLKB	2 ICLK
0008 B001h	CAC	CAC control register 1	CACR1	8	8	2, 3 PCLKB	2 ICLK
0008 B002h	CAC	CAC control register 2	CACR2	8	8	2, 3 PCLKB	2 ICLK
0008 B003h	CAC	CAC interrupt control register	CAICR	8	8	2, 3 PCLKB	2 ICLK
0008 B004h	CAC	CAC status register	CASTR	8	8	2, 3 PCLKB	2 ICLK
0008 B006h	CAC	CAC upper-limit value setting register	CAULVR	16	16	2, 3 PCLKB	2 ICLK
0008 B008h	CAC	CAC lower-limit value setting register	CALLVR	16	16	2, 3 PCLKB	2 ICLK
0008 B00Ah	CAC	CAC counter buffer register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK
0008 B080h	DOC	DOC control register	DOCR	8	8	2, 3 PCLKB	2 ICLK
0008 B082h	DOC	DOC data input register	DODIR	16	16	2, 3 PCLKB	2 ICLK
0008 B084h	DOC	DOC data setting register	DODSR	16	16	2, 3 PCLKB	2 ICLK
0008 B100h	ELC	Event link control register	ELCR	8	8	2, 3 PCLKB	2 ICLK
0008 B101h	ELC	Event link setting register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK
0008 B102h	ELC	Event link setting register 1	ELSR1	8	8	2, 3 PCLKB	2 ICLK
0008 B103h	ELC	Event link setting register 2	ELSR2	8	8	2, 3 PCLKB	2 ICLK
0008 B104h	ELC	Event link setting register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK
0008 B105h	ELC	Event link setting register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK
0008 B106h	ELC	Event link setting register 5	ELSR5	8	8	2, 3 PCLKB	2 ICLK
0008 B108h	ELC	Event link setting register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK
0008 B10Bh	ELC	Event link setting register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK
0008 B10Dh	ELC	Event link setting register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK
0008 B10Fh	ELC	Event link setting register 14	ELSR14	8	8	2, 3 PCLKB	2 ICLK
0008 B111h	ELC	Event link setting register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK
0008 B113h	ELC	Event link setting register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK
0008 B114h	ELC	Event link setting register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK
0008 B115h	ELC	Event link setting register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK
0008 B116h	ELC	Event link setting register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK
0008 B117h	ELC	Event link setting register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK
0008 B118h	ELC	Event link setting register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK
0008 B119h	ELC	Event link setting register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK
0008 B11Ah	ELC	Event link setting register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK

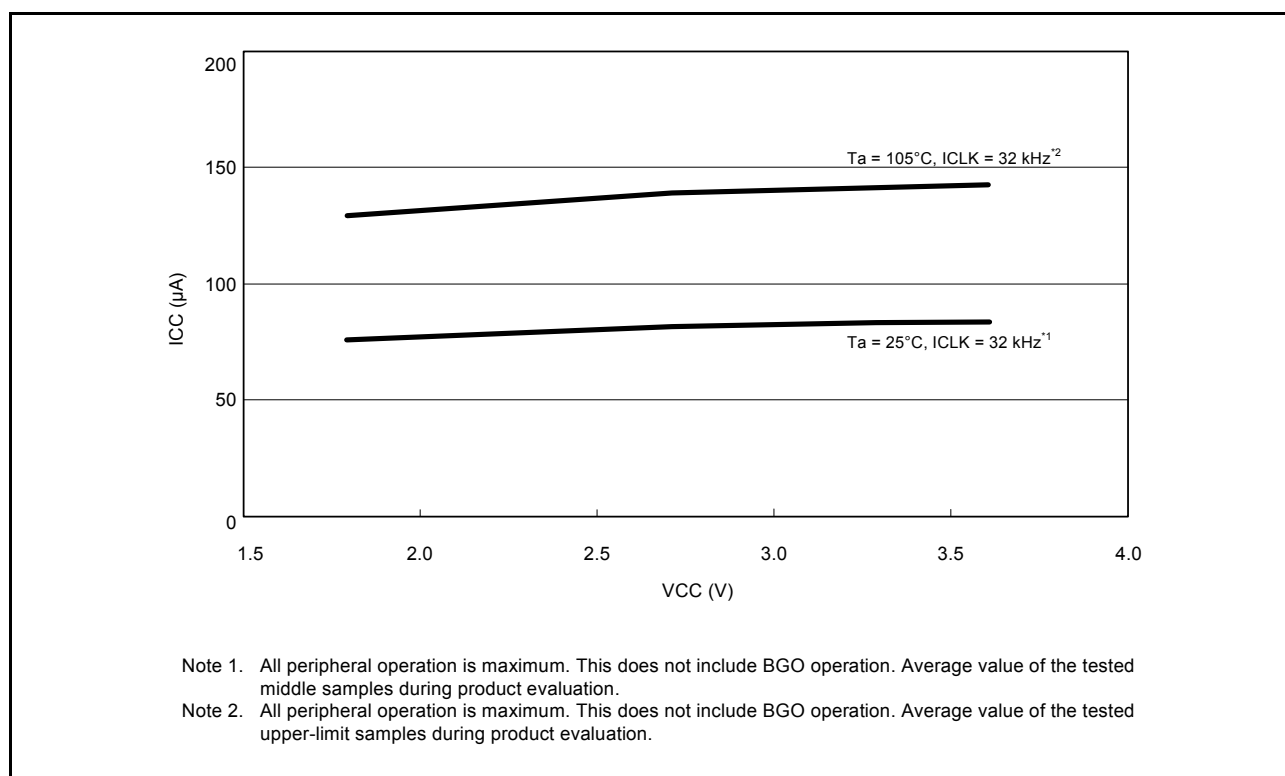


Figure 5.5 Voltage Dependency in Low-Speed Operating Mode 2 (Reference Data)

Table 5.8 DC Characteristics (7)

Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 1.8$ to 3.6 V, $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V,
 $T_a = -40$ to $+105^\circ\text{C}$

Item				Symbol	Typ.*3	Max.	Unit	Test Conditions			
Supply current**1	Software standby mode*2	Flash memory power supplied, HOCO power supplied, POR low power consumption function disabled (SOFTCUT[2:0] bits = 000b)	T _a = 25°C	I _{CC}	10	20	μA				
			T _a = 55°C		12	41					
			T _a = 85°C		18	113					
			T _a = 105°C		29	233					
		Flash memory power supplied, HOCO power not supplied, POR low power consumption function enabled (SOFTCUT[2:0] bits = 110b)	T _a = 25°C		1.7	7.9					
			T _a = 55°C		2.7	25					
			T _a = 85°C		7.0	86					
			T _a = 105°C		16	189					
	Deep software standby mode*2	Flash memory power not supplied, HOCO power not supplied, POR low power consumption function enabled	T _a = 25°C		0.3	0.8					
			T _a = 55°C		0.4	1.1					
			T _a = 85°C		0.8	2.2					
			T _a = 105°C		1.3	4.7					
	Increments produced by running voltage detection circuits and disabling the POR low power consumption function				1.2	—					
	Increment for RTC operation (low CL)				0.6	—					
	Increment for RTC operation (standard CL)				1.4	—					

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDG and LVD are stopped.

Note 3. $V_{CC} = 3.3$ V.

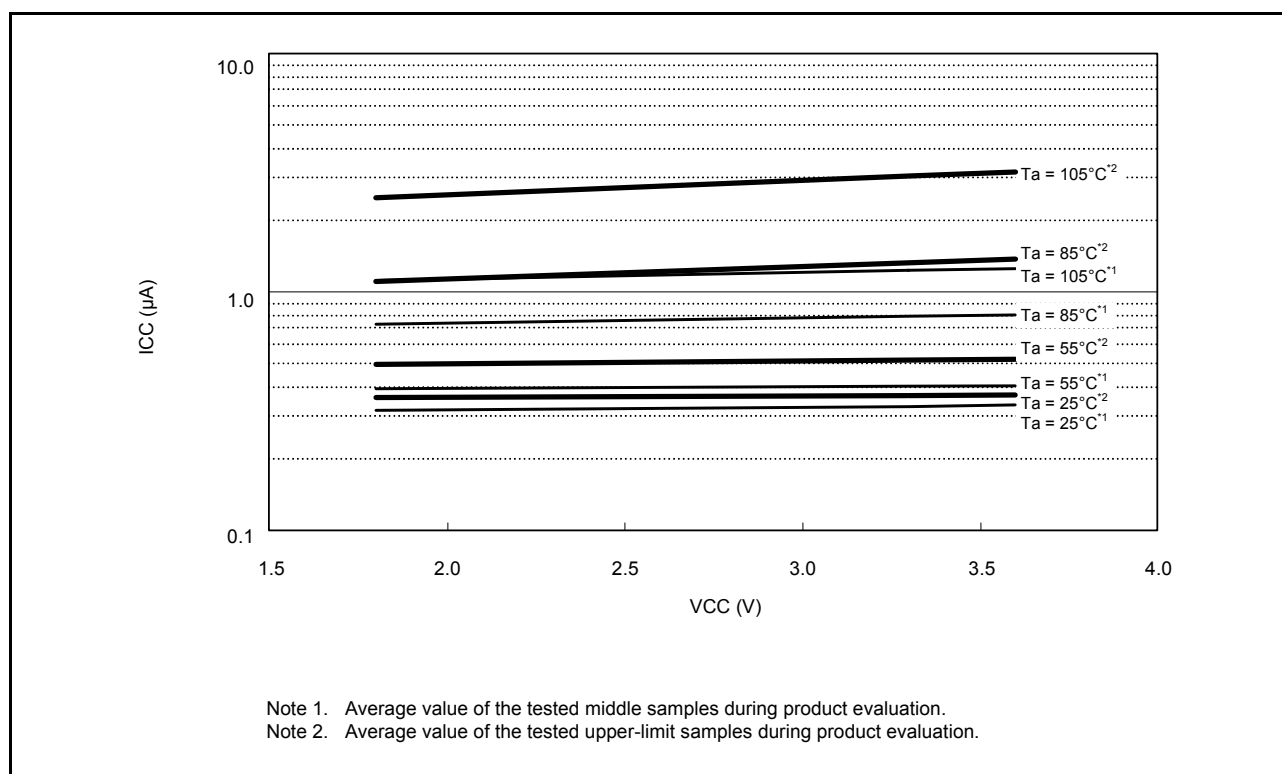


Figure 5.8 Voltage Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data)

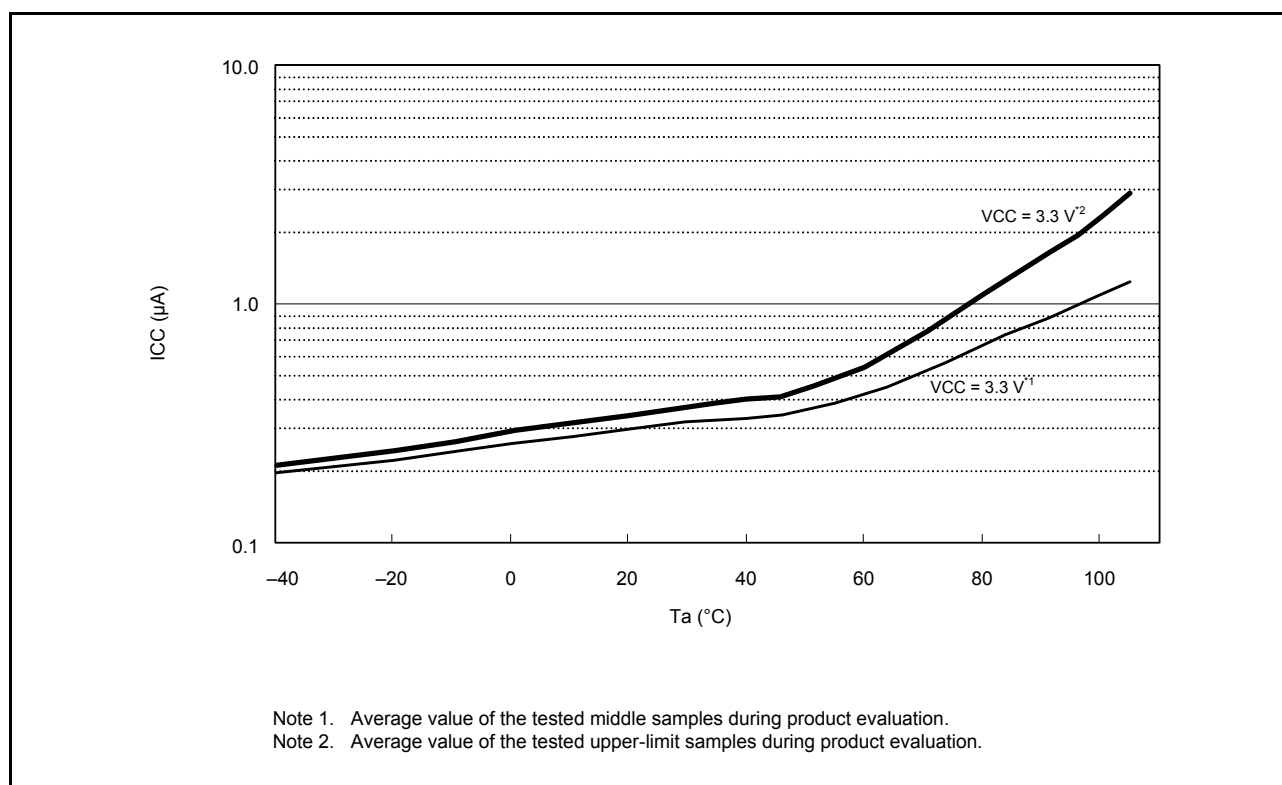


Figure 5.9 Temperature Dependency in Deep Software Standby Mode (DEEPCUT1 Bit = 1) (Reference Data)

Table 5.9 DC Characteristics (8)Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	P_d	—	350	mW	$T_a = -40$ to 85°C
		—	150		$85^\circ\text{C} < T_a \leq 105^\circ\text{C}$

Note: • Please contact Renesas Electronics sales office for derating of operation under $T_a = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Note 1. Total power dissipated by the entire chip (including output currents)

Table 5.10 DC Characteristics (9)Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 1.8$ to 3.6 V, $V_{REFH} = 1.8$ to AV_{CC0} , $V_{REFH0} = 1.8$ to AV_{CC0} , $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V, $T_a = -40$ to $+105^\circ\text{C}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion	Conversion time = 2 μs	I _{AVCC0}	—	0.65	1.1	mA	
	Temperature sensor enabled while waiting for A/D conversion			—	60	150	μA	
	During D/A conversion (per channel)		I _{VREFH} *1	—	0.25	0.45	mA	
	Waiting for A/D, D/A conversion (all units)*2		—	—	0.2	2.0	μA	
Reference power supply current	During A/D conversion	Conversion time = 2 μs	I _{VREFH0}	—	0.05	0.1	mA	
	Waiting for A/D conversion			—	0.2	0.4	μA	

Note: • The values for A/D conversion apply when the sample and hold circuit is not in use.

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. The values are the sum of I_{AVCC0} and I_{REFH} .

Table 5.11 DC Characteristics (10)Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 2.7$ to 3.6 V, $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V, $T_a = -40$ to $+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current	During $\Delta\Sigma$ A/D conversion (per channel)	AI_{CCA}	—	0.9	1.4	mA	
	$\Delta\Sigma$ A/D bias circuit operating current		—	90	130	μA	
	When $\Delta\Sigma$ A/D conversion is stopped (all units)		—	0.07	1.8		

Table 5.12 DC Characteristics (11)Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 1.8$ to 3.6 V, $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V, $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 5.13 DC Characteristics (12)Conditions: $V_{CC} = AV_{CC0} = AV_{CCA} = 0$ to 3.6 V, $V_{REFH} = V_{REFH0} = 0$ to AV_{CC0} , $V_{SS} = AV_{SS0} = AV_{SSA} = V_{REFL} = V_{REFL0} = V_{REFDSL} = 0$ V, $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising gradient	SrV_{CC}	0.02	—	20	ms/V	At cold start

5.2.1 Standard I/O Pin Output Characteristics (1)

Figure 5.11 to Figure 5.15 show the characteristics when normal output is selected by the drive capacity control register.

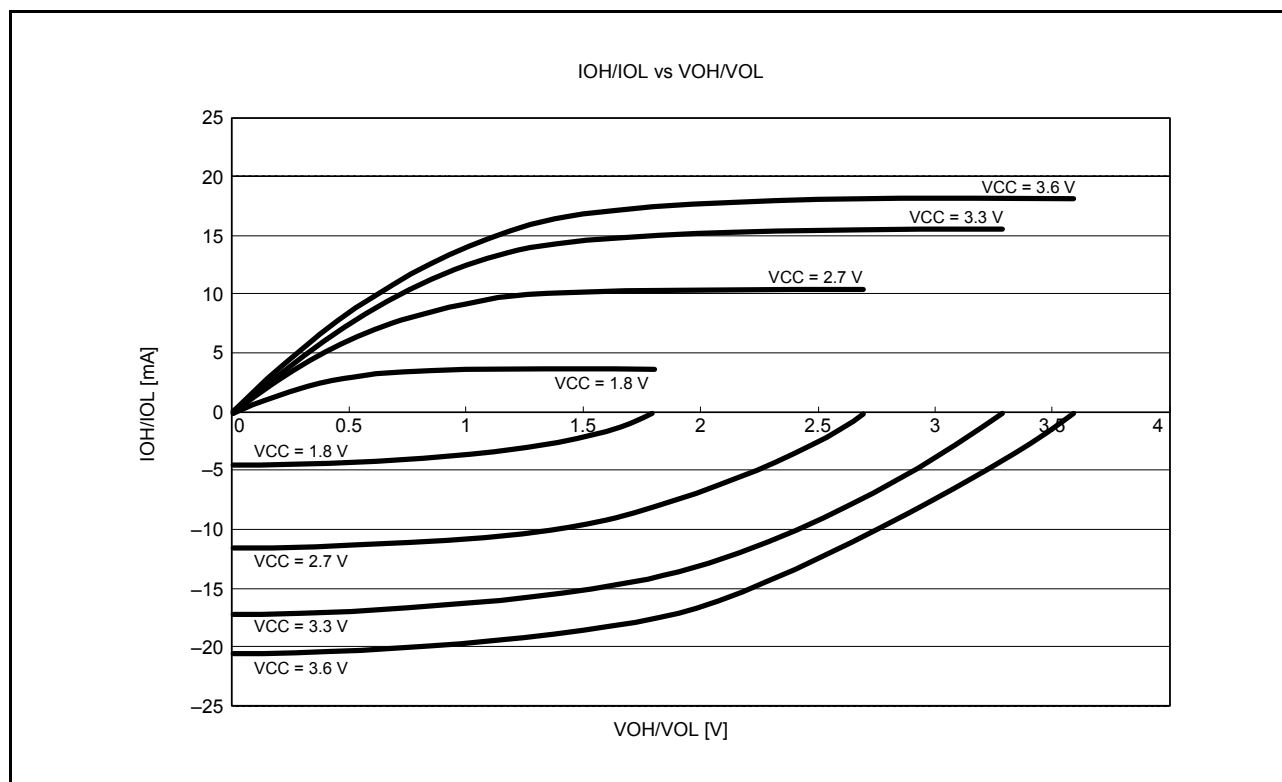


Figure 5.11 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when Normal Output is Selected (Reference Data)

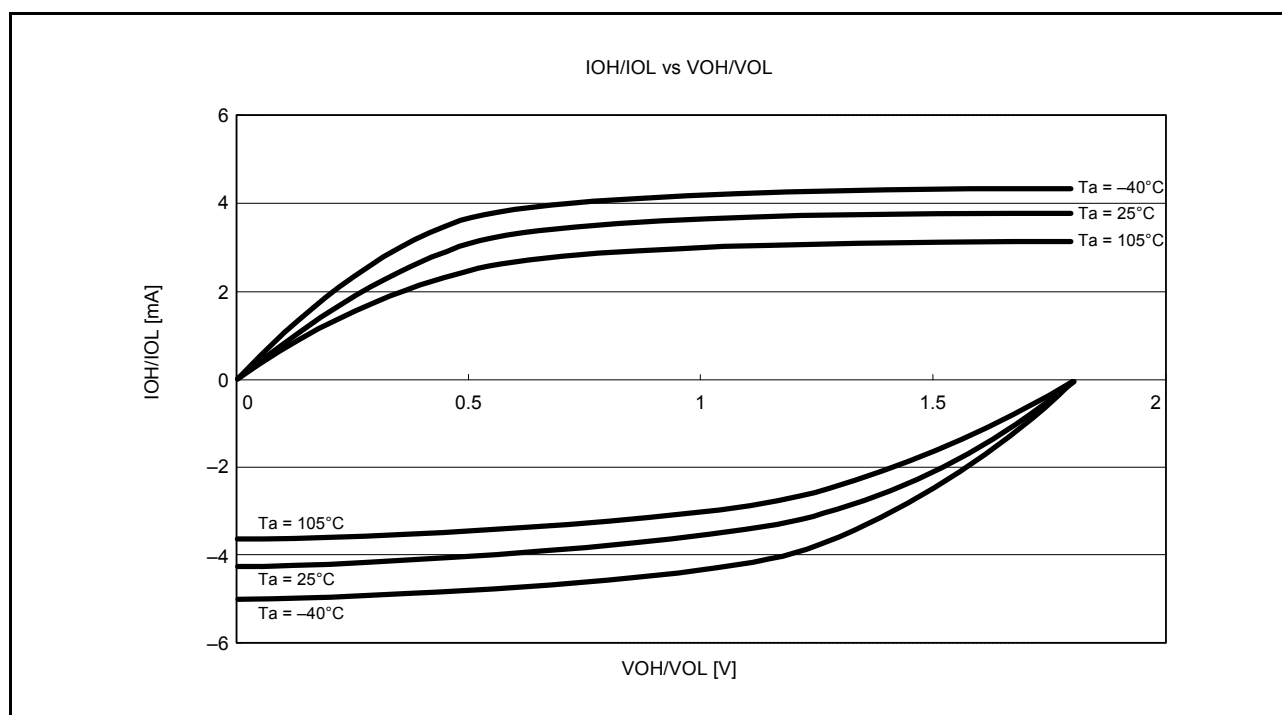


Figure 5.12 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when Normal Output is Selected (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.20 show the characteristics when high-drive output is selected by the drive capacity control register.

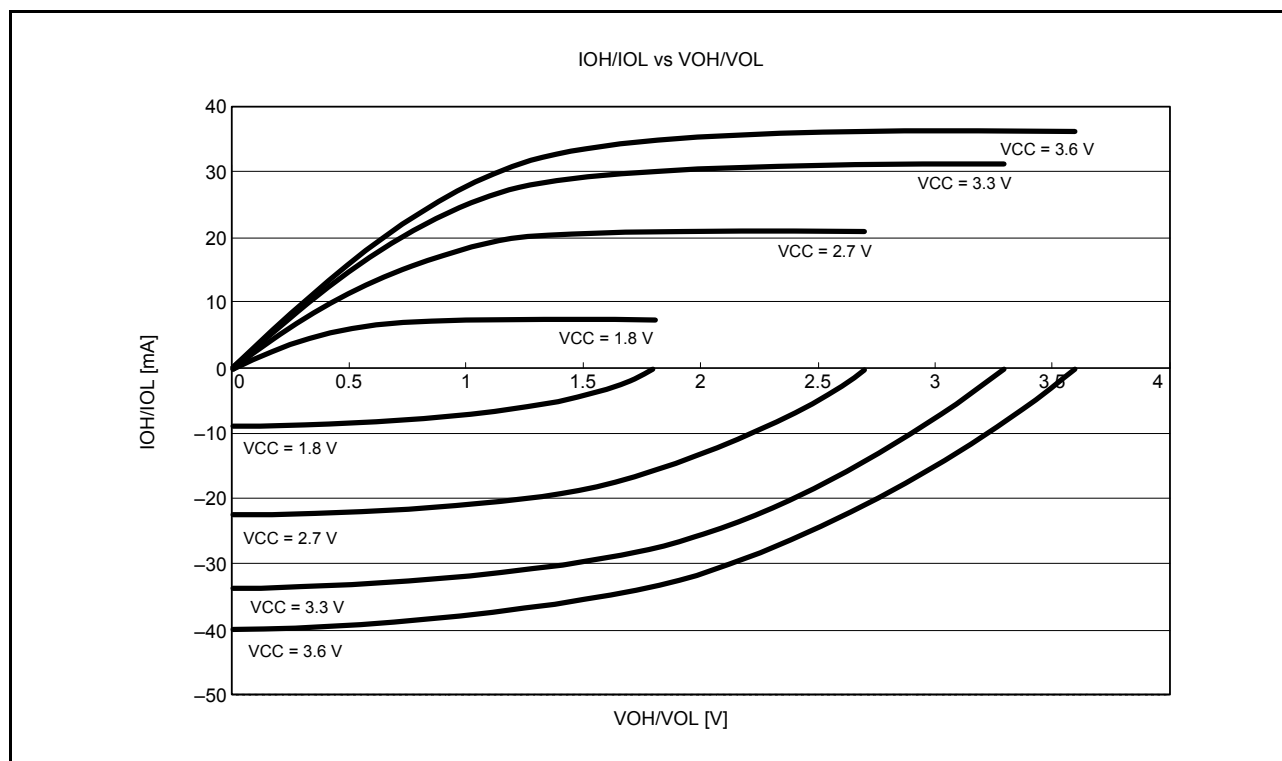


Figure 5.16 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)

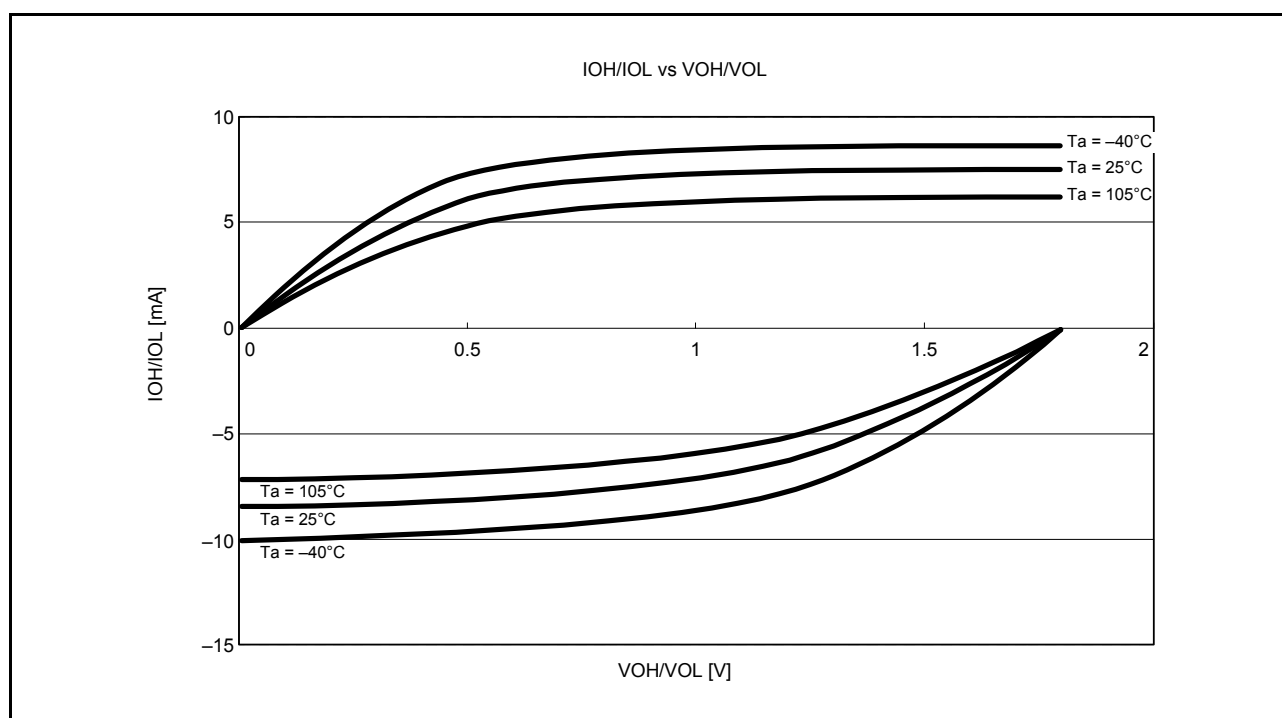


Figure 5.17 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when High-Drive Output is Selected (Reference Data)

5.2.3 RIIC Pin Output Characteristics

Figure 5.21 to Figure 5.24 show the output characteristics of the RIIC pin.

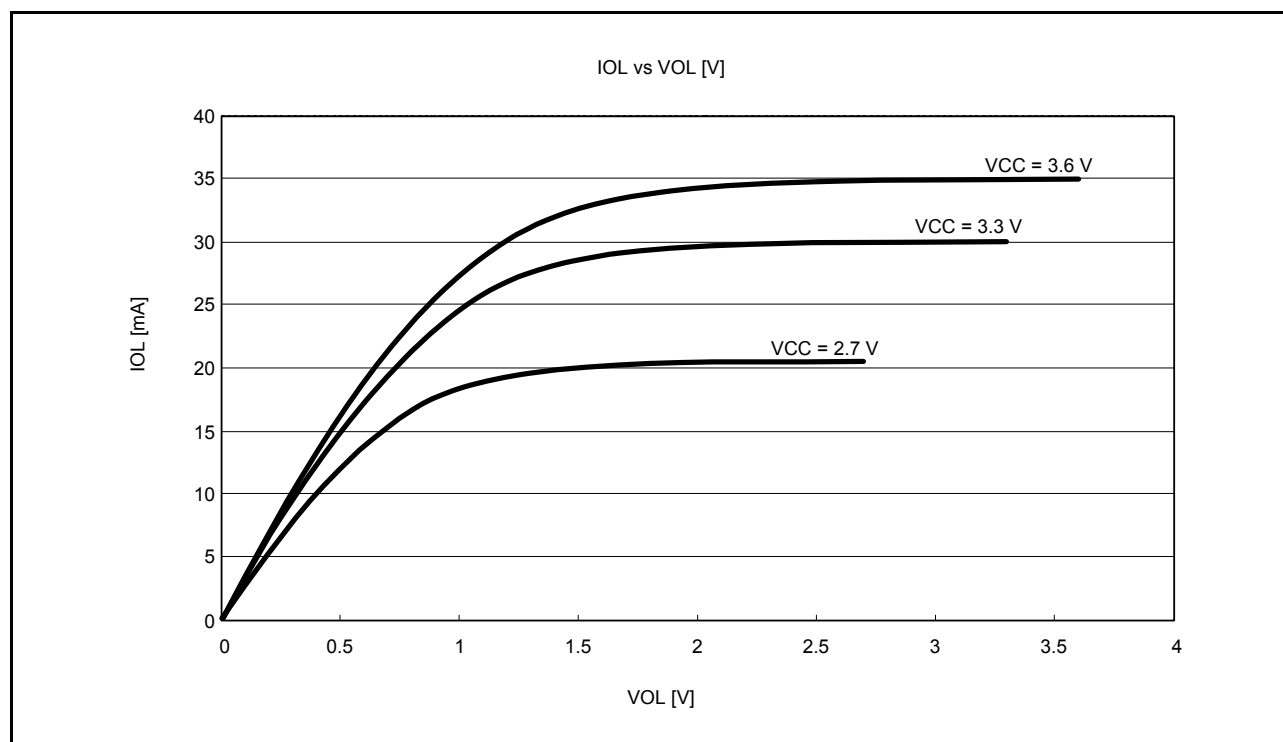


Figure 5.21 VOH and IOL Voltage Characteristics of RIIC Output Pin at $T_a = 25^\circ\text{C}$ (Reference Data)

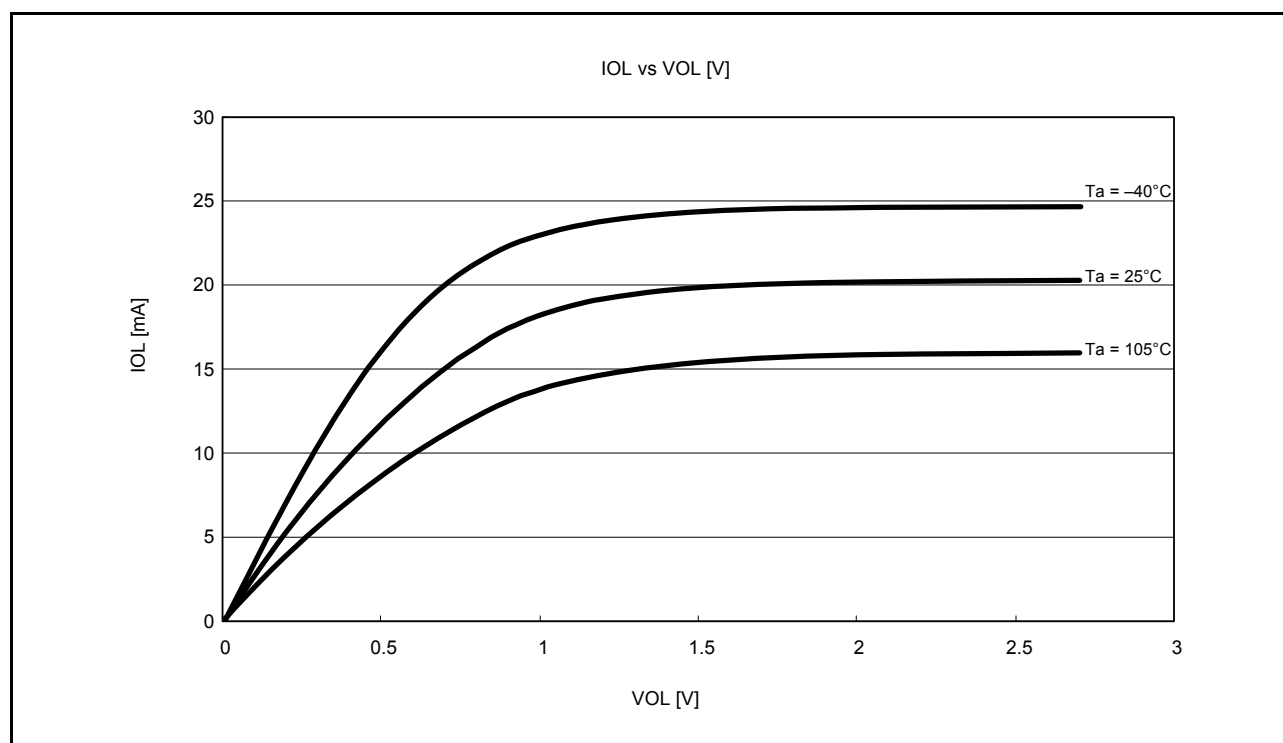


Figure 5.22 VOH and IOL Temperature Characteristics of RIIC Output Pin at $V_{CC} = 2.7\text{ V}$ (Reference Data)

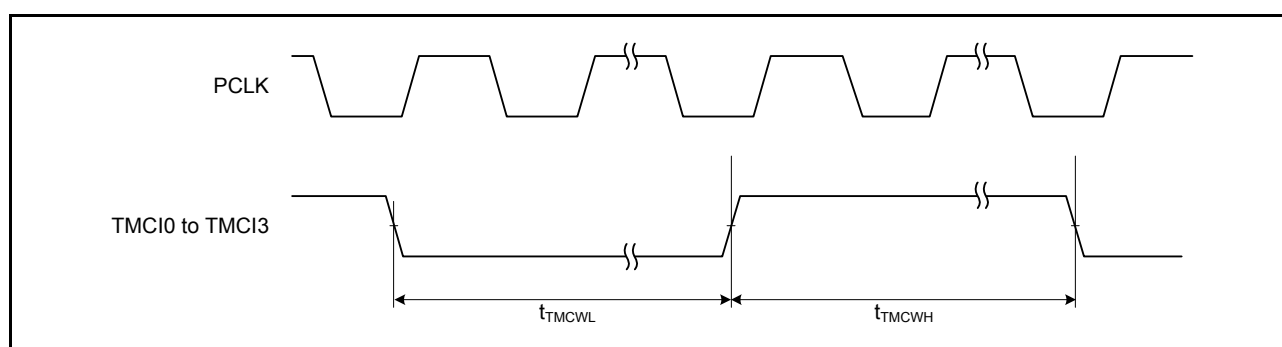


Figure 5.45 8-Bit Timer Clock Input Timing

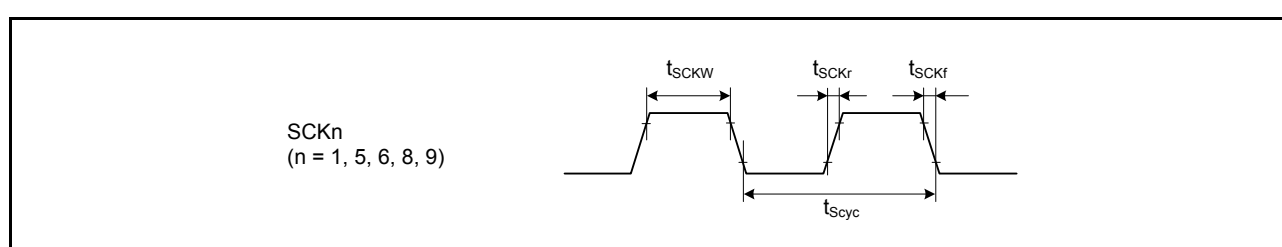


Figure 5.46 SCK Clock Input Timing

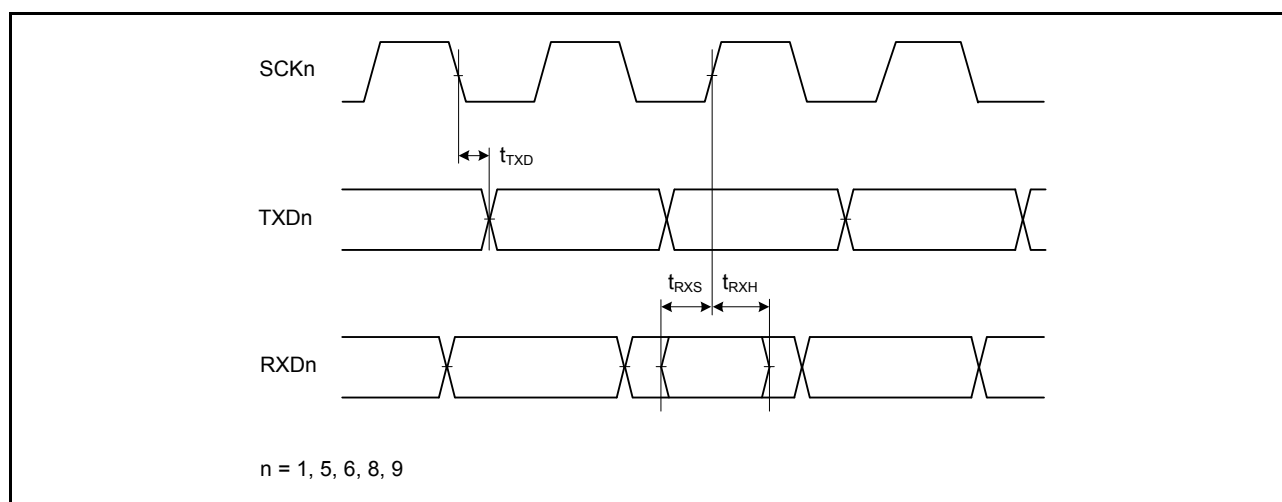


Figure 5.47 SCI Input/Output Timing: Clock Synchronous Mode

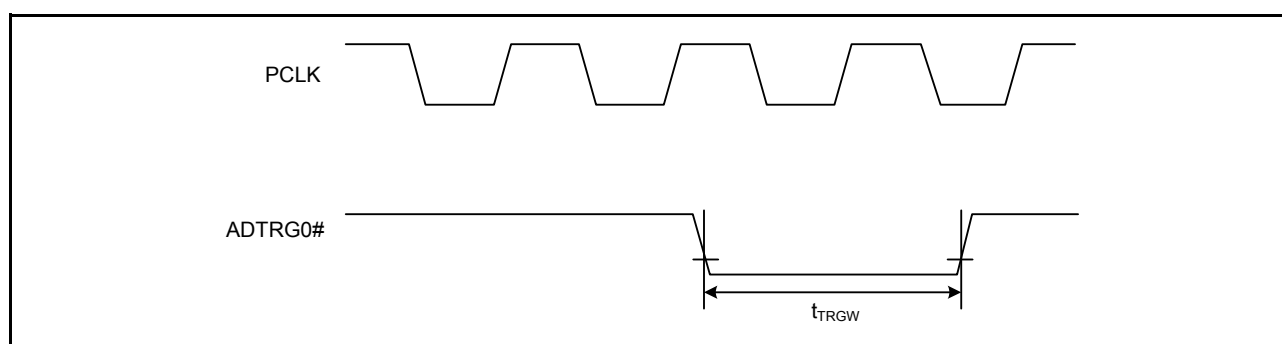


Figure 5.48 A/D Converter External Trigger Input Timing

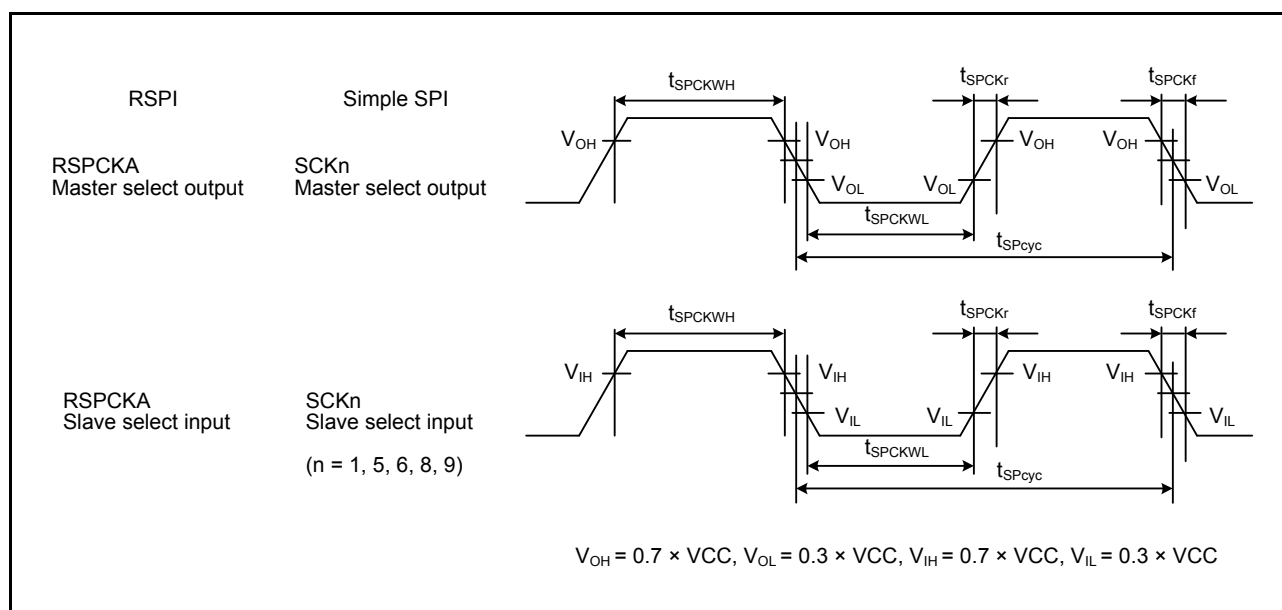


Figure 5.49 RSPCKA Clock Timing and Simple SPI Clock Timing

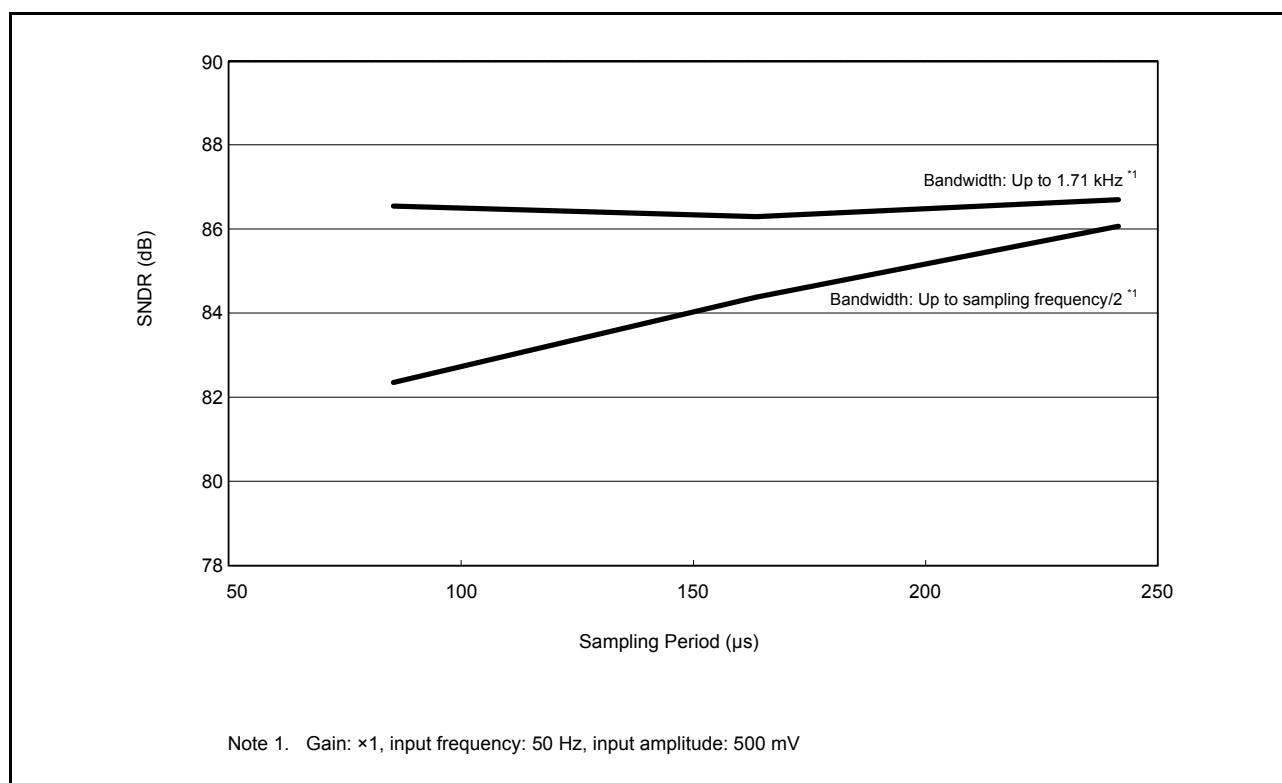


Figure 5.58 Sampling Period Dependency of SNDR (Reference Data)

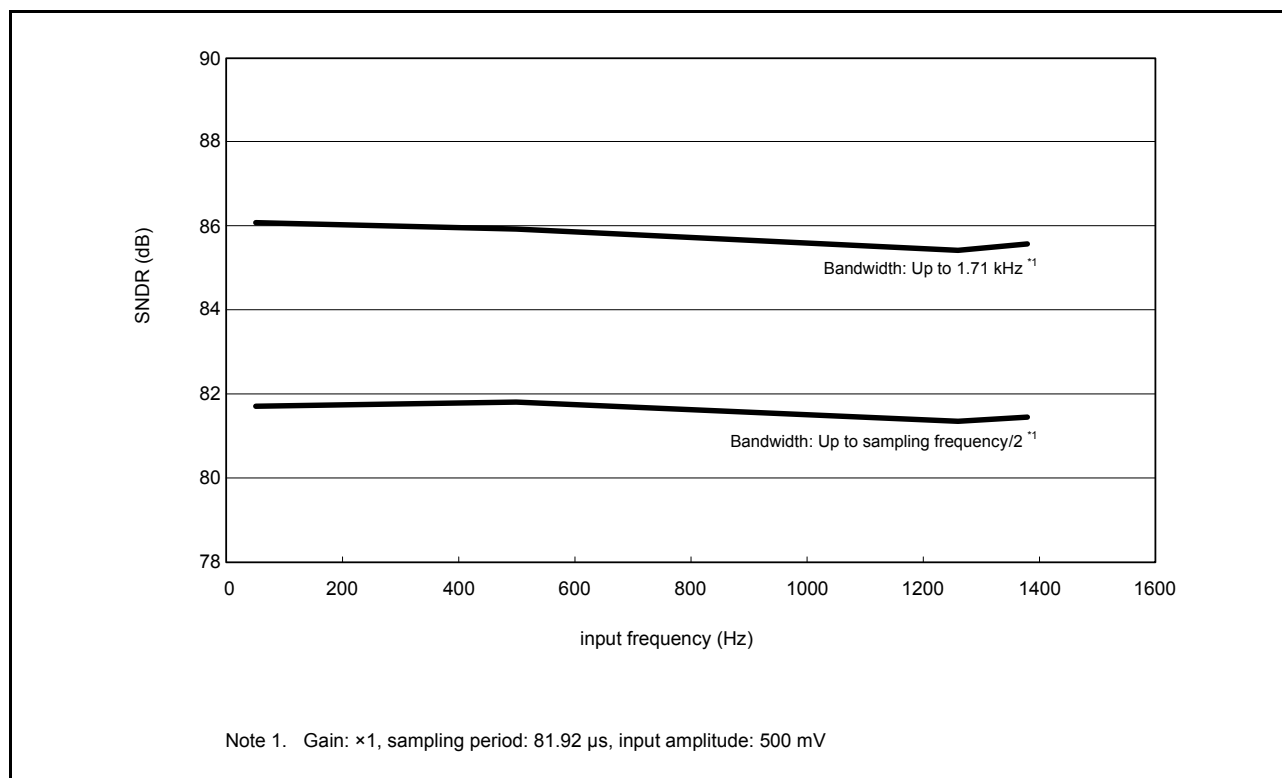


Figure 5.59 Input Frequency Dependency of SNDR (Reference Data)

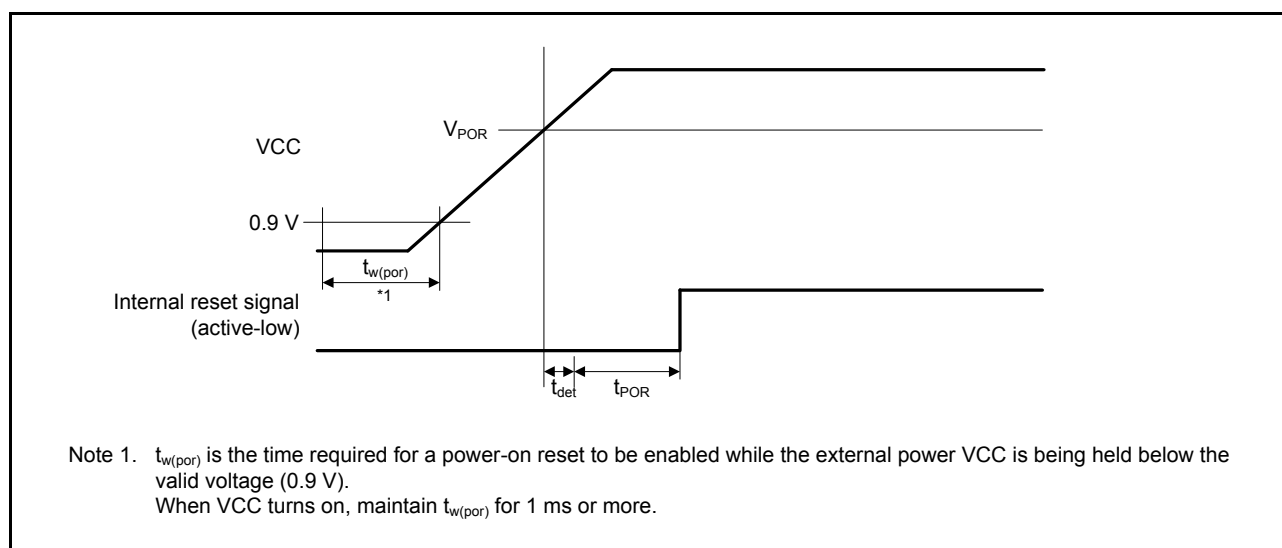


Figure 5.65 Power-on Reset Timing

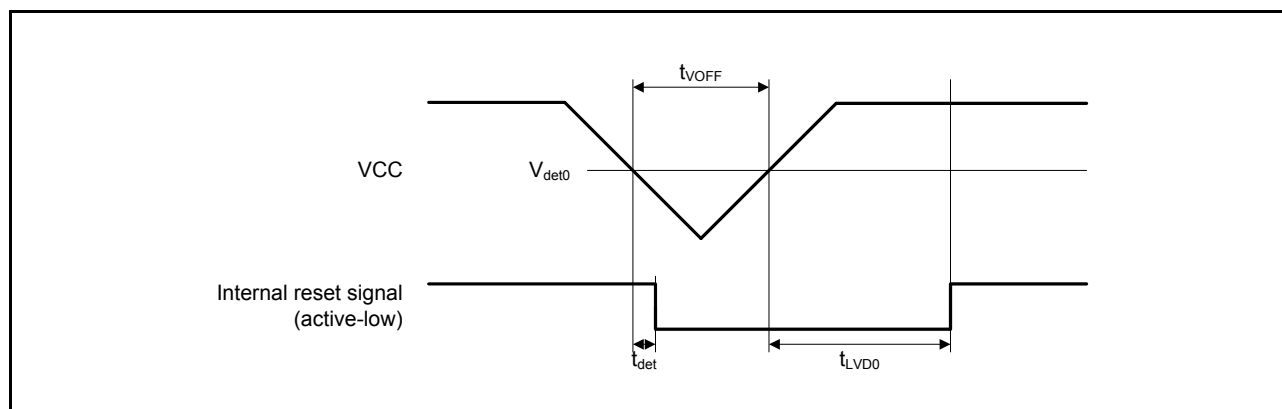


Figure 5.66 Voltage Detection Circuit Timing (V_{det0})

5.11 Oscillation Stop Detection Timing

Table 5.46 Oscillation Stop Detection Circuit Characteristics

Conditions: $V_{CC} = AVCC0 = AVCCA = 1.8$ to 3.6 V, $V_{SS} = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0$ V,
 $T_a = -40$ to $+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.69

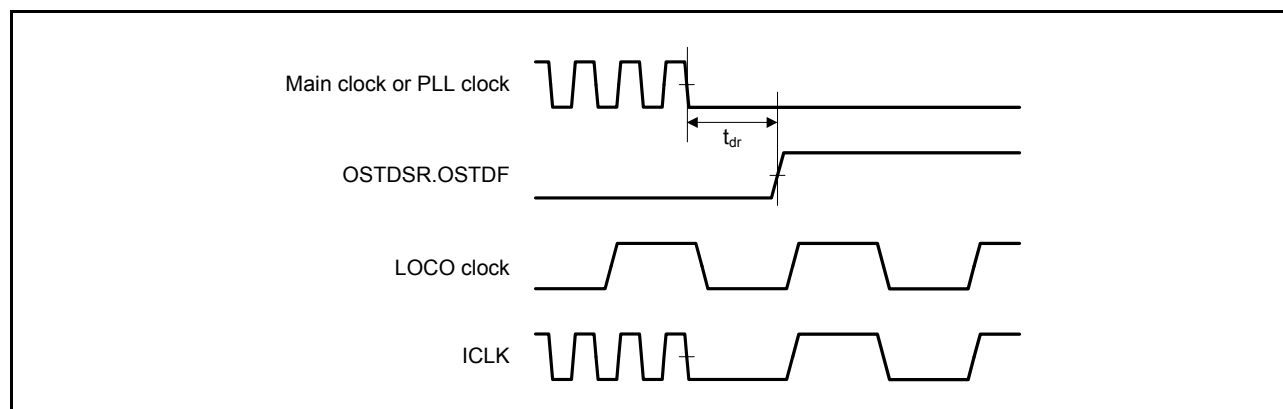


Figure 5.69 Oscillation Stop Detection Timing

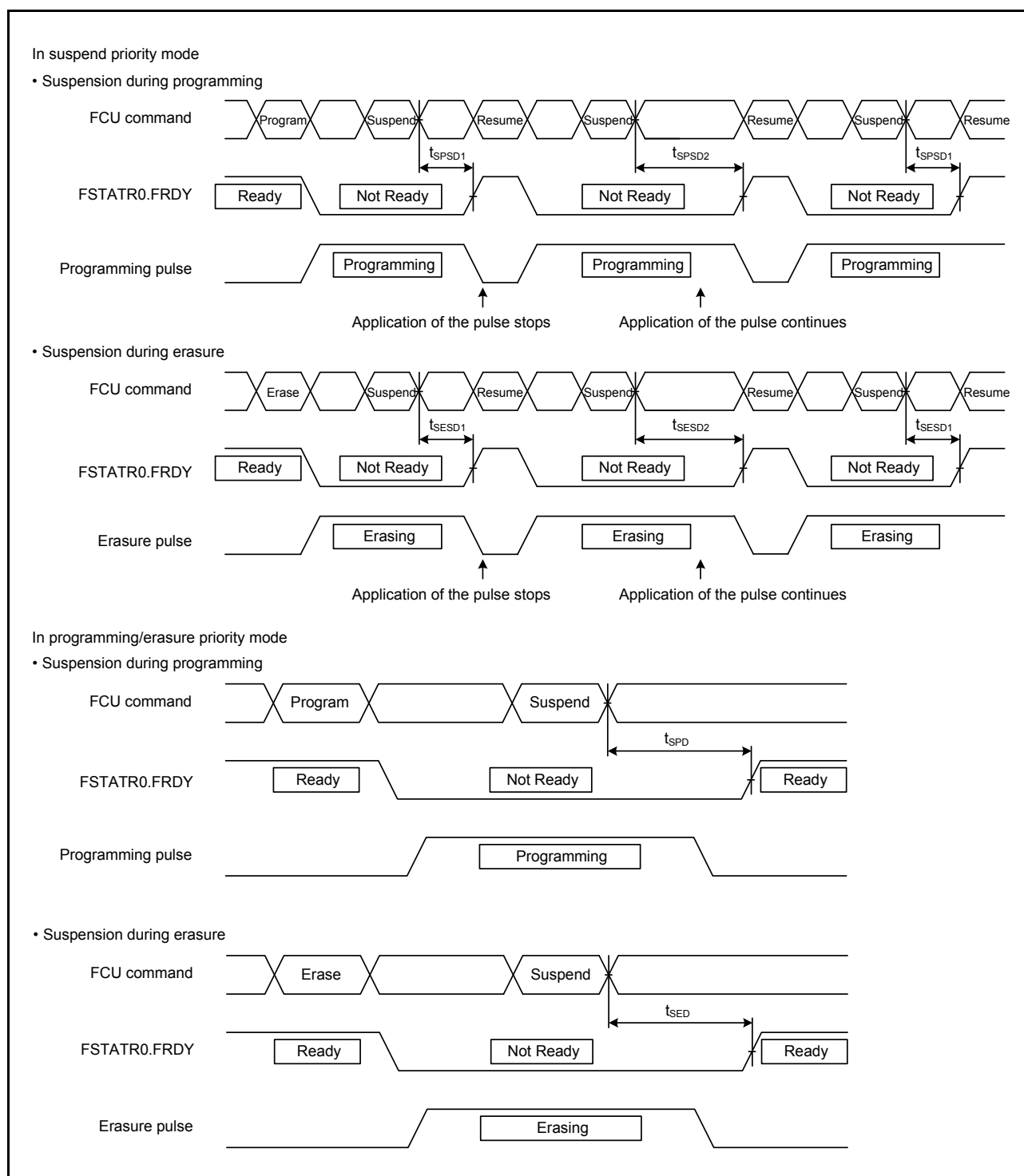


Figure 5.70 Flash Memory Program/Erase Suspend Timing

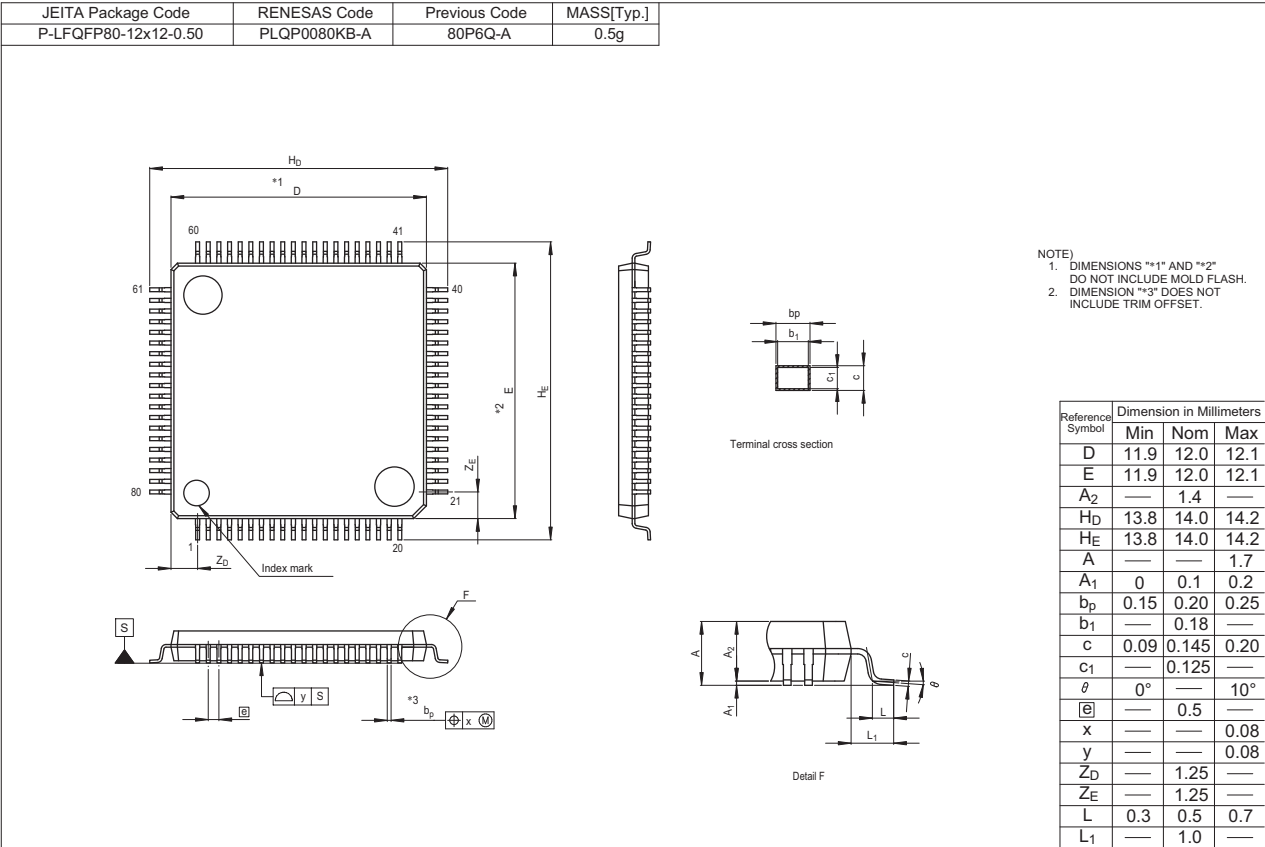


Figure B 80-Pin LQFP (PLQP0080KB-A)

REVISION HISTORY	RX21A Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 24, 2012	—	First edition, issued