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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16K x 8 |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151ret6 |

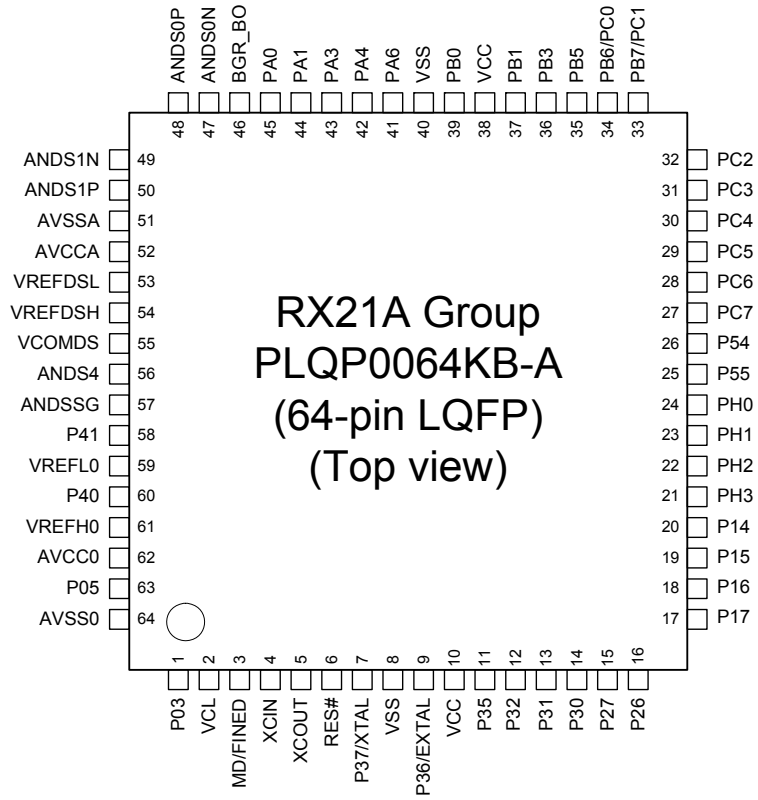
# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 shows the outline of the specifications and Table 1.2 shows the comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 50 MHz<br>• 32-bit RX CPU<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set<br>General purpose: Sixteen 32-bit registers<br>Control: Eight 32-bit registers<br>Accumulator: One 64-bit register<br>• Basic instructions: 73<br>• DSP instructions: 9<br>• Addressing modes: 10<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits<br>• Memory protection unit (MPU) |
| Memory | ROM | • Capacity: 256 K/384 K/512 Kbytes<br>• 50 MHz, no-wait memory access<br>• On-board programming: 3 types |
| | RAM | • Capacity:32 K/64 Kbytes<br>• 50 MHz, no-wait memory access |
| | E2 DataFlash | • Capacity: 8 Kbytes<br>• Number of times for programming/erasing: 100,000 |
| MCU operating mode | | Single-chip mode |
| Clock | Clock generation circuit | • Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator<br>• Oscillation stop detection<br>• Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC)<br>• Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK)<br>The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 50 MHz (at max.)<br>Peripheral modules run in synchronization with the peripheral module clock (PCLK):25 MHz (at max.)<br>The flash peripheral circuit runs in synchronization with the flash peripheral clock (FCLK): 25 MHz (at max.) |
| Reset | | RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset |
| Voltage detection | Voltage detection circuit (LVDAa) | • When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated.<br>Voltage detection circuit 0 is capable of selecting the detection voltage from 2 levels<br>Voltage detection circuit 1 is capable of selecting the detection voltage from 9 levels<br>Voltage detection circuit 2 is capable of selecting the detection voltage from 9 levels |
| Low power consumption | Low power consumption facilities | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| | Function for lower operating power consumption | High-speed operating mode, middle-speed operating mode 1A, middle-speed operating mode 1B, middle-speed operating mode 2A, middle-speed operating mode 2B, low-speed operating mode 1, low-speed operating mode 2 |
| Interrupt | Interrupt controller (ICUb) | • Interrupt vectors: 122<br>• External interrupts: 9 (NMI and IRQ0 to IRQ7 pins)<br>• Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt)<br>• 16 levels specifiable for the order of priority |




Note: • This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LQFP)”.

**Figure 1.5 Pin Assignments of the 64-Pin LQFP**

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 2)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| 42 | | PB6 | MTIOC3D | RXD9/SMISO9/SSCL9 | |
| 43 | | PB5 | MTIOC2A/MTIOC1B/TMRI1/ POE1# | SCK9 | |
| 44 | | PB4 | | CTS9#/RTS9#/SS9# | |
| 45 | | PB3 | MTIOC0A/MTIOC4A/TMO0/ POE3# | SCK6 | |
| 46 | | PB2 | | CTS6#/RTS6#/SS6# | |
| 47 | | PB1 | MTIOC0C/MTIOC4C/TMCI0 | TXD6/SMOSI6/SSDA6 | IRQ4-DS |
| 48 | VCC | | | | |
| 49 | | PB0 | MTIC5W | RXD6/SMISO6/SSCL6/RSPCKA | CMPB0 |
| 50 | VSS | | | | |
| 51 | | PA6 | MTIC5V/MTCLKB/TMCI3/ POE2# | CTS5#/RTS5#/SS5#/MOSIA | CVREFB0 |
| 52 | | PA5 | | RSPCKA | |
| 53 | | PA4 | MTIC5U/MTCLKA/TMRI0 | TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0 | IRQ5-DS/CVREFB1 |
| 54 | | PA3 | MTIOC0D/MTCLKD | RXD5/SMISO5/SSCL5/IRRXD5 | IRQ6-DS/CMPB1 |
| 55 | | PA2 | | RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3 | CMPA2 |
| 56 | | PA1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | CVREFA |
| 57 | | PA0 | MTIOC4A | SSLA1 | CACREF/CMPA1 |
| 58 | BGR_BO | | | | |
| 59 | | | | | ANDS0N |
| 60 | | | | | ANDS0P |
| 61 | | | | | ANDS1N |
| 62 | | | | | ANDS1P |
| 63 | AVSSA | | | | |
| 64 | AVCCA | | | | |
| 65 | VREFDSL | | | | |
| 66 | VREFDSH | | | | |
| 67 | VCOMDS | | | | |
| 68 | | | | | ANDS4 |
| 69 | | | | | ANDS5 |
| 70 | ANDSSG | | | | |
| 71 | | P43 | | | AN3 |
| 72 | | P42 | | | AN2 |
| 73 | | P41 | | | AN1 |
| 74 | VREFL0 | | | | |
| 75 | | P40 | | | AN0 |
| 76 | VREFH0 | | | | |
| 77 | AVCC0 | | | | |
| 78 | | P07 | | | AN6/ADTRG0# |
| 79 | AVSS0 | | | | |
| 80 | | P05 | | | AN5/DA1 |

Note: • Pin names to which –DS is appended are for pins that can be used to trigger release from deep software standby mode.

**Table 1.8 List of Pins and Pin Functions (100-Pin TFLGA) (1 / 3)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (MTU, TMR, POE) | Communications (SCIc, RSPI, RIIC) | Others |
|---|---|---|---|---|---|
| A1 | | P05 | | | AN5/DA1 |
| A2 | VREFH | | | | |
| A3 | | P07 | | | AN6/ADTRG0# |
| A4 | VREFL0 | | | | |
| A5 | | P43 | | | AN3 |
| A6 | VCOMDS | | | | |
| A7 | AVSSA | | | | |
| A8 | | | | | ANDS2N |
| A9 | | | | | ANDS1P |
| A10 | | | | | ANDS1N |
| B1 | | P03 | | | AN4/DA0 |
| B2 | AVSS0 | | | | |
| B3 | AVCC0 | | | | |
| B4 | | P40 | | | AN0 |
| B5 | ANDSSG | | | | |
| B6 | VREFDSH | | | | |
| B7 | AVCCA | | | | |
| B8 | | | | | ANDS3N |
| B9 | | | | | ANDS2P |
| B10 | | | | | ANDS0P |
| C1 | VCL | | | | |
| C2 | VREFL | | | | |
| C3 | | PJ3 | MTIOC3C | CTS6#/RTS6#/SS6# | |
| C4 | VREFH0 | | | | |
| C5 | | P42 | | | AN2 |
| C6 | | | | | ANDS4 |
| C7 | VREFDSL | | | | |
| C8 | | | | | ANDS3P |
| C9 | BGR_BO | | | | |
| C10 | | | | | ANDS0N |
| D1 | XCIN | | | | |
| D2 | XCOUT | | | | |
| D3 | MD | | | | FINED |
| D4 | | PJ1 | MTIOC3A | | |
| D5 | | | | | ANDS6 |
| D6 | | | | | ANDS5 |
| D7 | | PE6 | | MOSIB | IRQ6 |
| D8 | | PE7 | | MISOB | IRQ7-DS |
| D9 | | PA1 | MTIOC0B/MTCLKC | SCK5/SSLA2 | CVREFA |
| D10 | | PA0 | MTIOC4A | SSLA1 | CACREF/CMPA1 |
| E1 | XTAL | P37 | | | |
| E2 | VSS | | | | |
| E3 | RES# | | | | |
| E4 | | P34 | MTIOC0A/TMCI3/POE2# | SCK6 | IRQ4 |
| E5 | | P41 | | | AN1 |

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

This CPU has the following eight control registers.

### (1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

## 2.3 Register Associated with DSP Instructions

### (1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory map.

# 4. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

## (1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

## (2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

**[Examples of cases requiring special care]**

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERn of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

(a) Write to an I/O register.
(b) Read the value from the I/O register to a general register.
(c) Execute the operation using the value read.
(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

**Table 4.1 List of I/O Registers (Address Order) (9 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 73E2h | ICU | Interrupt source priority register 226 | IPR226 | 8 | 8 | | 2 ICLK |
| 0008 73E6h | ICU | Interrupt source priority register 230 | IPR230 | 8 | 8 | | 2 ICLK |
| 0008 73EAh | ICU | Interrupt source priority register 234 | IPR234 | 8 | 8 | | 2 ICLK |
| 0008 73F6h | ICU | Interrupt source priority register 246 | IPR246 | 8 | 8 | | 2 ICLK |
| 0008 73F7h | ICU | Interrupt source priority register 247 | IPR247 | 8 | 8 | | 2 ICLK |
| 0008 73F8h | ICU | Interrupt source priority register 248 | IPR248 | 8 | 8 | | 2 ICLK |
| 0008 73F9h | ICU | Interrupt source priority register 249 | IPR249 | 8 | 8 | | 2 ICLK |
| 0008 73FAh | ICU | Interrupt source priority register 250 | IPR250 | 8 | 8 | | 2 ICLK |
| 0008 73FBh | ICU | Interrupt source priority register 251 | IPR251 | 8 | 8 | | 2 ICLK |
| 0008 73FCh | ICU | Interrupt source priority register 252 | IPR252 | 8 | 8 | | 2 ICLK |
| 0008 73FDh | ICU | Interrupt source priority register 253 | IPR253 | 8 | 8 | | 2 ICLK |
| 0008 7400h | ICU | DMAC activation request select register 0 | DMRSR0 | 8 | 8 | | 2 ICLK |
| 0008 7404h | ICU | DMAC activation request select register 1 | DMRSR1 | 8 | 8 | | 2 ICLK |
| 0008 7408h | ICU | DMAC activation request select register 2 | DMRSR2 | 8 | 8 | | 2 ICLK |
| 0008 740Ch | ICU | DMAC activation request select register 3 | DMRSR3 | 8 | 8 | | 2 ICLK |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | | 2 ICLK |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | | 2 ICLK |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | | 2 ICLK |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | | 2 ICLK |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | | 2 ICLK |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | | 2 ICLK |
| 0008 7510h | ICU | IRQ pin digital filter enable register 0 | IRQFLTE0 | 8 | 8 | | 2 ICLK |
| 0008 7514h | ICU | IRQ pin digital filter setting register 0 | IRQFLTC0 | 16 | 16 | | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | | 2 ICLK |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | | 2 ICLK |
| 0008 7590h | ICU | NMI pin digital filter enable register | NMIFLTE | 8 | 8 | | 2 ICLK |
| 0008 7594h | ICU | NMI pin digital filter setting register | NMIFLTC | 8 | 8 | | 2 ICLK |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8020h | WDT | WDT refresh register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8022h | WDT | WDT control register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8024h | WDT | WDT status register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8026h | WDT | WDT reset control register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (10 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8036h | IWDT | IWDT reset control register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8038h | IWDT | IWDT count stop control register | IWDTCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C0h | DA | D/A data register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C2h | DA | D/A data register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C4h | DA | D/A control register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 80C5h | DA | DADRm format select register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8200h | TMR0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8201h | TMR1 | Timer counter control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8202h | TMR0 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8203h | TMR1 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8204h | TMR0 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8205h | TMR1 | Time constant register A | TCORA | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8206h | TMR0 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8207h | TMR1 | Time constant register B | TCORB | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8208h | TMR0 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8209h | TMR1 | Timer counter | TCNT | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Ah | TMR0 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Bh | TMR1 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 820Ch | TMR0 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8210h | TMR2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8211h | TMR3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8212h | TMR2 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8213h | TMR3 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8214h | TMR2 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8215h | TMR3 | Time constant register A | TCORA | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8216h | TMR2 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8217h | TMR3 | Time constant register B | TCORB | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 8218h | TMR2 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8219h | TMR3 | Timer counter | TCNT | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ah | TMR2 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Bh | TMR3 | Timer counter control register | TCCR | 8 | 8*1 | 2, 3 PCLKB | 2 ICLK |
| 0008 821Ch | TMR2 | Time count start register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 8300h | RIIC0 | $I^2C$ bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8301h | RIIC0 | $I^2C$ bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8302h | RIIC0 | $I^2C$ bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8303h | RIIC0 | $I^2C$ bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8304h | RIIC0 | $I^2C$ bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8305h | RIIC0 | $I^2C$ bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8306h | RIIC0 | $I^2C$ bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8307h | RIIC0 | $I^2C$ bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8308h | RIIC0 | $I^2C$ bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 8309h | RIIC0 | $I^2C$ bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ah | RIIC0 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Bh | RIIC0 | Timeout internal counter U | TMOCNTU | 8 | 8*2 | 2, 3 PCLKB | 2 ICLK |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (16 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 A108h | SCI8 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A109h | SCI8 | I²C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A10Ah | SCI8 | I²C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A10Bh | SCI8 | I²C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A10Ch | SCI8 | I²C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A10Dh | SCI8 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A120h | SCI9 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A121h | SCI9 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A122h | SCI9 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A123h | SCI9 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A124h | SCI9 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A125h | SCI9 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A126h | SCI9 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A127h | SCI9 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A128h | SCI9 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A129h | SCI9 | I²C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A12Ah | SCI9 | I²C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A12Bh | SCI9 | I²C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A12Ch | SCI9 | I²C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 A12Dh | SCI9 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B000h | CAC | CAC control register 0 | CACR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B001h | CAC | CAC control register 1 | CACR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B002h | CAC | CAC control register 2 | CACR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B003h | CAC | CAC interrupt control register | CAICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B004h | CAC | CAC status register | CASTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B006h | CAC | CAC upper-limit value setting register | CAULVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 B008h | CAC | CAC lower-limit value setting register | CALLVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 B00Ah | CAC | CAC counter buffer register | CACNTBR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 B080h | DOC | DOC control register | DOCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B082h | DOC | DOC data input register | DODIR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 B084h | DOC | DOC data setting register | DODSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK |
| 0008 B100h | ELC | Event link control register | ELCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B101h | ELC | Event link setting register 0 | ELSR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B102h | ELC | Event link setting register 1 | ELSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B103h | ELC | Event link setting register 2 | ELSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B104h | ELC | Event link setting register 3 | ELSR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B105h | ELC | Event link setting register 4 | ELSR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B106h | ELC | Event link setting register 5 | ELSR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B108h | ELC | Event link setting register 7 | ELSR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B10Bh | ELC | Event link setting register 10 | ELSR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B10Dh | ELC | Event link setting register 12 | ELSR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B10Fh | ELC | Event link setting register 14 | ELSR14 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B111h | ELC | Event link setting register 16 | ELSR16 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B113h | ELC | Event link setting register 18 | ELSR18 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B114h | ELC | Event link setting register 19 | ELSR19 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B115h | ELC | Event link setting register 20 | ELSR20 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B116h | ELC | Event link setting register 21 | ELSR21 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B117h | ELC | Event link setting register 22 | ELSR22 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B118h | ELC | Event link setting register 23 | ELSR23 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B119h | ELC | Event link setting register 24 | ELSR24 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B11Ah | ELC | Event link setting register 25 | ELSR25 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (18 / 24)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles: ICLK ≥ PCLK | Number of Access Cycles: ICLK < PCLK |
|---|---|---|---|---|---|---|---|
| 0008 B444h | DSAD | ΔΣ A/D data register 3 | DSADDR3 | 32 | 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 B448h | DSAD | ΔΣ A/D input select register 3 | DSADISR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B450h | DSAD | ΔΣ A/D control register 4 | DSADCR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B451h | DSAD | ΔΣ A/D control/status register 4 | DSADCSR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B452h | DSAD | ΔΣ A/D gain select register 4 | DSADGSR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B453h | DSAD | ΔΣ A/D overwrite flag register 4 | DSADFR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B454h | DSAD | ΔΣ A/D data register 4 | DSADDR4 | 32 | 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 B458h | DSAD | ΔΣ A/D input select register 4 | DSADISR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B460h | DSAD | ΔΣ A/D control register 5 | DSADCR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B461h | DSAD | ΔΣ A/D control/status register 5 | DSADCSR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B462h | DSAD | ΔΣ A/D gain select register 5 | DSADGSR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B463h | DSAD | ΔΣ A/D overwrite flag register 5 | DSADFR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B464h | DSAD | ΔΣ A/D data register 5 | DSADDR5 | 32 | 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 B468h | DSAD | ΔΣ A/D input select register 5 | DSADISR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B470h | DSAD | ΔΣ A/D control register 6 | DSADCR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B471h | DSAD | ΔΣ A/D control/status register 6 | DSADCSR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B472h | DSAD | ΔΣ A/D gain select register 6 | DSADGSR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B473h | DSAD | ΔΣ A/D overwrite flag register 6 | DSADFR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 B474h | DSAD | ΔΣ A/D data register 6 | DSADDR6 | 32 | 32 | 2, 3 PCLKB | 2 ICLK |
| 0008 B478h | DSAD | ΔΣ A/D input select register 6 | DSADISR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C000h | PORT0 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C001h | PORT1 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C002h | PORT2 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C003h | PORT3 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C004h | PORT4 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C005h | PORT5 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C00Ah | PORTA | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C00Bh | PORTB | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C00Ch | PORTC | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C00Eh | PORTE | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C011h | PORTH | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C012h | PORTJ | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C020h | PORT0 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C021h | PORT1 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C022h | PORT2 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C023h | PORT3 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C024h | PORT4 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C025h | PORT5 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C02Ah | PORTA | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C02Bh | PORTB | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C02Ch | PORTC | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C02Eh | PORTE | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C031h | PORTH | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C032h | PORTJ | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK |
| 0008 C040h | PORT0 | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |
| 0008 C041h | PORT1 | Port input data register | PIDR | 8 | 8 | 3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing | 3 ICLK cycles when reading, 2 ICLK cycles when writing |

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Low-speed operating mode 1 | Normal operating mode | No peripheral operation*6 | ICLK = 8 MHz | $I_{CC}$ | 1.9 | — | mA | |
| | | | | ICLK = 4 MHz | | 1.2 | — | | |
| | | | All peripheral operation: Normal*7 | ICLK = 8 MHz | | 2.5 | — | | |
| | | | | ICLK = 4 MHz | | 1.7 | — | | |
| | | | All peripheral operation: Max.*8 | ICLK = 8 MHz | | — | 12 | | |
| | | Sleep mode | No peripheral operation | ICLK = 8 MHz | | 1.3 | — | | |
| | | | | ICLK = 4 MHz | | 0.9 | — | | |
| | | | All peripheral operation: Normal | ICLK = 8 MHz | | 1.9 | — | | |
| | | | | ICLK = 4 MHz | | 1.3 | — | | |
| | | All-module clock stop mode | | ICLK = 8 MHz | | 1.1 | — | | |
| | | | | ICLK = 4 MHz | | 0.9 | — | | |
| | Low-speed operating mode 2 | Normal operating mode | No peripheral operation*9 | ICLK = 32 kHz | | 0.027 | — | | |
| | | | All peripheral operation: Normal*10 | ICLK = 32 kHz | | 0.030 | — | | |
| | | | All peripheral operation: Max.*11 | ICLK = 32 kHz | | — | 1.0 | | |
| | | Sleep mode | No peripheral operation | ICLK = 32 kHz | | 0.022 | — | | |
| | | | All peripheral operation: Normal | ICLK = 32 kHz | | 0.025 | — | | |
| | | All-module clock stop mode | | ICLK = 32 kHz | | 0.022 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.
Note 3. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 4. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are set to divided by 64.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are ICLK divided by 1.
Note 6. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 8. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is HOCO. FCLK and PCLK are ICLK divided by 1.
Note 9. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 10. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the sub oscillation circuit. FCLK and PCLK are set to divided by 64.
Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main oscillation circuit. FCLK and PCLK are ICLK divided by 1.

### 5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.16 to Figure 5.20 show the characteristics when high-drive output is selected by the drive capacity control register.

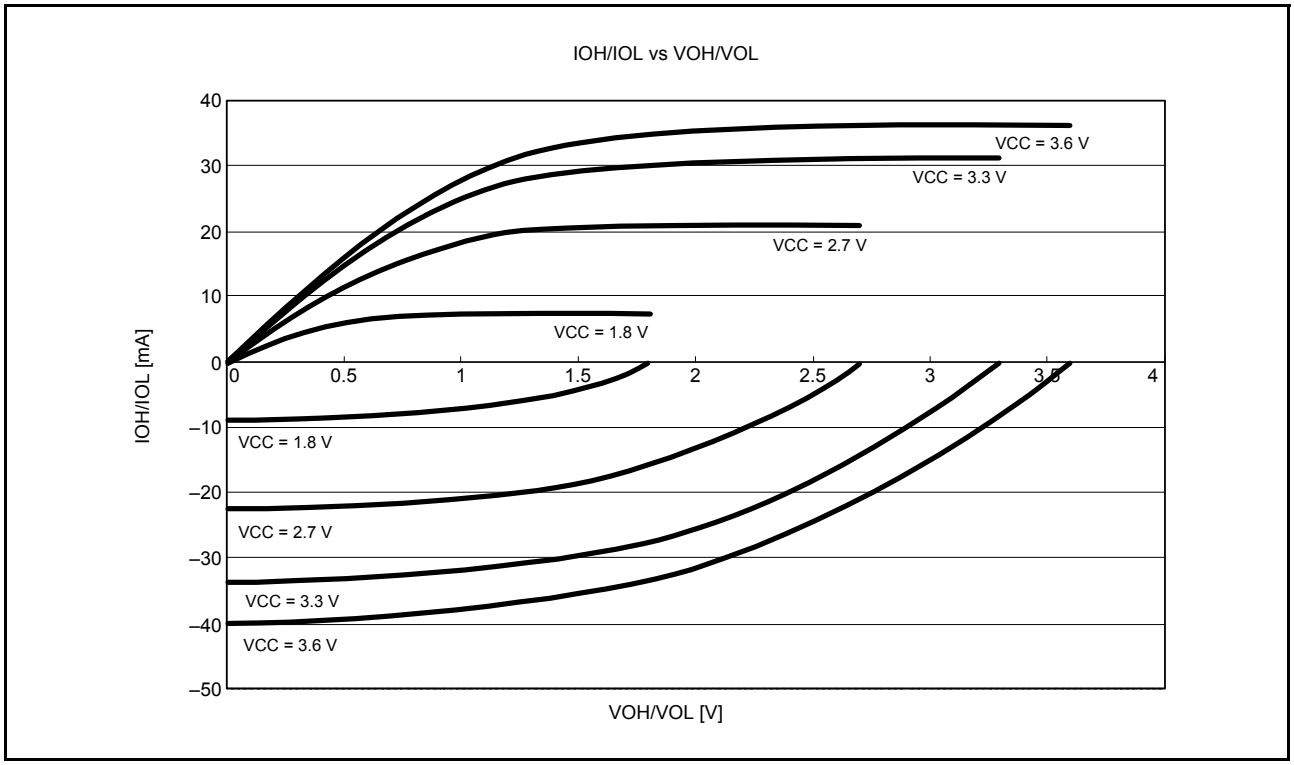



**Figure 5.16 VOH/VOL and IOH/IOL Voltage Characteristics at Ta = 25°C when High-Drive Output is Selected (Reference Data)**

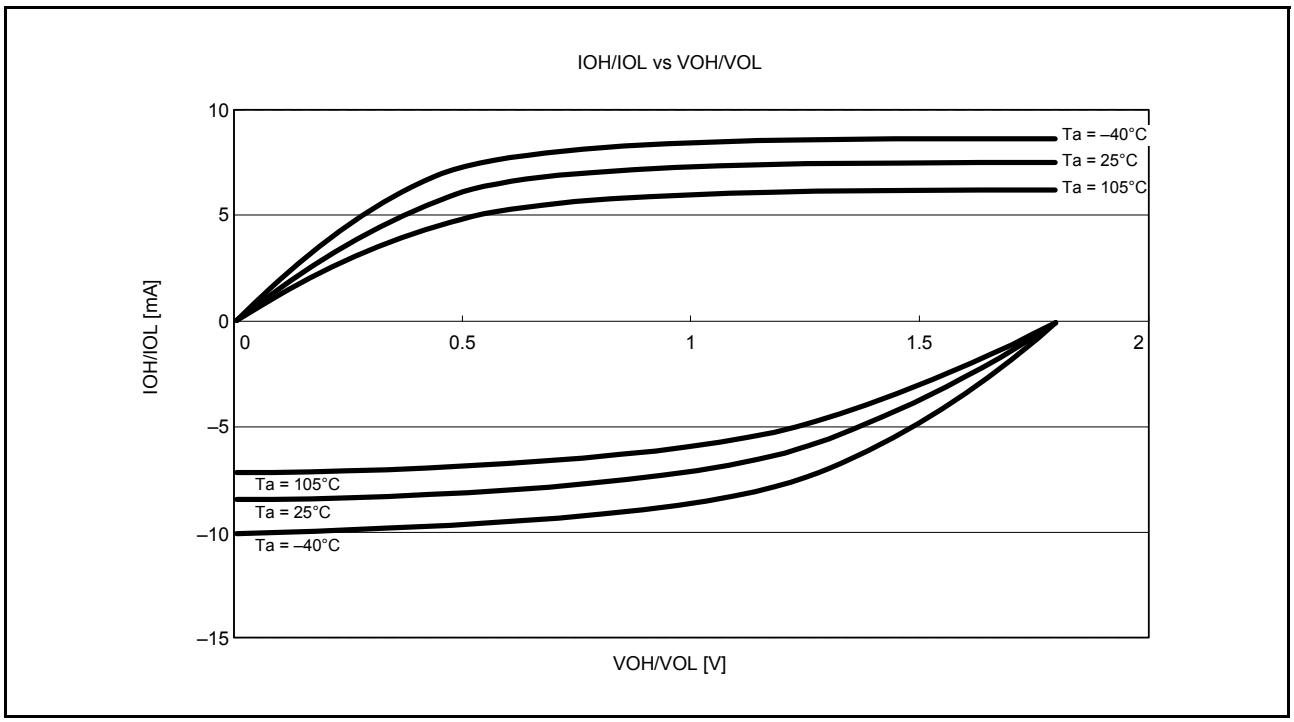



**Figure 5.17 VOH/VOL and IOH/IOL Temperature Characteristics at VCC = 1.8 V when High-Drive Output is Selected (Reference Data)**

Note 2. When specifying the main clock oscillator stabilization time, load MOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the main lock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the main clock oscillation stabilization time.
Start using the main clock in the main clock oscillation stabilization wait time (tMAINOSCWT) after setting up the main clock oscillator for operation with the MOSCCR.MOSTP bit.
The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 3. Sum of the main clock oscillation stabilization time and the PLL oscillation stabilization time.
Note 4. The indicated value is a reference value that is measured for an 8 MHz resonator.
Note 5. When specifying the sub-clock oscillation stabilization time, load SOSCWTCR register with a stabilization time value that is greater than the resonator-vendor-recommended value. When determining the sub-clock oscillation stabilization wait time, allow an adequate margin (2 times is recommended) for the sub-clock oscillation stabilization time. Start using the sub-clock in the sub-clock oscillation stabilization wait time (tSUBOSCWT) after setting up the sub-clock oscillator for operation with the SOSCCR.SOSTP or RCR3.RTCEN bit.

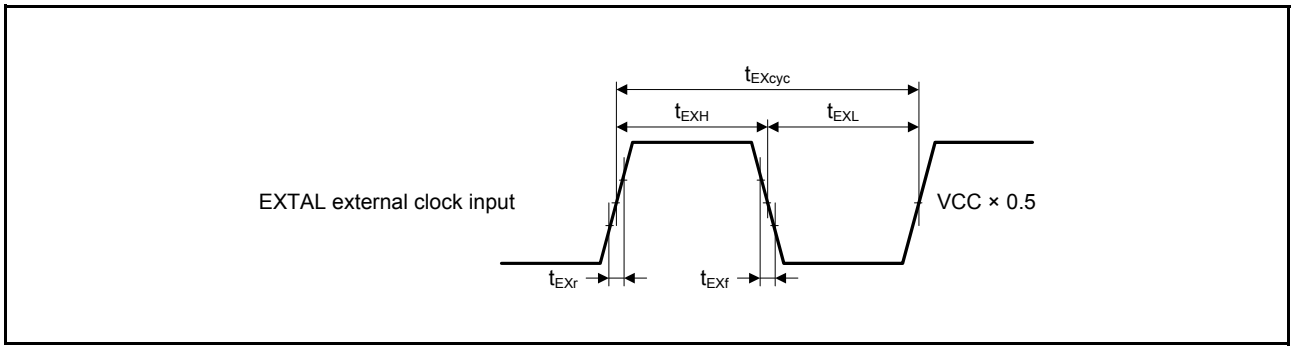



**Figure 5.25 EXTAL External Clock Input Timing**

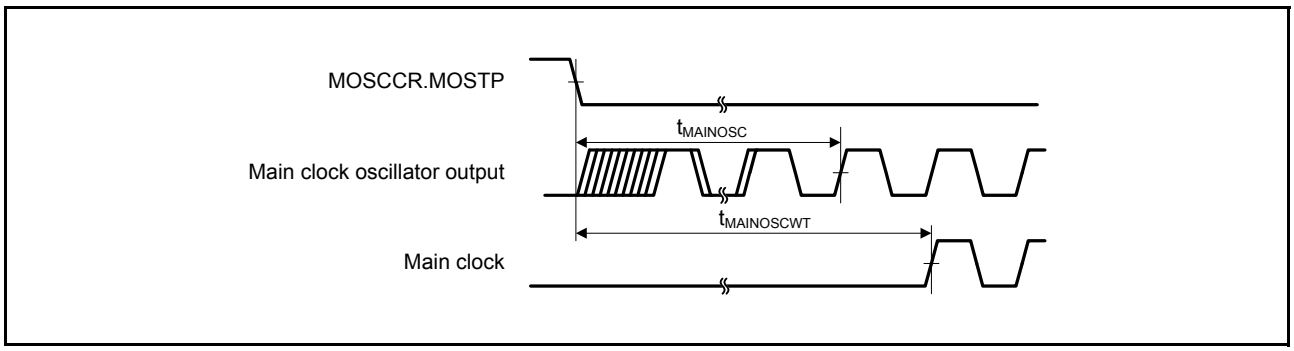



**Figure 5.26 Main Clock Oscillation Start Timing**

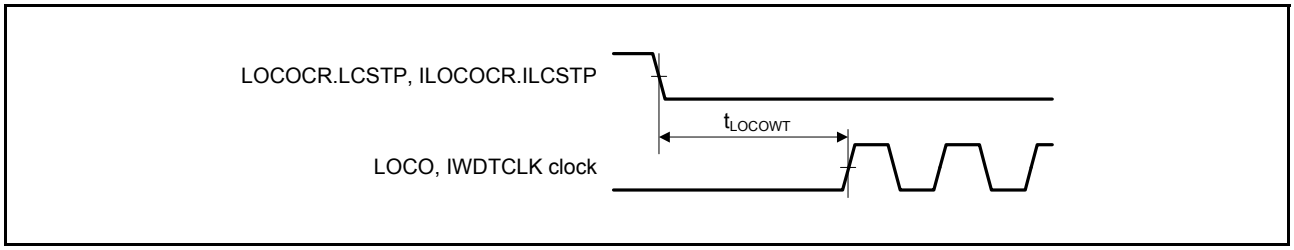



**Figure 5.27 LOCO, IWDTCLK Clock Oscillation Start Timing**

**Table 5.34 Timing of On-Chip Peripheral Modules (5)**

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard mode, SMBus) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.54 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | — | ns | Figure 5.54 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: • $t_{IICcyc}$: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. $C_b$ indicates the total capacity of the bus line.

**Table 5.35 Timing of On-Chip Peripheral Modules (6)**

Conditions: VCC = AVCC0 = AVCCA = 2.7 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard mode) | SDA input rise time | $t_{Sr}$ | — | 1000 | ns | Figure 5.54 |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{pcyc}$*2 | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| Simple IIC (Fast mode) | SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | Figure 5.54 |
| | SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{pcyc}$*2 | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: • $t_{Pcyc}$: PCLK cycle
Note 1. $C_b$ indicates the total capacity of the bus line.
Note 2. This applies when the SMR.CKS[1:0] bits = 00b and the SNFR.NFCS[2:0] bits = 010b while the SNFR.NFE bit = 1 and the digital filter is enabled.

| Item | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|
| Input impedance for single-ended input (×4) | 54 | 91 | — | kΩ | | |
| Oversampling frequency | 3.125 | 3.125 | 3.125 | MHz | | |
| Oversampling period | 0.32 | 0.32 | 0.32 | µs | | |
| Conversion time | 81.92 | — | 245.76 | µs | | |
| Sampling frequency | 4.07 | — | 12.21 | kHz | | |
| SNDR (Gain: ×1 Input amplitude: 500.0 mV) | — | 80 | — | dB | | Sampling frequency = 12.21 kHz<br><br>Clock source: Resonator |
| | — | 85 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×2 Input amplitude: 250.0 mV) | — | 80 | — | dB | | |
| | — | 85 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×4 Input amplitude: 125.0 mV) | — | 78 | — | dB | | |
| | — | 83 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×8 Input amplitude: 62.5 mV) | — | 75 | — | dB | | |
| | — | 80 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×16 Input amplitude: 31.2 mV) | — | 71 | — | dB | | |
| | — | 76 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×32 Input amplitude: 14.4 mV) | — | 64 | — | dB | | |
| | — | 69 | — | dB | Bandwidth = up to 1.7 kHz | |
| SNDR (Gain: ×64 Input amplitude: 5 mV) | — | 54 | — | dB | | |
| | — | 59 | — | dB | Bandwidth = up to 1.7 kHz | |

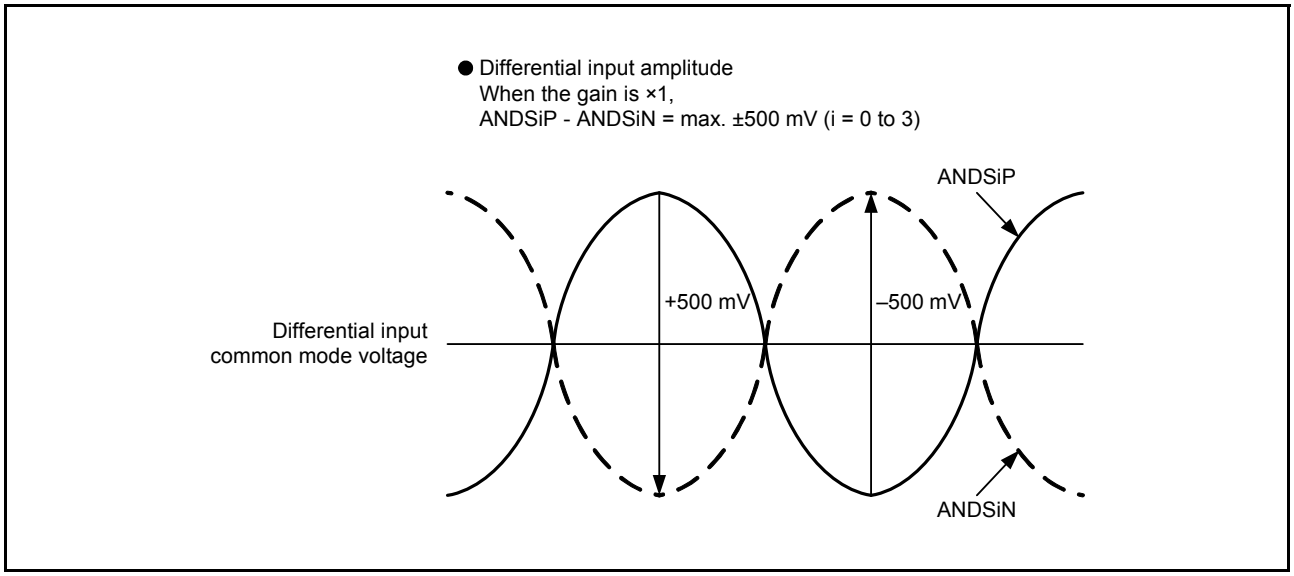



**Figure 5.55 Differential Input Amplitude**

**Differential nonlinearity error (DNL)**

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

**Offset error**

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

**Full-scale error**

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

## 5.11 Oscillation Stop Detection Timing

**Table 5.46 Oscillation Stop Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V,
$T_a$ = –40 to +105°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 5.69 |

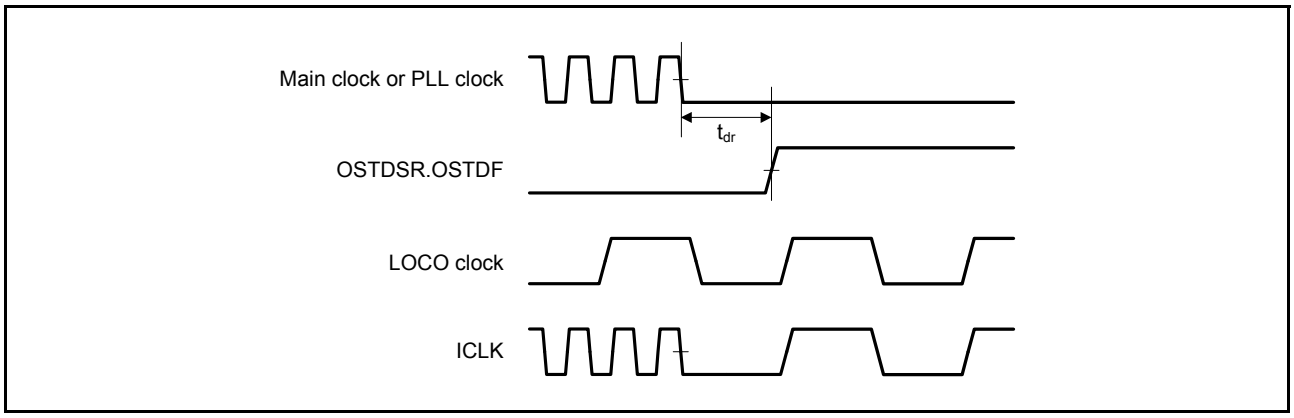



**Figure 5.69 Oscillation Stop Detection Timing**

**Table 5.49 ROM (Flash Memory for Code Storage) Characteristics (3) : medium-speed operating modes 1B and 2B**

Conditions: VCC = AVCC0 = AVCCA = 1.8 to 3.6 V, VSS = AVSS0 = AVSSA = VREFL = VREFL0 = VREFDSL = 0 V
Temperature range for the programming/erasure operation: $T_a$ = –40 to +105°C

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 25 MHz*1 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time when $N_{PEC}$ ≤ 100 times | 2 bytes | $t_{P2}$ | — | 0.25 | 5.0 | — | 0.21 | 2.9 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.25 | 5.3 | — | 0.21 | 3.1 | |
| | 128 bytes | $t_{P128}$ | — | 0.92 | 14.0 | — | 0.66 | 8.5 | |
| Programming time when $N_{PEC}$ > 100 times | 2 bytes | $t_{P2}$ | — | 0.31 | 6.2 | — | 0.26 | 3.6 | ms |
| | 8 bytes | $t_{P8}$ | — | 0.31 | 6.6 | — | 0.26 | 3.8 | |
| | 128 bytes | $t_{P128}$ | — | 1.09 | 17.5 | — | 0.78 | 10.3 | |
| Erasure time when $N_{PEC}$ ≤ 100 times | 2 Kbytes | $t_{E2K}$ | — | 21.0 | 113.6 | — | 18.6 | 48.7 | ms |
| Erasure time when $N_{PEC}$ > 100 times | 2 Kbytes | $t_{E2K}$ | — | 25.6 | 220.6 | — | 22.7 | 94.5 (1000 times ≥ $N_{PEC}$ > 100 times), 102.9 (10000 times ≥ $N_{PEC}$ > 1000 times) | ms |
| Suspend delay time during programming (in programming/erasure priority mode) | | $t_{SPD}$ | — | — | 1.7 | — | — | 1.604 | ms |
| First suspend delay time during programming (in suspend priority mode) | | $t_{SPSD1}$ | — | — | 220 | — | — | 124 | µs |
| Second suspend delay time during programming (in suspend priority mode) | | $t_{SPSD2}$ | — | — | 1.7 | — | — | 1.604 | ms |
| Suspend delay time during erasing (in programming/erasure priority mode) | | $t_{SED}$ | — | — | 1.7 | — | — | 1.604 | ms |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 220 | — | — | 124 | µs |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.604 | ms |
| FCU reset time | | $t_{FCUR}$ | 20 µs or longer and FCLK × 6 or greater | — | — | 20 µs or longer and FCLK × 6 or greater | — | — | µs |

Note 1. The FCLK operating frequency is 12.5 MHz (max.) when the voltage is in the range from 1.8 V to less than 2.7 V in mid-speed operating mode 2B.