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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8672
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	190
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s1200e-4ftg256q

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specification over the T_J = –40°C to +125°C temperature range (Q-Grade)
- XA Spartan-3E devices are available in the -4 speed grade only.
- PCI-66 is not supported in the XA Spartan-3E FPGA product line.
- The readback feature is not supported in the XA Spartan-3E FPGA product line.
- XA Spartan-3E devices are available in Step 1 only.
- JTAG configuration frequency reduced from 30 MHz to 25 MHz.
- Platform Flash is not supported within the XA family.
- XA Spartan-3E devices are available in Pb-free packaging only.
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3E device must be power cycled prior to reconfiguration.

Table 1: **Summary of XA Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XA3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XA3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	190	77
XA3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XA3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

Architectural Overview

The XA Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XA3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XA3S100E has only one DCM at the top and bottom, while the XA3S1200E and XA3S1600E add two DCMs in the middle of the left and right sides.

The XA Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQG100		CPG132		TQG144		PQG208		FTG256		FGG400		FGG484	
Size (mm)	16 x 16		8 x 8		22 x 22		28 x 28		17 x 17		21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XA3S100E	**66** *(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-
XA3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-
XA3S500E	-	-	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	-	-	-	-
XA3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**304** *(72)*	**124** *(20)*	-	-
XA3S1600E	-	-	-	-	-	-	-	-	-	-	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of DS312.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.

Power Supply Specifications

Table 3: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Table 7: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins *(Continued)***

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_{RPD}(2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	0.10	–	0.75	mA
R_{PD}(2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{IN} = V_{CCO}$ = 3.0V to 3.45V	4.0	–	34.5	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V	3.0	–	27.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V	2.3	–	19.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V	1.8	–	16.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	-	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Table 8: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3S100E	36	58	mA
		XA3S250E	104	158	mA
		XA3S500E	145	300	mA
		XA3S1200E	324	500	mA
		XA3S1600E	457	750	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3S100E	1.5	2.0	mA
		XA3S250E	1.5	3.0	mA
		XA3S500E	1.5	3.0	mA
		XA3S1200E	2.5	4.0	mA
		XA3S1600E	2.5	4.0	mA

Table 8: **Quiescent Supply Current Characteristics *(Continued)***

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XA3S100E	13	22	mA
		XA3S250E	26	43	mA
		XA3S500E	34	63	mA
		XA3S1200E	59	100	mA
		XA3S1600E	86	150	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx XPower tools.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

Single-Ended I/O Standards

Table 9: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.465				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3	3.0	3.3	3.465				0.3 * V_{CCO}	0.5 * V_{CCO}
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.125	V_{REF} + 0.125

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. The V_{CCO} rails supply only output drivers, not input circuits.
3. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72 in DS312.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci.

Table 16: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	5.97	ns
			3	**XA3S250E**	6.33	ns
			2	**XA3S500E**	6.49	ns
			5	**XA3S1200E**	8.15	ns
			4	**XA3S1600E**	7.16	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 17.

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Single-Ended Standards		
LVTTL	0.43	ns
LVCMOS33	0.43	ns
LVCMOS25	0	ns
LVCMOS18	0.98	ns
LVCMOS15	0.63	ns
LVCMOS12	0.27	ns
PCI33_3	0.42	ns
HSTL_I_18	0.12	ns
HSTL_III_18	0.17	ns
SSTL18_I	0.30	ns
SSTL2_I	0.15	ns

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Differential Standards		
LVDS_25	0.49	ns
BLVDS_25	0.39	ns
MINI_LVDS_25	0.49	ns
LVPECL_25	0.27	ns
RSDS_25	0.49	ns
DIFF_HSTL_I_18	0.49	ns
DIFF_HSTL_III_18	0.49	ns
DIFF_SSTL18_I	0.30	ns
DIFF_SSTL2_I	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 18: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below: -4 Speed Grade	Units
Single-Ended Standards				
LVTTL	Slow	2 mA	5.41	ns
		4 mA	2.41	ns
		6 mA	1.90	ns
		8 mA	0.67	ns
		12 mA	0.70	ns
		16 mA	0.43	ns
	Fast	2 mA	5.00	ns
		4 mA	1.96	ns
		6 mA	1.45	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS33	Slow	2 mA	5.29	ns
		4 mA	1.89	ns
		6 mA	1.04	ns
		8 mA	0.69	ns
		12 mA	0.42	ns
		16 mA	0.43	ns
	Fast	2 mA	4.87	ns
		4 mA	1.52	ns
		6 mA	0.39	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS25	Slow	2 mA	4.21	ns
		4 mA	2.26	ns
		6 mA	1.52	ns
		8 mA	1.08	ns
		12 mA	0.68	ns
	Fast	2 mA	3.67	ns
		4 mA	1.72	ns
		6 mA	0.46	ns
		8 mA	0.21	ns
		12 mA	0	ns

Table 18: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below: -4 Speed Grade	Units
LVCMOS18	Slow	2 mA	5.24	ns
		4 mA	3.21	ns
		6 mA	2.49	ns
		8 mA	1.90	ns
	Fast	2 mA	4.15	ns
		4 mA	2.13	ns
		6 mA	1.14	ns
		8 mA	0.75	ns
LVCMOS15	Slow	2 mA	4.68	ns
		4 mA	3.97	ns
		6 mA	3.11	ns
	Fast	2 mA	3.38	ns
		4 mA	2.70	ns
		6 mA	1.53	ns
LVCMOS12	Slow	2 mA	6.63	ns
	Fast	2 mA	4.44	ns
HSTL_I_18			0.34	ns
HSTL_III_18			0.55	ns
PCI33_3			0.46	ns
SSTL18_I			0.25	ns
SSTL2_I			–0.20	ns
Differential Standards				
LVDS_25			–0.55	ns
BLVDS_25			0.04	ns
MINI_LVDS_25			–0.56	ns
LVPECL_25			Input Only	ns
RSDS_25			–0.48	ns
DIFF_HSTL_I_18			0.42	ns
DIFF_HSTL_III_18			0.55	ns
DIFF_SSTL18_I			0.40	ns
DIFF_SSTL2_I			0.44	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Configurable Logic Block Timing

Table 20: **CLB (SLICEM) Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.60	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.81	-	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	572	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.76	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Table 21: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.35	ns
Setup Times				
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.40	-	ns
Hold Times				
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	-	ns

Table 22: **CLB Shift Register Switching Characteristics**

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	4.16	ns
Setup Times				
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	-	ns
Hold Times				
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	-	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	-	ns

Table 25: **Block RAM Timing *(Continued)***

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Timing				
T_{BPWH}	High pulse width of the CLK signal	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.59	-	ns
Clock Frequency				
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster.	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 26 and Table 27) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 28 through Table 31) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 26 and Table 27.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

Table 27: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description		-4 Speed Grade		Units
			Min	Max	
Duty Cycle(4)					
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		-	±[1% of CLKIN period + 400]	ps
Phase Alignment(4)					
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	-	±[1% of CLKIN period + 100]	ps
		All others	-	±[1% of CLKIN period + 200]	ps
Lock Time					
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	-	5	ms
		F_{CLKIN} > 15 MHz	-	600	µs
Delay Lines					
DCM_DELAY_STEP	Finest delay resolution		20	40	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 26.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer

Table 28: **Recommended Operating Conditions for the DFS**

Symbol		Description		-4 Speed Grade		Units
				Min	Max	
Input Frequency Ranges(2)						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 26.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 29: **Switching Characteristics for the DFS**

Symbol	Description		Device	-4 Speed Grade		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs		All	5	311	MHz
Output Clock Jitter(2,3)						
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs		All	**Typ**	**Max**	
		CLKIN ≤20 MHz		See Note 4		ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)						
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(6)						
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	ps
Lock Time						
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 28.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKFX period + 300]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.

Phase Shifter

Table 30: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	-

Configuration and JTAG Timing

Table 33: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	-4 Speed Grade		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XA3S100E	-	5	ms
		XA3S250E	-	5	ms
		XA3S500E	-	5	ms
		XA3S1200E	-	5	ms
		XA3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XA3S100E	-	0.5	ms
		XA3S250E	-	0.5	ms
		XA3S500E	-	1	ms
		XA3S1200E	-	2	ms
		XA3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Master Serial and Slave Serial Mode Timing

Table 38: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	-4 Speed Grade		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 36		
			Slave	See Table 37		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 36		
			Slave	See Table 37		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66(2)	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing

Table 39: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description			-4 Speed Grade		Units
				Min	Max	
Clock-to-Output Times						
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin			-	12.0	ns
Setup Times						
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the active edge the CCLK pin			11.0	-	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the active edge of the CCLK pin			10.0	-	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before active edge of the CCLK pin			23.0	-	ns
Hold Times						
T_{SMCCD}	The time from the active edge of the CCLK pin to the point when data is last held at the D0-D7 pins			1.0	-	ns
T_{SMCCCS}	The time from the active edge of the CCLK pin to the point when a logic level is last held at the CSO_B pin			0	-	ns
T_{SMWCC}	The time from the active edge of the CCLK pin to the point when a logic level is last held at the RDWR_B pin			0	-	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Byte Peripheral Interface Configuration Timing

Table 42: **Timing for BPI Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		(see Table 34)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		(see Table 34)		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	**BPI-UP:** (M[2:0]=<0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0]=<0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 38		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 38		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 38		

Table 43: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

IEEE 1149.1/1553 JTAG Test Access Port Timing

Table 44: **Timing for the JTAG Test Access Port**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	25	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/31/07	1.0	Initial Xilinx release.
01/20/09	1.1	• Updated "Key Feature Differences from Commercial XC Devices." • Updated T_{ACC} requirement in Table 43. • Updated description of T_{DCC} and T_{CCD} in Table 42. • Removed Table 45: MultiBoot Trigger Timing.
09/09/09	2.0	• Added package sizes to Table 2, page 4. • Removed Genealogy Viewer Link from "Package Marking," page 5. • Updated data and notes for Table 6, page 8. • Updated test conditions for R_{PU} and maximum value for C_{IN} in Table 7, page 8. • Updated notes for Table 8, page 9. • Updated Max V_{CCO} for LVTTL and LVCMOS33, removed PCIX data, updated V_{IL} Max for LVCMOS18, LVCMOS15, and LVCMOS12, updated V_{IH} Min for LVCMOS12, and added note 6 in Table 9, page 11. • Removed PCIX data, revised note 2, and added note 4 in Table 10, page 12. • Updated figure description of Figure 5, page 14. • Added note 4 to Table 13, page 14. • Removed PC166_3 and PCIX adjustment values from Table 17, page 17. • Deleted Table 18 (duplicate of Table 17, page 17). Subsequent tables renumbered. • Removed PCIX data Table 18, page 18. • Removed PCIX data and removed V_{REF} values for DIFF_HSTL_I_18, DIFF_HSTL_III_18, DIFF_SSTL18_I, and DIFF_SSTL2_I from Table 19, page 19. • Updated T_{DICK} minimum setup time in Table 20, page 20. • Updated notes, references to notes, and revised the maximum clock-to-output times for T_{MSCKP_P} Table 24, page 22. • Added "Spread Spectrum," page 24. • Updated note 3 in Table 26, page 25. • Added note 4 Table 28, page 26. • Updated notes, references to notes, and CLKOUT_PER_JITT_FX data in Table 29, page 27. • Updated MAX_STEPS data in Table 31, page 28. • Updated ConfigRate Setting for T_{CCLK1} to indicate 1 is the default value in Table 34, page 30. • Updated ConfigRate Setting for F_{CCLK1} to indicate 1 is the default value in Table 35, page 30.

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