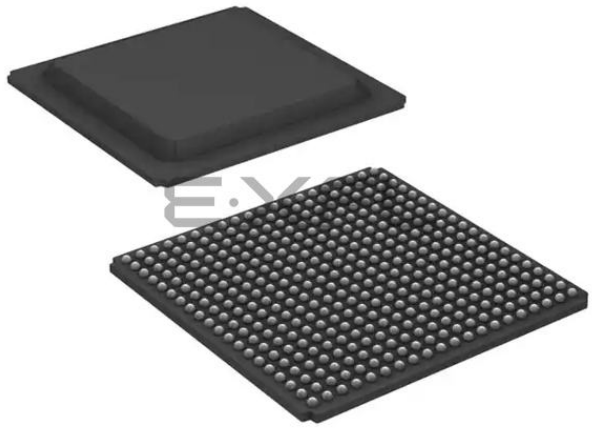
AMD Xilinx - XA3S1600E-4FG400I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	304
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s1600e-4fg400i

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQG100		CPG132		TQG144		PQG208		FTG256		FGG400		FGG484	
Size (mm)	16 x 16		8 x 8		22 x 22		28 x 28		17 x 17		21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XA3S100E	**66** *(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-
XA3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-
XA3S500E	-	-	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	-	-	-	-
XA3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**304** *(72)*	**124** *(20)*	-	-
XA3S1600E	-	-	-	-	-	-	-	-	-	-	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of DS312.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.

Package Marking

Figure 2 provides a top marking example for XA Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for XA Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for XA Spartan-3E FPGAs in the CPG132 package.

Note: **No marking is shown for stepping.**

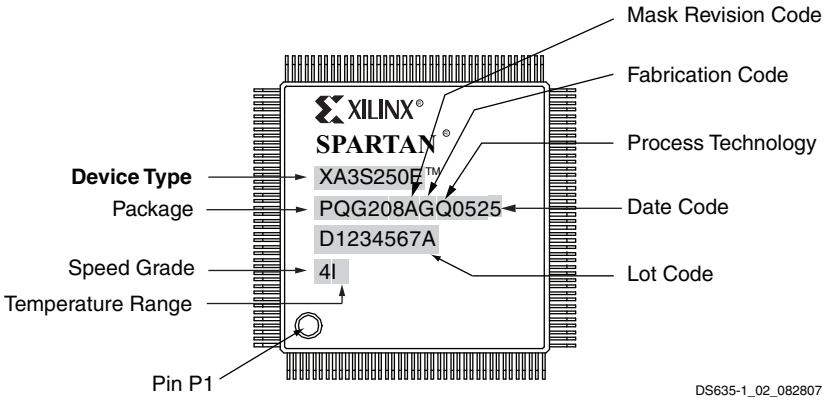


Figure 2: **XA Spartan-3E FPGA QFP Package Marking Example**

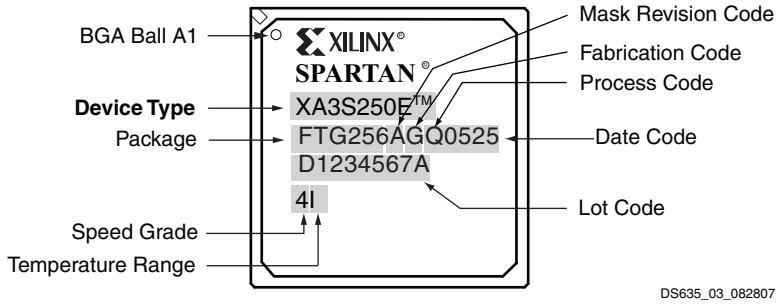


Figure 3: **XA Spartan-3E FPGA BGA Package Marking Example**

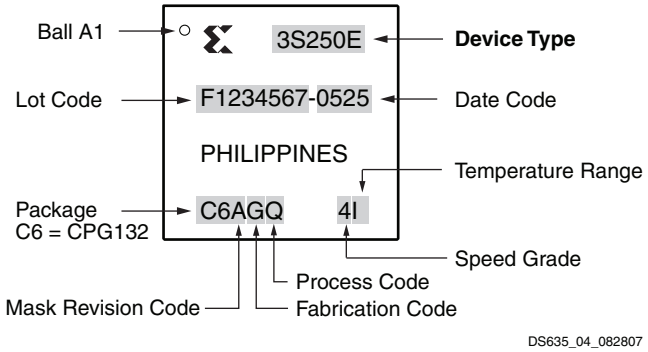
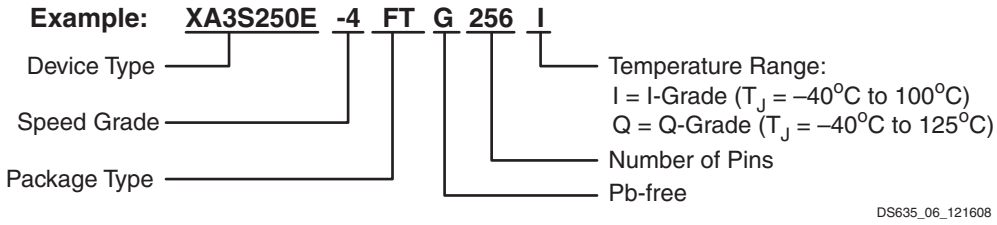


Figure 4: **XA Spartan-3E FPGA CPG132 Package Marking Example**

Ordering Information

XA Spartan-3E FPGAs are available in Pb-free packaging options for all device/package combinations. All devices are in Pb-free packages only, with a “G” character to the ordering code. All devices are available in either I-Grade or Q-Grade temperature ranges. Only the -4 speed grade is available for the XA Spartan-3E family. See Table 2 for valid device/package combinations.

Pb-Free Packaging



Device
XA3S100E
XA3S250E
XA3S500E
XA3S1200E
XA3S1600E

Speed Grade	
-4	Only

Package Type / Number of Pins	
VQG100	100-pin Very Thin Quad Flat Pack (VQFP)
CPG132	132-ball Chip-Scale Package (CSP)
TQG144	144-pin Thin Quad Flat Pack (TQFP)
PQG208	208-pin Plastic Quad Flat Pack (PQFP)
FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
I	I-Grade (–40°C to 100°C)
Q	Q-Grade (–40°C to 125°C)

Power Supply Specifications

Table 3: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

DC Specifications

Table 6: **General Recommended Operating Conditions**

Symbol	Description		Min	Nominal	Max	Units
T_J	Junction temperature	I-Grade	–40	25	100	°C
		Q-Grade	–40	25	125	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO}(1)	Output driver supply voltage		1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX}(2)	Voltage variance on V_{CCAUX} when using a DCM		-	-	10	mV/ms
V_{IN}(3,4,5,6)	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins(3)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins(4)	–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time(7)		–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 9 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 11 lists that specific to the differential standards.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.
3. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. See Absolute Maximum Ratings in DS312).
4. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
5. Input voltages outside the recommended range is permissible provided that the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. See Absolute Maximum Ratings in DS312).
6. See XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins."
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 7: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_L	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	–10	–	+10	µA
I_{RPU}(2)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V	–0.36	–	–1.24	mA
		V_{IN} = 0V, V_{CCO} = 2.5V	–0.22	–	–0.80	mA
		V_{IN} = 0V, V_{CCO} = 1.8V	–0.10	–	–0.42	mA
		V_{IN} = 0V, V_{CCO} = 1.5V	–0.06	–	–0.27	mA
		V_{IN} = 0V, V_{CCO} = 1.2V	–0.04	–	–0.22	mA
R_{PU}(2)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = 0V, V_{CCO} = 3.0V to 3.465V	2.4	–	10.8	kΩ
		V_{IN} = 0V, V_{CCO} = 2.3V to 2.7V	2.7	–	11.8	kΩ
		V_{IN} = 0V, V_{CCO} = 1.7V to 1.9V	4.3	–	20.2	kΩ
		V_{IN} = 0V, V_{CCO} =1.4V to 1.6V	5.0	–	25.9	kΩ
		V_{IN} = 0V, V_{CCO} = 1.14V to 1.26V	5.5	–	32.0	kΩ

Table 7: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins *(Continued)***

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_{RPD}(2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	0.10	–	0.75	mA
R_{PD}(2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{IN} = V_{CCO}$ = 3.0V to 3.45V	4.0	–	34.5	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V	3.0	–	27.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V	2.3	–	19.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V	1.8	–	16.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	-	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Table 8: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3S100E	36	58	mA
		XA3S250E	104	158	mA
		XA3S500E	145	300	mA
		XA3S1200E	324	500	mA
		XA3S1600E	457	750	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3S100E	1.5	2.0	mA
		XA3S250E	1.5	3.0	mA
		XA3S500E	1.5	3.0	mA
		XA3S1200E	2.5	4.0	mA
		XA3S1600E	2.5	4.0	mA

Single-Ended I/O Standards

Table 9: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.465				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3	3.0	3.3	3.465				0.3 * V_{CCO}	0.5 * V_{CCO}
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.125	V_{REF} + 0.125

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. The V_{CCO} rails supply only output drivers, not input circuits.
3. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72 in DS312.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci.

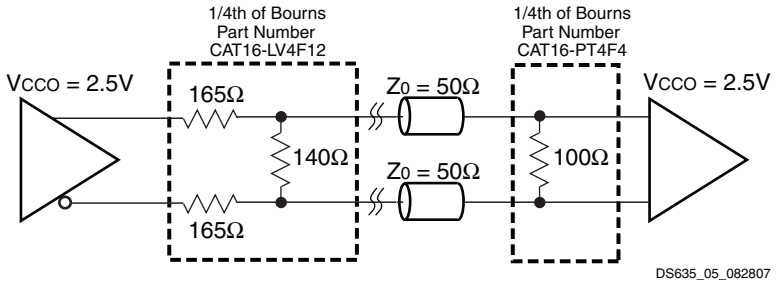


Figure 5: **External Termination Resistors for BLVDS Transmitter and BLVDS Receiver**

Switching Characteristics

I/O Timing

Table 13: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	-4 Speed Grade	Units
				Max	
Clock-to-Output Times					
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	**XA3S100E**	2.79	ns
			XA3S250E	3.45	ns
			XA3S500E	3.46	ns
			XA3S1200E	3.46	ns
			XA3S1600E	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	**XA3S100E**	5.92	ns
			XA3S250E	5.43	ns
			XA3S500E	5.51	ns
			XA3S1200E	5.94	ns
			XA3S1600E	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 17. If the latter is true, *add* the appropriate Output adjustment from Table 18.
3. DCM output jitter is included in all measurements.
4. For minimums, use the values reported by the Xilinx timing analyzer.

Table 14: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	-4 Speed Grade	Units
					Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	0	**XA3S100E**	2.98	ns
				XA3S250E	2.59	ns
				XA3S500E	2.59	ns
				XA3S1200E	2.58	ns
				XA3S1600E	2.59	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	3.58	ns
			3	**XA3S250E**	3.91	ns
			2	**XA3S500E**	4.02	ns
			5	**XA3S1200E**	5.52	ns
			4	**XA3S1600E**	4.46	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	0	**XA3S100E**	–0.52	ns
				XA3S250E	0.14	ns
				XA3S500E	0.14	ns
				XA3S1200E	0.15	ns
				XA3S1600E	0.14	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	–0.24	ns
			3	**XA3S250E**	–0.32	ns
			2	**XA3S500E**	–0.49	ns
			5	**XA3S1200E**	–0.63	ns
			4	**XA3S1600E**	–0.39	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 17. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 17. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 15: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade Min	Units
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	6.49	ns
			3	**XA3S250E**	6.85	ns
			2	**XA3S500E**	7.01	ns
			5	**XA3S1200E**	8.67	ns
			4	**XA3S1600E**	7.69	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	–0.76	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	–3.93	ns
			3	**XA3S250E**	–3.51	ns
			2	**XA3S500E**	–3.74	ns
			5	**XA3S1200E**	–4.30	ns
			4	**XA3S1600E**	–4.14	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 17.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 17. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 19: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_I_18		-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18		-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I		-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I		-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

Configurable Logic Block Timing

Table 20: **CLB (SLICEM) Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.60	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.81	-	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	572	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.76	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Clock Buffer/Multiplexer Switching Characteristics

Table 23: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum	Units
		-4 Speed Grade	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	311	MHz

18 x 18 Embedded Multiplier Timing

Table 24: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Combinatorial Delay				
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.88(1)	ns
Clock-to-Output Times				
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.97	ns
Setup Times				
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.39	-	ns
Hold Times				
T_{MSCKD_P}	Data hold time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	-0.97		
T_{MSCKD_A}	Data hold time at the A input before the active transition at the CLK when using the AREG input register(3)	0.04		
T_{MSCKD_B}	Data hold time at the B input before the active transition at the CLK when using the BREG input register(3)	0.05		

Table 25: **Block RAM Timing *(Continued)***

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Timing				
T_{BPWH}	High pulse width of the CLK signal	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.59	-	ns
Clock Frequency				
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster.	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 26 and Table 27) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 28 through Table 31) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 26 and Table 27.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

Table 27: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description		-4 Speed Grade		Units
			Min	Max	
Duty Cycle(4)					
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		-	±[1% of CLKIN period + 400]	ps
Phase Alignment(4)					
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	-	±[1% of CLKIN period + 100]	ps
		All others	-	±[1% of CLKIN period + 200]	ps
Lock Time					
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	-	5	ms
		F_{CLKIN} > 15 MHz	-	600	µs
Delay Lines					
DCM_DELAY_STEP	Finest delay resolution		20	40	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 26.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer

Table 28: **Recommended Operating Conditions for the DFS**

Symbol		Description		-4 Speed Grade		Units
				Min	Max	
Input Frequency Ranges(2)						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 26.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 29: **Switching Characteristics for the DFS**

Symbol	Description		Device	-4 Speed Grade		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs		All	5	311	MHz
Output Clock Jitter(2,3)						
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs		All	**Typ**	**Max**	
		CLKIN ≤20 MHz		See Note 4		ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)						
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(6)						
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	ps
Lock Time						
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 28.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKFX period + 300]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.

Phase Shifter

Table 30: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	-

Configuration and JTAG Timing

Table 33: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	-4 Speed Grade		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XA3S100E	-	5	ms
		XA3S250E	-	5	ms
		XA3S500E	-	5	ms
		XA3S1200E	-	5	ms
		XA3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XA3S100E	-	0.5	ms
		XA3S250E	-	0.5	ms
		XA3S500E	-	1	ms
		XA3S1200E	-	2	ms
		XA3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Configuration Clock (CCLK) Characteristics

Table 34: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	I-Grade Q-Grade	485	1,250	ns
T_{CCLK3}		3	I-Grade Q-Grade	242	625	ns
T_{CCLK6}		6	I-Grade Q-Grade	121	313	ns
T_{CCLK12}		12	I-Grade Q-Grade	60.6	157	ns
T_{CCLK25}		25	I-Grade Q-Grade	30.3	78.2	ns
T_{CCLK50}		50	I-Grade Q-Grade	15.1	39.1	ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in DS312, Module 2.

Table 35: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	I-Grade Q-Grade	0.8	2.1	MHz
F_{CCLK3}		3	I-Grade Q-Grade	1.6	4.2	MHz
F_{CCLK6}		6	I-Grade Q-Grade	3.2	8.3	MHz
F_{CCLK12}		12	I-Grade Q-Grade	6.4	16.5	MHz
F_{CCLK25}		25	I-Grade Q-Grade	12.8	33.0	MHz
F_{CCLK50}		50	I-Grade Q-Grade	25.6	66.0	MHz

Table 36: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	I-Grade Q-Grade	235	117	58	29.3	14.5	7.3	ns

Table 37: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

Table 38: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	-4 Speed Grade		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 36		
			Slave	See Table 37		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 36		
			Slave	See Table 37		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66(2)	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

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