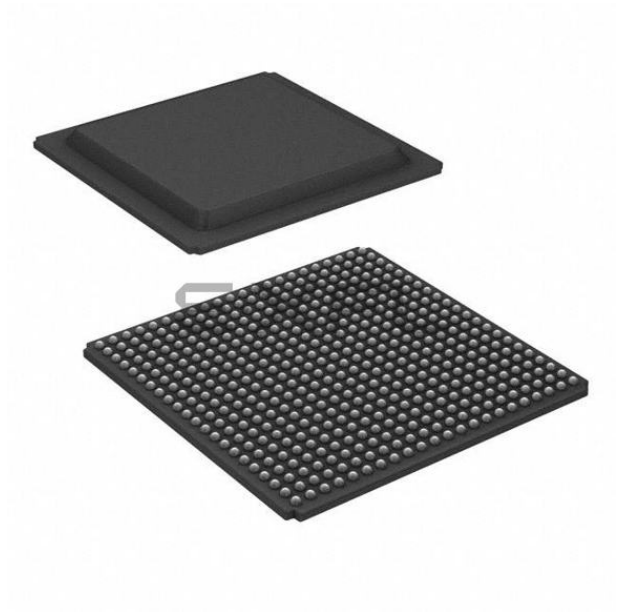
AMD Xilinx - XA3S1600E-4FGG484I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	376
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s1600e-4fgg484i

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQG100		CPG132		TQG144		PQG208		FTG256		FGG400		FGG484	
Size (mm)	16 x 16		8 x 8		22 x 22		28 x 28		17 x 17		21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XA3S100E	**66** *(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-
XA3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-
XA3S500E	-	-	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	-	-	-	-
XA3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**304** *(72)*	**124** *(20)*	-	-
XA3S1600E	-	-	-	-	-	-	-	-	-	-	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

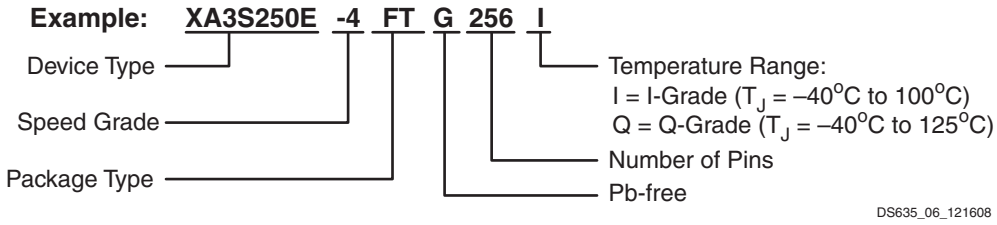
Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of DS312.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.

Ordering Information

XA Spartan-3E FPGAs are available in Pb-free packaging options for all device/package combinations. All devices are in Pb-free packages only, with a “G” character to the ordering code. All devices are available in either I-Grade or Q-Grade temperature ranges. Only the -4 speed grade is available for the XA Spartan-3E family. See Table 2 for valid device/package combinations.

Pb-Free Packaging



Device
XA3S100E
XA3S250E
XA3S500E
XA3S1200E
XA3S1600E

Speed Grade	
-4	Only

Package Type / Number of Pins	
VQG100	100-pin Very Thin Quad Flat Pack (VQFP)
CPG132	132-ball Chip-Scale Package (CSP)
TQG144	144-pin Thin Quad Flat Pack (TQFP)
PQG208	208-pin Plastic Quad Flat Pack (PQFP)
FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
I	I-Grade (–40°C to 100°C)
Q	Q-Grade (–40°C to 125°C)

Table 7: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins *(Continued)***

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_{RPD}(2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	0.10	–	0.75	mA
R_{PD}(2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{IN} = V_{CCO}$ = 3.0V to 3.45V	4.0	–	34.5	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V	3.0	–	27.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V	2.3	–	19.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V	1.8	–	16.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	-	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Table 8: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3S100E	36	58	mA
		XA3S250E	104	158	mA
		XA3S500E	145	300	mA
		XA3S1200E	324	500	mA
		XA3S1600E	457	750	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3S100E	1.5	2.0	mA
		XA3S250E	1.5	3.0	mA
		XA3S500E	1.5	3.0	mA
		XA3S1200E	2.5	4.0	mA
		XA3S1600E	2.5	4.0	mA

Single-Ended I/O Standards

Table 9: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.465				0.8	2.0
LVCMOS25(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3	3.0	3.3	3.465				0.3 * V_{CCO}	0.5 * V_{CCO}
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.125	V_{REF} + 0.125

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. The V_{CCO} rails supply only output drivers, not input circuits.
3. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72 in DS312.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci.

Differential I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2
LVPECL_25(2)	Inputs Only			100	800	1000	0.5	1.2	2.0
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

Table 12: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	–	–	1.125	–	1.375	–	–	–	–
BLVDS_25	250	350	450	–	–	–	1.20	–	–	–	–	–
MINI_LVDS_25	300	–	600	–	50	1.0	–	1.4	–	50	–	–
RSDS_25	100	–	400	–	–	1.1	–	1.4	–	–	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6, and Table 11.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 5 below.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

Table 16: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	5.97	ns
			3	**XA3S250E**	6.33	ns
			2	**XA3S500E**	6.49	ns
			5	**XA3S1200E**	8.15	ns
			4	**XA3S1600E**	7.16	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 17.

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Single-Ended Standards		
LVTTL	0.43	ns
LVCMOS33	0.43	ns
LVCMOS25	0	ns
LVCMOS18	0.98	ns
LVCMOS15	0.63	ns
LVCMOS12	0.27	ns
PCI33_3	0.42	ns
HSTL_I_18	0.12	ns
HSTL_III_18	0.17	ns
SSTL18_I	0.30	ns
SSTL2_I	0.15	ns

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Differential Standards		
LVDS_25	0.49	ns
BLVDS_25	0.39	ns
MINI_LVDS_25	0.49	ns
LVPECL_25	0.27	ns
RSDS_25	0.49	ns
DIFF_HSTL_I_18	0.49	ns
DIFF_HSTL_III_18	0.49	ns
DIFF_SSTL18_I	0.30	ns
DIFF_SSTL2_I	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 19: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_I_18		-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18		-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I		-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I		-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

Configurable Logic Block Timing

Table 20: **CLB (SLICEM) Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.60	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.81	-	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	572	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.76	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Table 21: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.35	ns
Setup Times				
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.40	-	ns
Hold Times				
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	-	ns

Table 22: **CLB Shift Register Switching Characteristics**

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	4.16	ns
Setup Times				
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	-	ns
Hold Times				
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	-	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 23: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum	Units
		-4 Speed Grade	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	311	MHz

18 x 18 Embedded Multiplier Timing

Table 24: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Combinatorial Delay				
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.88(1)	ns
Clock-to-Output Times				
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.97	ns
Setup Times				
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.39	-	ns
Hold Times				
T_{MSCKD_P}	Data hold time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	-0.97		
T_{MSCKD_A}	Data hold time at the A input before the active transition at the CLK when using the AREG input register(3)	0.04		
T_{MSCKD_B}	Data hold time at the B input before the active transition at the CLK when using the BREG input register(3)	0.05		

Table 24: **18 x 18 Embedded Multiplier Timing *(Continued)***

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Frequency				
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	240	MHz

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Block RAM Timing

Table 25: **Block RAM Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.82	ns
Setup Times				
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.26	-	ns
Hold Times				
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	ns

Delay-Locked Loop

Table 26: **Recommended Operating Conditions for the DLL**

Symbol		Description		-4 Speed Grade		Units
				Min	Max	
Input Frequency Ranges						
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	240(3)	MHz
Input Pulse Requirements						
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz	40%	60%	-
			$F_{CLKIN} > 150$ MHz	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation(4)						
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz	-	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	-	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		-	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 28.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 27: **Switching Characteristics for the DLL**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Output Frequency Ranges				
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	5	240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	10	311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	0.3125	160	MHz
Output Clock Jitter(2,3,4)				
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division	-	±[1% of CLKIN period + 200]	ps

Table 27: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description		-4 Speed Grade		Units
			Min	Max	
Duty Cycle(4)					
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		-	±[1% of CLKIN period + 400]	ps
Phase Alignment(4)					
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	-	±[1% of CLKIN period + 100]	ps
		All others	-	±[1% of CLKIN period + 200]	ps
Lock Time					
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	-	5	ms
		F_{CLKIN} > 15 MHz	-	600	µs
Delay Lines					
DCM_DELAY_STEP	Finest delay resolution		20	40	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 26.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. ***Example:*** The data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer

Table 28: **Recommended Operating Conditions for the DFS**

Symbol		Description		-4 Speed Grade		Units
				Min	Max	
Input Frequency Ranges(2)						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 26.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 31: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description			Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 30.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 27.

Miscellaneous DCM Timing

Table 32: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specification. This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration and JTAG Timing

Table 33: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	-4 Speed Grade		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XA3S100E	-	5	ms
		XA3S250E	-	5	ms
		XA3S500E	-	5	ms
		XA3S1200E	-	5	ms
		XA3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XA3S100E	-	0.5	ms
		XA3S250E	-	0.5	ms
		XA3S500E	-	1	ms
		XA3S1200E	-	2	ms
		XA3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Configuration Clock (CCLK) Characteristics

Table 34: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	I-Grade Q-Grade	485	1,250	ns
T_{CCLK3}		3	I-Grade Q-Grade	242	625	ns
T_{CCLK6}		6	I-Grade Q-Grade	121	313	ns
T_{CCLK12}		12	I-Grade Q-Grade	60.6	157	ns
T_{CCLK25}		25	I-Grade Q-Grade	30.3	78.2	ns
T_{CCLK50}		50	I-Grade Q-Grade	15.1	39.1	ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in DS312, Module 2.

Table 35: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	I-Grade Q-Grade	0.8	2.1	MHz
F_{CCLK3}		3	I-Grade Q-Grade	1.6	4.2	MHz
F_{CCLK6}		6	I-Grade Q-Grade	3.2	8.3	MHz
F_{CCLK12}		12	I-Grade Q-Grade	6.4	16.5	MHz
F_{CCLK25}		25	I-Grade Q-Grade	12.8	33.0	MHz
F_{CCLK50}		50	I-Grade Q-Grade	25.6	66.0	MHz

Table 36: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	I-Grade Q-Grade	235	117	58	29.3	14.5	7.3	ns

Table 37: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Serial Peripheral Interface Configuration Timing

Table 40: **Timing for SPI Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	(see Table 34)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	(see Table 34)		
T_{MINIT}	Setup time on VS[2:0] and M[2:0] mode pins before the rising edge of INIT_B	50	-	ns
T_{INITM}	Hold time on VS[2:0] and M[2:0]mode pins after the rising edge of INIT_B	0	-	ns
T_{CCO}	MOSI output valid after CCLK edge	See Table 38		
T_{DCC}	Setup time on DIN data input before CCLK edge	See Table 38		
T_{CCD}	Hold time on DIN data input after CCLK edge	See Table 38		

Table 41: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \le T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \le T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \le T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \le T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \ge \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface Configuration Timing

Table 42: **Timing for BPI Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		(see Table 34)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		(see Table 34)		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	**BPI-UP:** (M[2:0]=<0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0]=<0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 38		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 38		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 38		

Table 43: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/31/07	1.0	Initial Xilinx release.
01/20/09	1.1	• Updated "Key Feature Differences from Commercial XC Devices." • Updated T_{ACC} requirement in Table 43. • Updated description of T_{DCC} and T_{CCD} in Table 42. • Removed Table 45: MultiBoot Trigger Timing.
09/09/09	2.0	• Added package sizes to Table 2, page 4. • Removed Genealogy Viewer Link from "Package Marking," page 5. • Updated data and notes for Table 6, page 8. • Updated test conditions for R_{PU} and maximum value for C_{IN} in Table 7, page 8. • Updated notes for Table 8, page 9. • Updated Max V_{CCO} for LVTTL and LVCMOS33, removed PCIX data, updated V_{IL} Max for LVCMOS18, LVCMOS15, and LVCMOS12, updated V_{IH} Min for LVCMOS12, and added note 6 in Table 9, page 11. • Removed PCIX data, revised note 2, and added note 4 in Table 10, page 12. • Updated figure description of Figure 5, page 14. • Added note 4 to Table 13, page 14. • Removed PC166_3 and PCIX adjustment values from Table 17, page 17. • Deleted Table 18 (duplicate of Table 17, page 17). Subsequent tables renumbered. • Removed PCIX data Table 18, page 18. • Removed PCIX data and removed V_{REF} values for DIFF_HSTL_I_18, DIFF_HSTL_III_18, DIFF_SSTL18_I, and DIFF_SSTL2_I from Table 19, page 19. • Updated T_{DICK} minimum setup time in Table 20, page 20. • Updated notes, references to notes, and revised the maximum clock-to-output times for T_{MSCKP_P} Table 24, page 22. • Added "Spread Spectrum," page 24. • Updated note 3 in Table 26, page 25. • Added note 4 Table 28, page 26. • Updated notes, references to notes, and CLKOUT_PER_JITT_FX data in Table 29, page 27. • Updated MAX_STEPS data in Table 31, page 28. • Updated ConfigRate Setting for T_{CCLK1} to indicate 1 is the default value in Table 34, page 30. • Updated ConfigRate Setting for F_{CCLK1} to indicate 1 is the default value in Table 35, page 30.

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