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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	92
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	132-TFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xa3s250e-4cpg132q">https://www.e-xfl.com/product-detail/xilinx/xa3s250e-4cpg132q</a>

## Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specification over the  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range (Q-Grade)
- XA Spartan-3E devices are available in the -4 speed grade only.
- PCI-66 is not supported in the XA Spartan-3E FPGA product line.
- The readback feature is not supported in the XA Spartan-3E FPGA product line.
- XA Spartan-3E devices are available in Step 1 only.
- JTAG configuration frequency reduced from 30 MHz to 25 MHz.
- Platform Flash is not supported within the XA family.
- XA Spartan-3E devices are available in Pb-free packaging only.
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3E device must be power cycled prior to reconfiguration.

Table 1: Summary of XA Spartan-3E FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits <sup>(1)</sup>	Block RAM bits <sup>(1)</sup>	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XA3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XA3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	190	77
XA3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XA3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

### Notes:

- By convention, one Kb is equivalent to 1,024 bits.

## Architectural Overview

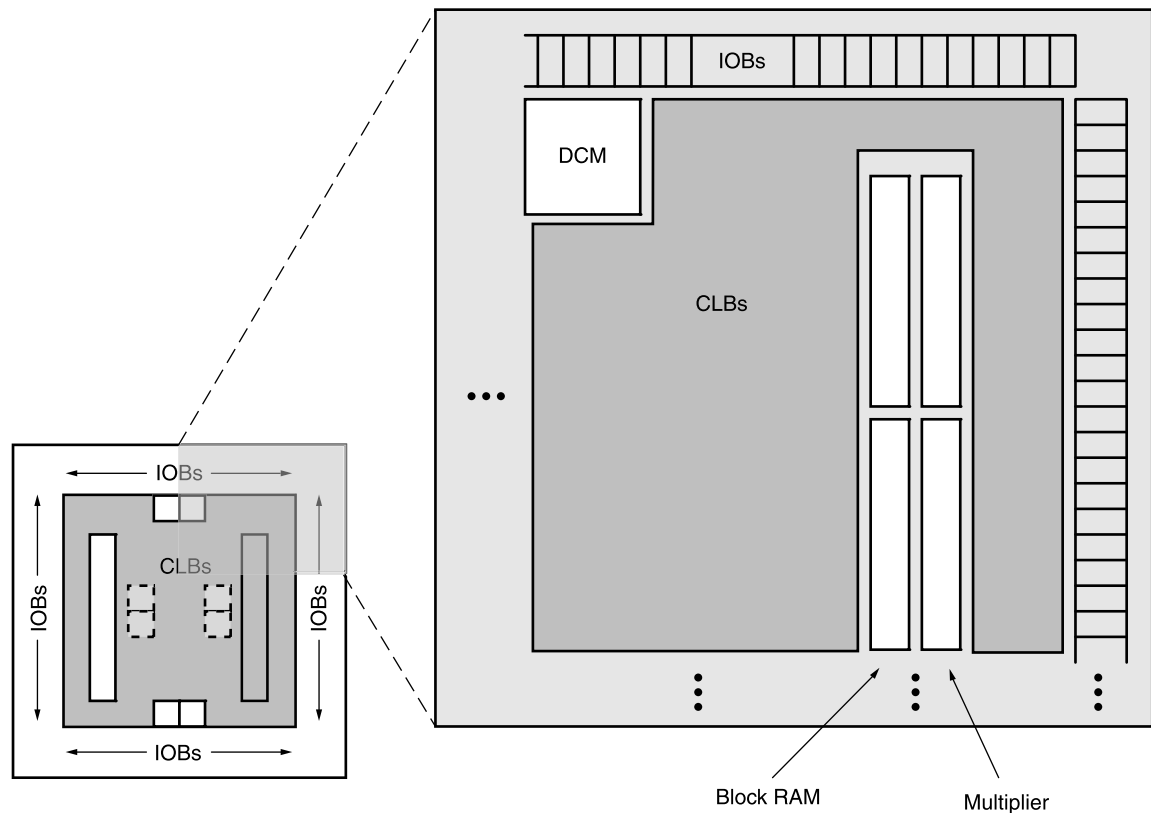
The XA Spartan-3E family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.

- Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XA3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XA3S100E has only one DCM at the top and bottom, while the XA3S1200E and XA3S1600E add two DCMs in the middle of the left and right sides.

The XA Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



#### Notes:

1. The XA3S1200E and XA3S1600E have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XA3S100E has only one DCM at the top and one at the bottom.

Figure 1: XA Spartan-3E Family Architecture

## Configuration

XA Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

## I/O Capabilities

The XA Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

XA Spartan-3E FPGAs support the following single-ended standards:

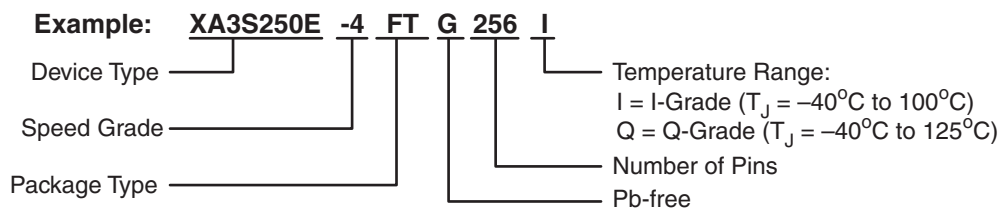
- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

## Ordering Information

XA Spartan-3E FPGAs are available in Pb-free packaging options for all device/package combinations. All devices are in Pb-free packages only, with a “G” character to the ordering code. All devices are available in either I-Grade or

Q-Grade temperature ranges. Only the -4 speed grade is available for the XA Spartan-3E family. See [Table 2](#) for valid device/package combinations.

### Pb-Free Packaging



DS635\_06\_121608

Device	Speed Grade		Package Type / Number of Pins		Temperature Range ( $T_J$ )	
XA3S100E	-4	Only	VQG100	100-pin Very Thin Quad Flat Pack (VQFP)	I	I-Grade ( $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$ )
XA3S250E			CPG132	132-ball Chip-Scale Package (CSP)	Q	Q-Grade ( $-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ )
XA3S500E			TQG144	144-pin Thin Quad Flat Pack (TQFP)		
XA3S1200E			PQG208	208-pin Plastic Quad Flat Pack (PQFP)		
XA3S1600E			FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)		
			FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
			FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		

## Power Supply Specifications

Table 3: Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
$V_{CCINTT}$	Threshold for the $V_{CCINT}$ supply	0.4	1.0	V
$V_{CCAUXT}$	Threshold for the $V_{CCAUX}$ supply	0.8	2.0	V
$V_{CCO2T}$	Threshold for the $V_{CCO}$ Bank 2 supply	0.4	1.0	V

**Notes:**

1.  $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on,  $V_{CCINT}$ ,  $V_{CCO}$  Bank 2, and  $V_{CCAUX}$  supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
$V_{CCINTR}$	Ramp rate from GND to valid $V_{CCINT}$ supply level	0.2	50	ms
$V_{CCAUXR}$	Ramp rate from GND to valid $V_{CCAUX}$ supply level	0.2	50	ms
$V_{CCO2R}$	Ramp rate from GND to valid $V_{CCO}$ Bank 2 supply level	0.2	50	ms

**Notes:**

1.  $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on,  $V_{CCINT}$ ,  $V_{CCO}$  Bank 2, and  $V_{CCAUX}$  supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: Supply Voltage Levels Necessary for Preserving RAM Contents

Symbol	Description	Min	Units
$V_{DRINT}$	$V_{CCINT}$ level required to retain RAM data	1.0	V
$V_{DRAUX}$	$V_{CCAUX}$ level required to retain RAM data	2.0	V

**Notes:**

1. RAM contents include configuration data.

## DC Specifications

Table 6: General Recommended Operating Conditions

Symbol	Description		Min	Nominal	Max	Units
T <sub>J</sub>	Junction temperature	I-Grade	−40	25	100	°C
		Q-Grade	−40	25	125	°C
V <sub>CCINT</sub>	Internal supply voltage		1.140	1.200	1.260	V
V <sub>CCO</sub> <sup>(1)</sup>	Output driver supply voltage		1.100	-	3.465	V
V <sub>CCAUX</sub>	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV <sub>CCAUX</sub> <sup>(2)</sup>	Voltage variance on V <sub>CCAUX</sub> when using a DCM		-	-	10	mV/ms
V <sub>IN</sub> <sup>(3,4,5,6)</sup>	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins <sup>(3)</sup>	−0.5	−	V <sub>CCO</sub> + 0.5	V
		Dedicated pins <sup>(4)</sup>	−0.5	−	V <sub>CCAUX</sub> + 0.5	V
T <sub>IN</sub>	Input signal transition time <sup>(7)</sup>		−	−	500	ns

### Notes:

1. This  $V_{CCO}$  range spans the lowest and highest operating voltages for all supported I/O standards. Table 9 lists the recommended  $V_{CCO}$  range specific to each of the single-ended I/O standards, and Table 11 lists that specific to the differential standards.
2. Only during DCM operation is it recommended that the rate of change of  $V_{CCAUX}$  not exceed 10 mV/ms.
3. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks'  $V_{CCO}$  rails. Meeting the  $V_{IN}$  limit ensures that the internal diode junctions that exist between these pins and their associated  $V_{CCO}$  and GND rails do not turn on. See Absolute Maximum Ratings in DS312.
4. All Dedicated pins (PROG\_B, DONE, TCK, TDI, TDO, and TMS) draw power from the  $V_{CCAUX}$  rail (2.5V). Meeting the  $V_{IN}$  max limit ensures that the internal diode junctions that exist between each of these pins and the  $V_{CCAUX}$  and GND rails do not turn on.
5. Input voltages outside the recommended range is permissible provided that the  $I_{IK}$  input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. See Absolute Maximum Ratings in DS312.
6. See XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins."
7. Measured between 10% and 90%  $V_{CCO}$ . Follow Signal Integrity recommendations.

## General DC Characteristics for I/O Pins

Table 7: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins

Symbol	Description	Test Conditions	Min	Typ	Max	Units
$I_L$	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, $V_{IN} = 0V$ or $V_{CCO}$ max, sample-tested	–10	–	+10	$\mu A$
$I_{RPU}^{(2)}$	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = 0V$ , $V_{CCO} = 3.3V$	–0.36	–	–1.24	mA
		$V_{IN} = 0V$ , $V_{CCO} = 2.5V$	–0.22	–	–0.80	mA
		$V_{IN} = 0V$ , $V_{CCO} = 1.8V$	–0.10	–	–0.42	mA
		$V_{IN} = 0V$ , $V_{CCO} = 1.5V$	–0.06	–	–0.27	mA
		$V_{IN} = 0V$ , $V_{CCO} = 1.2V$	–0.04	–	–0.22	mA
$R_{PU}^{(2)}$	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on $I_{RPU}$ per Note 2)	$V_{IN} = 0V$ , $V_{CCO} = 3.0V$ to $3.465V$	2.4	–	10.8	k $\Omega$
		$V_{IN} = 0V$ , $V_{CCO} = 2.3V$ to $2.7V$	2.7	–	11.8	k $\Omega$
		$V_{IN} = 0V$ , $V_{CCO} = 1.7V$ to $1.9V$	4.3	–	20.2	k $\Omega$
		$V_{IN} = 0V$ , $V_{CCO} = 1.4V$ to $1.6V$	5.0	–	25.9	k $\Omega$
		$V_{IN} = 0V$ , $V_{CCO} = 1.14V$ to $1.26V$	5.5	–	32.0	k $\Omega$

Table 8: Quiescent Supply Current Characteristics (Continued)

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
$I_{CCAUXQ}$	Quiescent $V_{CCAUX}$ supply current	XA3S100E	13	22	mA
		XA3S250E	26	43	mA
		XA3S500E	34	63	mA
		XA3S1200E	59	100	mA
		XA3S1600E	86	150	mA

**Notes:**

1. The numbers in this table are based on the conditions set forth in [Table 6](#).
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature ( $T_J$  of 25°C at  $V_{CCINT} = 1.2$  V,  $V_{CCO} = 3.3$  V, and  $V_{CCAUX} = 2.5$  V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with  $V_{CCINT} = 1.26$  V,  $V_{CCO} = 3.465$  V, and  $V_{CCAUX} = 2.625$  V. The FPGA is programmed with a “blank” configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx XPower tools.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The [Spartan-3E XPower Estimator](#) provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

## Single-Ended I/O Standards

Table 9: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	V <sub>CCO</sub> for Drivers <sup>(2)</sup>			V <sub>REF</sub>			V <sub>IL</sub>	V <sub>IH</sub>
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465	V <sub>REF</sub> is not used for these I/O standards			0.8	2.0
LVC MOS33 <sup>(4)</sup>	3.0	3.3	3.465				0.8	2.0
LVC MOS25 <sup>(4,5)</sup>	2.3	2.5	2.7				0.7	1.7
LVC MOS18	1.65	1.8	1.95				0.4	0.8
LVC MOS15	1.4	1.5	1.6				0.4	0.8
LVC MOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3	3.0	3.3	3.465				0.3 * V <sub>CCO</sub>	0.5 * V <sub>CCO</sub>
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125

### Notes:

- Descriptions of the symbols used in this table are as follows:  
V<sub>CCO</sub> – the supply voltage for output drivers  
V<sub>REF</sub> – the reference voltage for setting the input switching threshold  
V<sub>IL</sub> – the input voltage that indicates a Low logic level  
V<sub>IH</sub> – the input voltage that indicates a High logic level
- The V<sub>CCO</sub> rails supply only output drivers, not input circuits.
- For device operation, the maximum signal voltage (V<sub>IH</sub> max) may be as high as V<sub>IN</sub> max. See Table 72 in DS312.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG\_B, DONE, TCK, TDI, TDO, and TMS) use the LVC MOS25 standard and draw power from the V<sub>CCAUX</sub> rail (2.5V). The Dual-Purpose configuration pins use the LVC MOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V<sub>CCO</sub> lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see [www.xilinx.com/pci](http://www.xilinx.com/pci).



## Differential I/O Standards

Table 11: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V <sub>CCO</sub> for Drivers <sup>(1)</sup>			V <sub>ID</sub>			V <sub>ICM</sub>		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2
LVPECL_25 <sup>(2)</sup>	Inputs Only			100	800	1000	0.5	1.2	2.0
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5

**Notes:**

1. The V<sub>CCO</sub> rails supply only differential output drivers, not input circuits.
2. V<sub>REF</sub> inputs are not used for any of the differential I/O standards.

Table 12: DC Characteristics of User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V <sub>OD</sub>			$\Delta V_{OD}$		V <sub>OCM</sub>			$\Delta V_{OCM}$		V <sub>OH</sub>	V <sub>OL</sub>
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	-	-	1.125	-	1.375	-	-	-	-
BLVDS_25	250	350	450	-	-	-	1.20	-	-	-	-	-
MINI_LVDS_25	300	-	600	-	50	1.0	-	1.4	-	50	-	-
RSDS_25	100	-	400	-	-	1.1	-	1.4	-	-	-	-
DIFF_HSTL_I_18	-	-	-	-	-	-	-	-	-	-	V <sub>CCO</sub> - 0.4	0.4
DIFF_HSTL_III_18	-	-	-	-	-	-	-	-	-	-	V <sub>CCO</sub> - 0.4	0.4
DIFF_SSTL18_I	-	-	-	-	-	-	-	-	-	-	V <sub>TT</sub> + 0.475	V <sub>TT</sub> - 0.475
DIFF_SSTL2_I	-	-	-	-	-	-	-	-	-	-	V <sub>TT</sub> + 0.61	V <sub>TT</sub> - 0.61

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 6, and Table 11.
2. Output voltage measurements for all differential standards are made with a termination resistor (R<sub>T</sub>) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 5 below.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS\_25, RSDS\_25, MINI\_LVDS\_25

Table 14: Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	-4 Speed Grade	Units
					Min	
Setup Times						
T <sub>PSDCM</sub>	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed.	LVCMOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = 0, with DCM <sup>(4)</sup>	0	XA3S100E	2.98	ns
				XA3S250E	2.59	ns
				XA3S500E	2.59	ns
				XA3S1200E	2.58	ns
				XA3S1600E	2.59	ns
T <sub>PSFD</sub>	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = default software setting	2	XA3S100E	3.58	ns
			3	XA3S250E	3.91	ns
			2	XA3S500E	4.02	ns
			5	XA3S1200E	5.52	ns
			4	XA3S1600E	4.46	ns
Hold Times						
T <sub>PHDCM</sub>	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed.	LVCMOS25 <sup>(3)</sup> , IFD_DELAY_VALUE = 0, with DCM <sup>(4)</sup>	0	XA3S100E	−0.52	ns
				XA3S250E	0.14	ns
				XA3S500E	0.14	ns
				XA3S1200E	0.15	ns
				XA3S1600E	0.14	ns
T <sub>PHFD</sub>	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25 <sup>(3)</sup> , IFD_DELAY_VALUE = default software setting	2	XA3S100E	−0.24	ns
			3	XA3S250E	−0.32	ns
			2	XA3S500E	−0.49	ns
			5	XA3S1200E	−0.63	ns
			4	XA3S1600E	−0.39	ns

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 17. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 17. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 15: Setup and Hold Times for the IOB Input Path

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade	Units
					Min	
Setup Times						
T <sub>IOPICK</sub>	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVC MOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = 0	0	All	2.12	ns
T <sub>IOPICKD</sub>	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVC MOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = default software setting	2	XA3S100E	6.49	ns
			3	XA3S250E	6.85	ns
			2	XA3S500E	7.01	ns
			5	XA3S1200E	8.67	ns
			4	XA3S1600E	7.69	ns
Hold Times						
T <sub>IOICKP</sub>	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVC MOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = 0	0	All	−0.76	ns
T <sub>IOICKPD</sub>	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVC MOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = default software setting	2	XA3S100E	−3.93	ns
			3	XA3S250E	−3.51	ns
			2	XA3S500E	−3.74	ns
			5	XA3S1200E	−4.30	ns
			4	XA3S1600E	−4.14	ns
Set/Reset Pulse Width						
T <sub>RPW_IOB</sub>	Minimum pulse width to SR control input on IOB			All	1.80	ns

**Notes:**

1. The numbers in this table are tested using the methodology presented in [Table 19](#) and are based on the operating conditions set forth in [Table 6](#) and [Table 9](#).
2. This setup time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from [Table 17](#).
3. These hold times require adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from [Table 17](#). When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: CLB Distributed RAM Switching Characteristics

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T <sub>SHCKO</sub>	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.35	ns
Setup Times				
T <sub>DS</sub>	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	-	ns
T <sub>AS</sub>	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.52	-	ns
T <sub>WS</sub>	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.40	-	ns
Hold Times				
T <sub>DH</sub>	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.15	-	ns
T <sub>AH</sub> , T <sub>WH</sub>	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	ns
Clock Pulse Width				
T <sub>WPH</sub> , T <sub>WPL</sub>	Minimum High or Low pulse width at CLK input	1.01	-	ns

Table 22: CLB Shift Register Switching Characteristics

Symbol	Description	-4		Units
		Min	Max	
Clock-to-Output Times				
T <sub>REG</sub>	Time from the active edge at the CLK input to data appearing on the shift register output	-	4.16	ns
Setup Times				
T <sub>SRLDS</sub>	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.46	-	ns
Hold Times				
T <sub>SRLDH</sub>	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	-	ns
Clock Pulse Width				
T <sub>WPH</sub> , T <sub>WPL</sub>	Minimum High or Low pulse width at CLK input	1.01	-	ns

Table 24: 18 x 18 Embedded Multiplier Timing (Continued)

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Frequency				
F <sub>MULT</sub>	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register <sup>(1)</sup>	0	240	MHz

**Notes:**

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

## Block RAM Timing

Table 25: Block RAM Timing

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T <sub>BCKO</sub>	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.82	ns
Setup Times				
T <sub>BACK</sub>	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.38	-	ns
T <sub>BDCK</sub>	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	ns
T <sub>BECK</sub>	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.77	-	ns
T <sub>BWCK</sub>	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.26	-	ns
Hold Times				
T <sub>BCKA</sub>	Hold time on the ADDR inputs after the active transition at the CLK input	0.14	-	ns
T <sub>BCKD</sub>	Hold time on the DIN inputs after the active transition at the CLK input	0.13	-	ns
T <sub>BCKE</sub>	Hold time on the EN input after the active transition at the CLK input	0	-	ns
T <sub>BCKW</sub>	Hold time on the WE input after the active transition at the CLK input	0	-	ns

Table 25: Block RAM Timing (Continued)

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Timing				
T <sub>BPWH</sub>	High pulse width of the CLK signal	1.59	-	ns
T <sub>BPWL</sub>	Low pulse width of the CLK signal	1.59	-	ns
Clock Frequency				
F <sub>BRAM</sub>	Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster.	0	230	MHz

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).

## Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables ([Table 26](#) and [Table 27](#)) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables ([Table 28](#) through [Table 31](#)) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in [Table 26](#) and [Table 27](#).

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

## Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See [XAPP469](#), *Spread-Spectrum Clocking Reception for Displays* for details.

## Delay-Locked Loop

Table 26: Recommended Operating Conditions for the DLL

Symbol		Description	-4 Speed Grade		Units	
			Min	Max		
Input Frequency Ranges						
F <sub>CLKIN</sub>	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input	5 <sup>(2)</sup>	240 <sup>(3)</sup>	MHz	
Input Pulse Requirements						
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	F <sub>CLKIN</sub> ≤ 150 MHz	40%	60%	-
			F <sub>CLKIN</sub> > 150 MHz	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation <sup>(4)</sup>						
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	F <sub>CLKIN</sub> ≤ 150 MHz	-	±300	ps
CLKIN_CYC_JITT_DLL_HF			F <sub>CLKIN</sub> > 150 MHz	-	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		-	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		-	±1	ns

### Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower  $F_{CLKIN}$  frequencies. See [Table 28](#).
3. To support double the maximum effective  $F_{CLKIN}$  limit, set the CLKIN\_DIVIDE\_BY\_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 27: Switching Characteristics for the DLL

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Output Frequency Ranges				
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	5	240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	10	311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	0.3125	160	MHz
Output Clock Jitter <sup>(2,3,4)</sup>				
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division	-	±[1% of CLKIN period + 200]	ps

Table 29: Switching Characteristics for the DFS

Symbol	Description	Device	-4 Speed Grade		Units
			Min	Max	
Output Frequency Ranges					
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	All	5	311	MHz
Output Clock Jitter <sup>(2,3)</sup>					
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	Typ	Max	
			See Note 4		ps
			±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle <sup>(5,6)</sup>					
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	All	-	±[1% of CLKFX period + 400]	ps
Phase Alignment <sup>(6)</sup>					
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	All	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	All	-	±[1% of CLKFX period + 300]	ps
Lock Time					
LOCK_FX <sup>(2)</sup>	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	All	-	5	ms
			-	450	µs

**Notes:**

- The numbers in this table are based on the operating conditions set forth in Table 6 and Table 28.
- For optimal jitter tolerance and faster lock time, use the CLKIN\_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- Use the Spartan-3A Jitter Calculator ([www.xilinx.com/support/documentation/data\\_sheets/s3a\\_jitter\\_calc.zip](http://www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip)) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI. **Example:** The data sheet specifies a maximum jitter of "±[1% of CLKFX period + 300]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.

## Phase Shifter

Table 30: Recommended Operating Conditions for the PS in Variable Phase Mode

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F <sub>PSCLK</sub> )	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	-



Table 31: Switching Characteristics for the PS in Variable Phase Mode

Symbol	Description			Units
Phase Shifting Range				
MAX_STEPS <sup>(2)</sup>	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	$\pm \text{INTEGER}(10 \bullet (T_{\text{CLKIN}} - 3 \text{ ns}))$	steps
		CLKIN $\geq$ 60 MHz	$\pm \text{INTEGER}(15 \bullet (T_{\text{CLKIN}} - 3 \text{ ns}))$	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	$\pm [\text{MAX\_STEPS} \bullet \text{DCM\_DELAY\_STEP\_MIN}]$		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	$\pm [\text{MAX\_STEPS} \bullet \text{DCM\_DELAY\_STEP\_MAX}]$		ns

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 30.
2. The maximum variable phase shift range, MAX\_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE\_SHIFT attribute is set to 0.
3. The DCM\_DELAY\_STEP values are provided at the bottom of Table 27.

### Miscellaneous DCM Timing

Table 32: Miscellaneous DCM Timing

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN <sup>(1)</sup>	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX <sup>(2)</sup>	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME <sup>(3)</sup>	Maximum duration from V <sub>CCINT</sub> applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

**Notes:**

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM\_RESET specification. This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

## Slave Parallel Mode Timing

Table 39: Timing for the Slave Parallel Configuration Mode

Symbol	Description		-4 Speed Grade		Units		
			Min	Max			
Clock-to-Output Times							
T <sub>SMCKBY</sub>	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin		-	12.0	ns		
Setup Times							
T <sub>SMDCC</sub>	The time from the setup of data at the D0-D7 pins to the active edge the CCLK pin		11.0	-	ns		
T <sub>SMCSCC</sub>	Setup time on the CSI_B pin before the active edge of the CCLK pin		10.0	-	ns		
T <sub>SMCCW</sub> <sup>(2)</sup>	Setup time on the RDWR_B pin before active edge of the CCLK pin		23.0	-	ns		
Hold Times							
T <sub>SMCCD</sub>	The time from the active edge of the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	-	ns		
T <sub>SMCCCS</sub>	The time from the active edge of the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	-	ns		
T <sub>SMWCC</sub>	The time from the active edge of the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	-	ns		
Clock Timing							
T <sub>CCH</sub>	The High pulse width at the CCLK input pin		5	-	ns		
T <sub>CCL</sub>	The Low pulse width at the CCLK input pin		5	-	ns		
F <sub>CCPAR</sub>	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin <sup>(2)</sup>		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression		0	20	MHz	

### Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

## Byte Peripheral Interface Configuration Timing

Table 42: Timing for BPI Configuration Mode

Symbol	Description		Minimum	Maximum	Units
T <sub>CCLK1</sub>	Initial CCLK clock period		(see <a href="#">Table 34</a> )		
T <sub>CCLKn</sub>	CCLK clock period after FPGA loads ConfigRate setting		(see <a href="#">Table 34</a> )		
T <sub>INIT</sub>	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T <sub>INITM</sub>	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
T <sub>INITADDR</sub>	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	<b>BPI-UP:</b> (M[2:0]=<0:1:0>)	5	5	T <sub>CCLK1</sub> cycles
		<b>BPI-DN:</b> (M[2:0]=<0:1:1>)	2	2	
T <sub>CCO</sub>	Address A[23:0] outputs valid after CCLK falling edge		See <a href="#">Table 38</a>		
T <sub>DCC</sub>	Setup time on D[7:0] data inputs before CCLK rising edge		See <a href="#">Table 38</a>		
T <sub>CCD</sub>	Hold time on D[7:0] data inputs after CCLK rising edge		See <a href="#">Table 38</a>		

Table 43: Configuration Timing Requirements for Attached Parallel NOR Flash

Symbol	Description	Requirement	Units
$T_{CE}$ ( $t_{ELQV}$ )	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
$T_{OE}$ ( $t_{GLQV}$ )	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
$T_{ACC}$ ( $t_{AVQV}$ )	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
$T_{BYTE}$ ( $t_{FLQV}$ , $t_{FHQV}$ )	For x8/x16 PROMs only: BYTE# to output valid time <sup>(3)</sup>	$T_{BYTE} \leq T_{INITADDR}$	ns

### Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

## IEEE 1149.1/1553 JTAG Test Access Port Timing

Table 44: Timing for the JTAG Test Access Port

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T <sub>TCKTDO</sub>	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T <sub>TDITCK</sub>	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T <sub>TMSTCK</sub>	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T <sub>TCKTDI</sub>	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T <sub>TCKTMS</sub>	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T <sub>CCH</sub>	The High pulse width at the TCK pin	5	-	ns
T <sub>CCL</sub>	The Low pulse width at the TCK pin	5	-	ns
F <sub>TCK</sub>	Frequency of the TCK signal	-	25	MHz

### Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 6](#).

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/31/07	1.0	Initial Xilinx release.
01/20/09	1.1	<ul style="list-style-type: none"> <li>Updated <a href="#">"Key Feature Differences from Commercial XC Devices."</a></li> <li>Updated <math>T_{ACC}</math> requirement in <a href="#">Table 43</a>.</li> <li>Updated description of <math>T_{DCC}</math> and <math>T_{CCD}</math> in <a href="#">Table 42</a>.</li> <li>Removed Table 45: MultiBoot Trigger Timing.</li> </ul>
09/09/09	2.0	<ul style="list-style-type: none"> <li>Added package sizes to <a href="#">Table 2, page 4</a>.</li> <li>Removed Genealogy Viewer Link from <a href="#">"Package Marking," page 5</a>.</li> <li>Updated data and notes for <a href="#">Table 6, page 8</a>.</li> <li>Updated test conditions for <math>R_{PU}</math> and maximum value for <math>C_{IN}</math> in <a href="#">Table 7, page 8</a>.</li> <li>Updated notes for <a href="#">Table 8, page 9</a>.</li> <li>Updated Max <math>V_{CCO}</math> for LVTTTL and LVCMOS33, removed PCIX data, updated <math>V_{IL}</math> Max for LVCMOS18, LVCMOS15, and LVCMOS12, updated <math>V_{IH}</math> Min for LVCMOS12, and added note 6 in <a href="#">Table 9, page 11</a>.</li> <li>Removed PCIX data, revised note 2, and added note 4 in <a href="#">Table 10, page 12</a>.</li> <li>Updated figure description of <a href="#">Figure 5, page 14</a>.</li> <li>Added note 4 to <a href="#">Table 13, page 14</a>.</li> <li>Removed PC166_3 and PCIX adjustment values from <a href="#">Table 17, page 17</a>.</li> <li>Deleted Table 18 (duplicate of <a href="#">Table 17, page 17</a>). Subsequent tables renumbered.</li> <li>Removed PCIX data <a href="#">Table 18, page 18</a>.</li> <li>Removed PCIX data and removed <math>V_{REF}</math> values for DIFF_HSTL_I_18, DIFF_HSTL_III_18, DIFF_SSTL18_I, and DIFF_SSTL2_I from <a href="#">Table 19, page 19</a>.</li> <li>Updated <math>T_{DICK}</math> minimum setup time in <a href="#">Table 20, page 20</a>.</li> <li>Updated notes, references to notes, and revised the maximum clock-to-output times for <math>T_{MSCKP\_P}</math> <a href="#">Table 24, page 22</a>.</li> <li>Added <a href="#">"Spread Spectrum," page 24</a>.</li> <li>Updated note 3 in <a href="#">Table 26, page 25</a>.</li> <li>Added note 4 <a href="#">Table 28, page 26</a>.</li> <li>Updated notes, references to notes, and CLKOUT_PER_JITT_FX data in <a href="#">Table 29, page 27</a>.</li> <li>Updated MAX_STEPS data in <a href="#">Table 31, page 28</a>.</li> <li>Updated ConfigRate Setting for <math>T_{CCLK1}</math> to indicate 1 is the default value in <a href="#">Table 34, page 30</a>.</li> <li>Updated ConfigRate Setting for <math>F_{CCLK1}</math> to indicate 1 is the default value in <a href="#">Table 35, page 30</a>.</li> </ul>

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