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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	158
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s250e-4pqg208q

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS

Table 2: Available User I/Os and Differential (Diff) I/O Pairs

Package	VQG100		CPG	a132	TQC	à144	PQG	208	FTG	i256	FGG	3400	FGG	i484
Size (mm)	16 :	c 16	8	x 8	22 >	22 x 22		28 x 28		c 17	21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XA3S100E	66 (7)	30 (2)	83 (11)	35 (2)	108 (28)	40 (4)	-	-	-	-	-	-	-	-
XA3S250E	66 (7)	30 (2)	92 (7)	41 <i>(2)</i>	108 (28)	40 (4)	158 (32)	65 (5)	172 (40)	68 (8)	-	-	-	-
XA3S500E	-	-	92 (7)	41 <i>(2)</i>	-	-	158 (32)	65 (5)	190 (41)	77 (8)	-	-	-	-
XA3S1200E	-	-	-	-	-	-	-	-	190 (40)	77 (8)	304 (72)	124 (20)	-	-
XA3S1600E	-	-	-	-	-	-	-	-	-	-	304 (72)	124 (20)	376 (82)	156 (21)

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Differential HSTL (1.8V, Types I and III)

2.5V LVPECL inputs

Differential SSTL (2.5V and 1.8V, Type I)

Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of DS312.

2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.



Package Marking

Figure 2 provides a top marking example for XA Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for XA Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CPG132). The markings for the BGA packages are nearly identical to those

for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for XA Spartan-3E FPGAs in the CPG132 package.





Figure 2: XA Spartan-3E FPGA QFP Package Marking Example



Figure 3: XA Spartan-3E FPGA BGA Package Marking Example



Figure 4: XA Spartan-3E FPGA CPG132 Package Marking Example

Power Supply Specifications

Table 3: Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Мах	Units
V _{CCINTT}	Threshold for the V _{CCINT} supply	0.4	1.0	V
V _{CCAUXT}	Threshold for the V _{CCAUX} supply	0.8	2.0	V
V _{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.

2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
V _{CCINTR}	Ramp rate from GND to valid $V_{\mbox{CCINT}}$ supply level	0.2	50	ms
V _{CCAUXR}	Ramp rate from GND to valid $V_{\mbox{CCAUX}}$ supply level	0.2	50	ms
V _{CCO2R}	Ramp rate from GND to valid $\mathrm{V}_{\mathrm{CCO}}$ Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.

2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: Supply Voltage Levels Necessary for Preserving RAM Contents

Symbol	Description	Min	Units
V _{DRINT}	V _{CCINT} level required to retain RAM data	1.0	V
V _{DRAUX}	V _{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I _{CCAUXQ}	Quiescent V _{CCAUX}	XA3S100E	13	22	mA
supply current	XA3S250E	26	43	mA	
		XA3S500E	34	63	mA
		XA3S1200E	59	100	mA
		XA3S1600E	86	150	mA

Table 8: Quiescent Supply Current Characteristics (Continued)

Notes:

- 1. The numbers in this table are based on the conditions set forth in Table 6.
- The numbers in this table are based on the conditions set for the half of the conditions of the conditions of the conditions and the conditions of the condit
- There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The <u>Spartan-3E XPower Estimator</u> provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower <u>Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.</u>
- 4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.

Single-Ended I/O Standards

Table	<u>9</u> :	Recommended O	perating	Conditions for	or User I/Os	Usina Sin	ale-Ended	Standards
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IOSTANDARD	V _{CC}	_{CO} for Drive	rs ⁽²⁾		V _{REF}		V _{IL}	V _{IH}
Attribute	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465				0.8	2.0
LVCMOS33 ⁽⁴⁾	3.0	3.3	3.465				0.8	2.0
LVCMOS25 ^(4,5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95	V _{RE} the	_{EF} is not use se I/O stand	d for ards	0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3	3.0	3.3	3.465				0.3 * V _{CCO}	0.5 * V _{CCO}
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V _{REF} - 0.1	V _{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	- 1.1 -			V _{REF} - 0.1	V _{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833 0.900 0.969			V _{REF} - 0.125	V _{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V _{REF} - 0.125	V _{REF} + 0.125

Notes:

- 1. Descriptions of the symbols used in this table are as follows:

 - $\label{eq:V_CCO} V_{CCO} \text{the supply voltage for output drivers} \\ V_{REF} \text{the reference voltage for setting the input switching threshold} \\ V_{IL} \text{the input voltage that indicates a Low logic level} \\ V_{IH} \text{the input voltage that indicates a High logic level} \\ \end{array}$
- 2. The V_{CCO} rails supply only output drivers, not input circuits.
- For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 72 in DS312. З.
- There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards. 4.
- All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). 5. The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see www.xilinx.com/pci. 6.



Table 10: DC Characteristics of User I/Os UsingSingle-Ended Standards

		Te Cond	est itions	Logic Charac	: Level teristics
IOSTANDAR Attribute	D	I _{OL} (mA)	I _{OH} (mA)	V _{OL} Max (V)	V _{OH} Min (V)
LVTTL ⁽³⁾	2	2	-2	0.4	2.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
LVCMOS33 ⁽³⁾	2	2	-2	0.4	V _{CCO} – 0.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
LVCMOS25 ⁽³⁾	2	2	-2	0.4	V _{CCO} – 0.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
LVCMOS18 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
	4	4	-4		
	6	6	-6		
	8	8	-8		
LVCMOS15 ⁽³⁾	2	2	-2	0.4	V _{CCO} – 0.4
	4	4	-4		
	6	6	-6		

Table 10: DC Characteristics of User I/Os Using Single-Ended Standards (Continued)

		Te Cond	est itions	Logic Charac	gic Level racteristics		
IOSTANDARD Attribute		I _{OL} (mA)	I _{OH} (mA)	V _{OL} Max (V)	V _{OH} Min (V)		
LVCMOS12 ⁽³⁾ 2		2	-2	0.4	V _{CCO} - 0.4		
PCI33_3 ⁽⁴⁾		1.5	-0.5	10% V _{CCO}	90% V _{CCO}		
HSTL_I_18		8	-8	0.4	V _{CCO} - 0.4		
HSTL_III_18		24	-8	0.4	V _{CCO} - 0.4		
SSTL18_I		6.7	-6.7	V _{TT} – 0.475	V _{TT} + 0.475		
SSTL2_I		8.1	-8.1	V _{TT} – 0.61	V _{TT} + 0.61		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6 and Table 9.

2. Descriptions of the symbols used in this table are as follows: I_{OL} — the output current condition under which V_{OL} is tested I_{OH} — the output current condition under which V_{OH} is tested V_{OL} — the output voltage that indicates a Low logic level V_{OH} — the output voltage that indicates a High logic level V_{CCO} — the supply voltage for output drivers V_{TT} — the voltage applied to a resistor termination

- 3. For the LVCMOS and LVTTL standards: the same $\rm V_{OL}$ and $\rm V_{OH}$ limits apply for both the Fast and Slow slew attributes.
- Tested according to the relevant PCI specifications. For information on PCI IP solutions, see <u>www.xilinx.com/pci.</u>

Differential I/O Standards

	Vcc	_{CO} for Drive	rs ⁽¹⁾		V _{ID}		V _{ICM}			
IOSTANDARD Attribute	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)	
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2	
LVPECL_25 ⁽²⁾		Inputs Only		100	800	1000	0.5	1.2	2.0	
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4	
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1	
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1	
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1	
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5	

Table 11: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.

2. V_{REF} inputs are not used for any of the differential I/O standards.

Table 12: DC Characteristics of User I/Os Using Differential Signal Standards

		V _{OD}		ΔV	ОD		V _{OCM}		ΔV	ОСМ	V _{OH}	V _{OL}
IOSTANDARD Attribute	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Тур (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	-	-	1.125	-	1.375	-	-	-	-
BLVDS_25	250	350	450	-	-	-	1.20	-	-	-	_	-
MINI_LVDS_25	300	-	600	-	50	1.0	-	1.4	-	50	-	-
RSDS_25	100	-	400	-	-	1.1	-	1.4	-	-	-	-
DIFF_HSTL_I_18	-	-	-	-	-	-	-	-	-	-	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	-	-	-	-	-	-	-	-	-	-	V _{CCO} -0.4	0.4
DIFF_SSTL18_I	-	-	-	-	-	-	-	-	-	-	V _{TT} + 0.475	V _{TT} – 0.475
DIFF_SSTL2_I	-	-	_	-	-	-	-	-	-	-	V _{TT} + 0.61	V _{TT} – 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6, and Table 11.

2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 5 below.

3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25



Figure 5: External Termination Resistors for BLVDS Transmitter and BLVDS Receiver

Switching Characteristics

I/O Timing

Table 13: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

				-4 Speed Grade	
Symbol	Description	Conditions	Device	Max	Units
Clock-to-Outpu	t Times				
TICKOFDCM	When reading from the Output	LVCMOS25 ⁽²⁾ , 12mA	XA3S100E	2.79	ns
	Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	output drive, Fast slew rate, with DCM ⁽³⁾	XA3S250E	3.45	ns
			XA3S500E	3.46	ns
			XA3S1200E	3.46	ns
			XA3S1600E	3.45	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data	LVCMOS25 ⁽²⁾ , 12mA	XA3S100E	5.92	ns
		output drive, Fast slew rate, without DCM	XA3S250E	5.43	ns
	appearing at the Output pin. The		XA3S500E	5.51	ns
			XA3S1200E	5.94	ns
			XA3S1600E	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.

 This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 17. If the latter is true, *add* the appropriate Output adjustment from Table 18.

3. DCM output jitter is included in all measurements.

4. For minimums, use the values reported by the Xilinx timing analyzer.

Table 16: Propagation Times for the IOB Input Path

		II DF			-4 Speed Grade	
Symbol	Description	Conditions	VALUE	Device	Max	Units
Propagatio	on Times					
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0	0	All	2.25	ns
T _{IOPLID}	The time it takes for data to	LVCMOS25 ⁽²⁾ ,	2	XA3S100E	5.97	ns
	travel from the Input pin through	IFD_DELAY_VALUE = default software setting	3	XA3S250E	6.33	ns
	the input delay programmed		2	XA3S500E	6.49	ns
			5	XA3S1200E	8.15	ns
			4	XA3S1600E	7.16	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.

2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 17.

Table 17: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVCMOS25 to the Following	Add the Adjustment Below	
(IOSTANDARD)	-4 Speed Grade	Units
Single-Ended Standards		
LVTTL	0.43	ns
LVCMOS33	0.43	ns
LVCMOS25	0	ns
LVCMOS18	0.98	ns
LVCMOS15	0.63	ns
LVCMOS12	0.27	ns
PCI33_3	0.42	ns
HSTL_I_18	0.12	ns
HSTL_III_18	0.17	ns
SSTL18_I	0.30	ns
SSTL2_I	0.15	ns

Table 17: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVCMOS25 to the Following Signal Standard	Add the Adjustment Below	
(IOSTANDARD)	-4 Speed Grade	Units
Differential Standards		
LVDS_25	0.49	ns
BLVDS_25	0.39	ns
MINI_LVDS_25	0.49	ns
LVPECL_25	0.27	ns
RSDS_25	0.49	ns
DIFF_HSTL_I_18	0.49	ns
DIFF_HSTL_III_18	0.49	ns
DIFF_SSTL18_I	0.30	ns
DIFF_SSTL2_I	0.32	ns

Notes:

- 1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
- 2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	-
			-4 Speed Grade	Units
Single-Ended	Standards		I	
LVTTL	Slow	2 mA	5.41	ns
		4 mA	2.41	ns
		6 mA	1.90	ns
		8 mA	0.67	ns
		12 mA	0.70	ns
		16 mA	0.43	ns
	Fast	2 mA	5.00	ns
		4 mA	1.96	ns
		6 mA	1.45	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS33	Slow	2 mA	5.29	ns
		4 mA	1.89	ns
		6 mA	1.04	ns
		8 mA	0.69	ns
		12 mA	0.42	ns
		16 mA	0.43	ns
	Fast	2 mA	4.87	ns
		4 mA	1.52	ns
		6 mA	0.39	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS25	Slow	2 mA	4.21	ns
		4 mA	2.26	ns
		6 mA	1.52	ns
		8 mA	1.08	ns
		12 mA	0.68	ns
	Fast	2 mA	3.67	ns
		4 mA	1.72	ns
		6 mA	0.46	ns
		8 mA	0.21	ns
		12 mA	0	ns

Table 18: Output Timing Adjustments for IOB

Table 18: Output Timing Adjustments for IOB (Continued)

Convert Output Time from LVCMOS25 with 12mA Drive and East Slow Pate to the Following			Add the Adjustment Below	
Signal Standa	rd (IOSTA	NDARD)	Grade	Units
LVCMOS18	Slow	2 mA	5.24	ns
4 mA 6 mA		4 mA	3.21	ns
		6 mA	2.49	ns
		8 mA	1.90	ns
	Fast	2 mA	4.15	ns
		4 mA	2.13	ns
		6 mA	1.14	ns
		8 mA	0.75	ns
LVCMOS15	Slow	2 mA	4.68	ns
		4 mA	3.97	ns
		6 mA	3.11	ns
	Fast	2 mA	3.38	ns
		4 mA	2.70	ns
		6 mA	1.53	ns
LVCMOS12	Slow	2 mA	6.63	ns
	Fast	2 mA	4.44	ns
HSTL_I_18			0.34	ns
HSTL_III_18			0.55 ns	
PCI33_3			0.46	ns
SSTL18_I			0.25	ns
SSTL2_I			-0.20	ns
Differential Star	ndards			
LVDS_25			-0.55	ns
BLVDS_25			0.04	ns
MINI_LVDS_25			-0.56	ns
LVPECL_25			Input Only	ns
RSDS_25			-0.48	ns
DIFF_HSTL_I_18			0.42	ns
DIFF_HSTL_III_	18		0.55	ns
DIFF_SSTL18_I			0.40	ns
DIFF_SSTL2_I			0.44	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.

 These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Table	19:	Test Methods	for	Timing	Measurement	at	I/Os
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Signal Standard			Inputs		Out	Inputs and Outputs	
(IOSTA	NDARD)	V _{REF} (V)	V _L (V)	V _H (V)	R_T (Ω)	V _T (V)	V _M (V)
Single-Ende	d	·					
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18	1	0.9	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
HSTL_III_18		1.1	V _{REF} – 0.5	V _{REF} + 0.5	50	1.8	V _{REF}
SSTL18_I		0.9	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{REF}
SSTL2_I		1.25	V _{REF} – 0.75	V _{REF} + 0.75	50	1.25	V _{REF}
Differential							
LVDS_25		-	V _{ICM} – 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
BLVDS_25		-	V _{ICM} – 0.125	V _{ICM} + 0.125	1M	0	V _{ICM}
MINI_LVDS_2	25	-	V _{ICM} – 0.125	V _{ICM} + 0.125	50	1.2	V _{ICM}
LVPECL_25		-	V _{ICM} – 0.3	V _{ICM} + 0.3	1M	0	V _{ICM}
RSDS_25		-	V _{ICM} – 0.1	V _{ICM} + 0.1	50	1.2	V _{ICM}
DIFF_HSTL_I_18		-	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{ICM}
DIFF_HSTL_	III_18	-	V _{REF} – 0.5	V _{REF} + 0.5	50	1.8	V _{ICM}
DIFF_SSTL1	8_I	-	V _{REF} – 0.5	V _{REF} + 0.5	50	0.9	V _{ICM}
DIFF_SSTL2	_	-	V _{REF} – 0.5	V _{REF} + 0.5	50	1.25	V _{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:

 $V_{\mbox{\scriptsize REF}}$ – The reference voltage for setting the input switching threshold

 V_{ICM} – The common mode input voltage V_M – Voltage of measurement point on signal transition V_L – Low-level test voltage at Input pin V_H – High-level test voltage at Input pin

 R_T – Effective termination resistance, which takes on a value of 1M Ω when no parallel termination is required

V_T – Termination voltage

The load capacitance (C₁) at the Output pin is 0 pF for all signal standards. 2.

З. According to the PCI specification.

Clock Buffer/Multiplexer Switching Characteristics

Table 23: Clock Distribution Switching Characteristics

		Maximum	
Description	Symbol	-4 Speed Grade	Units
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T _{GIO}	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T _{GSI}	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F _{BUFG}	311	MHz

18 x 18 Embedded Multiplier Timing

Table 24: 18 x 18 Embedded Multiplier Timing

		-4 Spee		
Symbol	Description	Min	Max	Units
Combinatorial	Delay			
T _{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.88 ⁽¹⁾	ns
Clock-to-Outpu	t Times			
T _{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ⁽²⁾	-	1.10	ns
Т _{MSCKP_A} Т _{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ⁽³⁾	-	4.97	ns
Setup Times				
T _{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽²⁾	3.98	-	ns
T _{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register $^{\rm (3)}$	0.23	-	ns
T _{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register $^{\rm (3)}$	0.39	-	ns
Hold Times				
T _{MSCKD_P}	Data hold time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽²⁾	-0.97		
T _{MSCKD_A}	Data hold time at the A input before the active transition at the CLK when using the AREG input register $^{\rm (3)}$	0.04		
T _{MSCKD_B}	Data hold time at the B input before the active transition at the CLK when using the BREG input register $^{\rm (3)}$	0.05		

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Table 25: Block RAM Timing (Continued)

	-4 Spe							
Symbol	Description	Min	Max	Units				
Clock Timing		,	,	,				
T _{BPWH}	High pulse width of the CLK signal	1.59	-	ns				
T _{BPWL}	Low pulse width of the CLK signal	1.59	-	ns				
Clock Frequency								
F _{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster.	0	230	MHz				

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 26 and Table 27) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 28 through Table 31) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 26 and Table 27.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See <u>XAPP469</u>, *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop

Table 26: Recommended Operating Conditions for the DLL

				-4 Spee		
	Symbol	Des	scription	Min	Max	Units
Input Fr	equency Ranges					
F _{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock in	Frequency of the CLKIN clock input			MHz
Input Pu	Ise Requirements	-			•	
CLKIN_PULSE		CLKIN pulse width as a	F _{CLKIN} ≤ 150 MHz	40%	60%	-
		percentage of the CLKIN period	F _{CLKIN} > 150 MHz	45%	55%	-
Input Cl	ock Jitter Tolerance and	I Delay Path Variation ⁽⁴⁾				
CLKIN_C	CYC_JITT_DLL_LF	Cycle-to-cycle jitter at the	F _{CLKIN} ≤ 150 MHz	-	±300	ps
CLKIN_C	CYC_JITT_DLL_HF	CLKIN input	F _{CLKIN} > 150 MHz	-	±150	ps
CLKIN_F	PER_JITT_DLL	Period jitter at the CLKIN input	Period jitter at the CLKIN input			ns
CLKFB_	DELAY_VAR_EXT	Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input			±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.

2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 28.

3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.

4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 27: Switching Characteristics for the DLL

		-4 Spe	ed Grade	_
Symbol	Description	Min	Max	Units
Output Frequency Ranges	•			
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	5	240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	10	311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	0.3125	160	MHz
Output Clock Jitter ^(2,3,4)	1	L	I	
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division	-	±[1% of CLKIN period + 200]	ps

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Table 27: Switching Characteristics for the DLL (Continued)

			-4 Speed Grade		
Symbol	Description	-	Min	Max	Units
Duty Cycle ⁽⁴⁾	·				
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CL CLK270, CLK2X, CLK2X180, and CL including the BUFGMUX and clock tr distortion	K90, CLK180, KDV outputs, ee duty-cycle	-	±[1% of CLKIN period + 400]	ps
Phase Alignment ⁽⁴⁾					
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and	I CLKFB inputs	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	-	±[1% of CLKIN period + 100]	ps
		All others	-	±[1% of CLKIN period + 200]	ps
Lock Time		· · · · ·			
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's Reset	$\begin{array}{c} 5 \text{ MHz} \leq \text{F}_{\text{CLKIN}} \leq \\ 15 \text{ MHz} \end{array}$	-	5	ms
	Input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	F _{CLKIN} > 15 MHz	-	600	μs
Delay Lines					
DCM_DELAY_STEP	Finest delay resolution		20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 26.

- 2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
- 3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. *Example:* The data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.

Digital Frequency Synthesizer

Table 28: Recommended Operating Conditions for the DFS

				-4 Speed Grade		
	Symbol	Description		Min	Max	Units
Input Freque						
F _{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333 ⁽⁴⁾	MHz
Input Clock	Jitter Tolerance ⁽³⁾					
CLKIN_CYC	_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN	F _{CLKFX} ≤ 150 MHz	-	±300	ps
CLKIN_CYC_JITT_FX_HF		input, based on CLKFX output frequency	F _{CLKFX} > 150 MHz	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.

2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 26.

3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

 To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Configuration and JTAG Timing

Table 33: Power-On Timing and the Beginning of Configuration

			-4 Speed Grade			
Symbol	Description	Device	Min	Max	Units	
T _{POR} ⁽²⁾	The time from the application of $V_{CCINT}\!, V_{CCAUX}\!,$ and V_{CCO}	XA3S100E	-	5	ms	
	Bank 2 supply voltage ramps (whichever occurs last) to the	XA3S250E	-	5	ms	
		XA3S500E	-	5	ms	
		XA3S1200E	-	5	ms	
		XA3S1600E	-	7	ms	
T _{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	μs	
T _{PL} ⁽²⁾	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XA3S100E	-	0.5	ms	
		XA3S250E	-	0.5	ms	
		XA3S500E	-	1	ms	
		XA3S1200E	-	2	ms	
		XA3S1600E	-	2	ms	
T _{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns	
T _{ICCK} ⁽³⁾	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	μs	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6. This means power must be applied to all V_{CCINT} , V_{CCO} , and V_{CCAUX} lines.

2. Power-on reset and the clearing of configuration memory occurs during this period.

3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.



Configuration Clock (CCLK) Characteristics

Symbol	Description	<i>ConfigRate</i> Setting	Temperature Range	Minimum	Maximum	Units
T _{CCLK1}	CCLK clock period by <i>ConfigRate</i> setting	1 (power-on value and default value)	I-Grade Q-Grade	485	1,250	ns
T _{CCLK3}		3	I-Grade Q-Grade	242	625	ns
T _{CCLK6}		6	I-Grade Q-Grade	121	313	ns
T _{CCLK12}		12	I-Grade Q-Grade	60.6	157	ns
T _{CCLK25}		25	I-Grade Q-Grade	30.3	78.2	ns
T _{CCLK50}		50	I-Grade Q-Grade	15.1	39.1	ns

Table 34: Master Mode CCLK Output Period by ConfigRate Option Setting

Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in <u>DS312</u>, Module 2.

Table	35:	Master	Mode CCLK C	Output Free	quency by	ConfigR	ate Option Sett	ing

Symbol	Description	ConfigRate Setting	Temperature Range	Minimum	Maximum	Units
F _{CCLK1}	Equivalent CCLK clock frequency by <i>ConfigRate</i> setting	1 (power-on value and default value)	I-Grade Q-Grade	0.8	2.1	MHz
F _{CCLK3}		3	I-Grade Q-Grade	1.6	4.2	MHz
F _{CCLK6}		6	I-Grade Q-Grade	3.2	8.3	MHz
F _{CCLK12}		12	I-Grade Q-Grade	6.4	16.5	MHz
F _{CCLK25}		25	I-Grade Q-Grade	12.8	33.0	MHz
F _{CCLK50}		50	I-Grade Q-Grade	25.6	66.0	MHz

Table 36: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description		ConfigRate Setting						Unito
	Description	1	3	6	12	25	50	Units	
T _{MCCL,} T _{MCCH}	Master mode CCLK minimum Low and High time	I-Grade Q-Grade	235	117	58	29.3	14.5	7.3	ns

Table 37: Slave Mode CCLK Input Low and High Time

Symbol	Description	Min	Max	Units
T _{SCCL,} T _{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

Table	38:	Timing for	r the Master	Serial and	Slave Serial	Configuration	Modes
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			Slave/	-4 Spee	d Grade		
Symbol	Descri	ption	Master	Min	Max	Units	
Clock-to-C	Output Times						
T _{CCO}	The time from the falling transition appearing at the DOUT pin	on the CCLK pin to data	Both	1.5	10.0	ns	
Setup Tim	es						
T _{DCC}	The time from the setup of data at the CCLK pin	Both	11.0	-	ns		
Hold Times							
T _{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin			0	-	ns	
Clock Tim	ing						
т _{ссн}	High pulse width at the CCLK inpu	ut pin	Master	Se	e Table 36		
			Slave	Se	e Table 37		
T _{CCL}	Low pulse width at the CCLK input	t pin	Master	Se	e Table 36		
				See Table 37			
F _{CCSER}	Frequency of the clock signal at	No bitstream compression	Slave	0	66 ⁽²⁾	MHz	
	the CCLK input pin	With bitstream compression		0	20	MHz	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.



Serial Peripheral Interface Configuration Timing

Table	40:	Timina	for	SPI	Configuration	Mode
10010				••••	•••ingalation	

Symbol	Description	Minimum	Maximum	Units
T _{CCLK1}	Initial CCLK clock period	(see Table 34)		
T _{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	(see Table 34)		
T _{MINIT}	Setup time on VS[2:0] and M[2:0] mode pins before the rising edge of INIT_B	50	-	ns
T _{INITM}	Hold time on VS[2:0] and M[2:0]mode pins after the rising edge of INIT_B $\ensuremath{NIT_B}$	0	-	ns
T _{CCO}	MOSI output valid after CCLK edge	See Table 38		
T _{DCC}	Setup time on DIN data input before CCLK edge	See Table 38		
T _{CCD}	Hold time on DIN data input after CCLK edge	See Table 38		

Table 41: Configuration Timing Requirements for Attached SPI Serial Flash

Symbol	Description	Requirement	Units
T _{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T _{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T _{DH}	SPI serial Flash PROM data input hold time	T _{DH} ≤T _{MCCH1}	ns
T _V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f _C or f _R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_{C} \ge \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.

2. Subtract additional printed circuit board routing delay as required by the application.

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