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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	108
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s250e-4tqg144q

Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specification over the T_J = –40°C to +125°C temperature range (Q-Grade)
- XA Spartan-3E devices are available in the -4 speed grade only.
- PCI-66 is not supported in the XA Spartan-3E FPGA product line.
- The readback feature is not supported in the XA Spartan-3E FPGA product line.
- XA Spartan-3E devices are available in Step 1 only.
- JTAG configuration frequency reduced from 30 MHz to 25 MHz.
- Platform Flash is not supported within the XA family.
- XA Spartan-3E devices are available in Pb-free packaging only.
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3E device must be power cycled prior to reconfiguration.

Table 1: **Summary of XA Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XA3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XA3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XA3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	190	77
XA3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XA3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

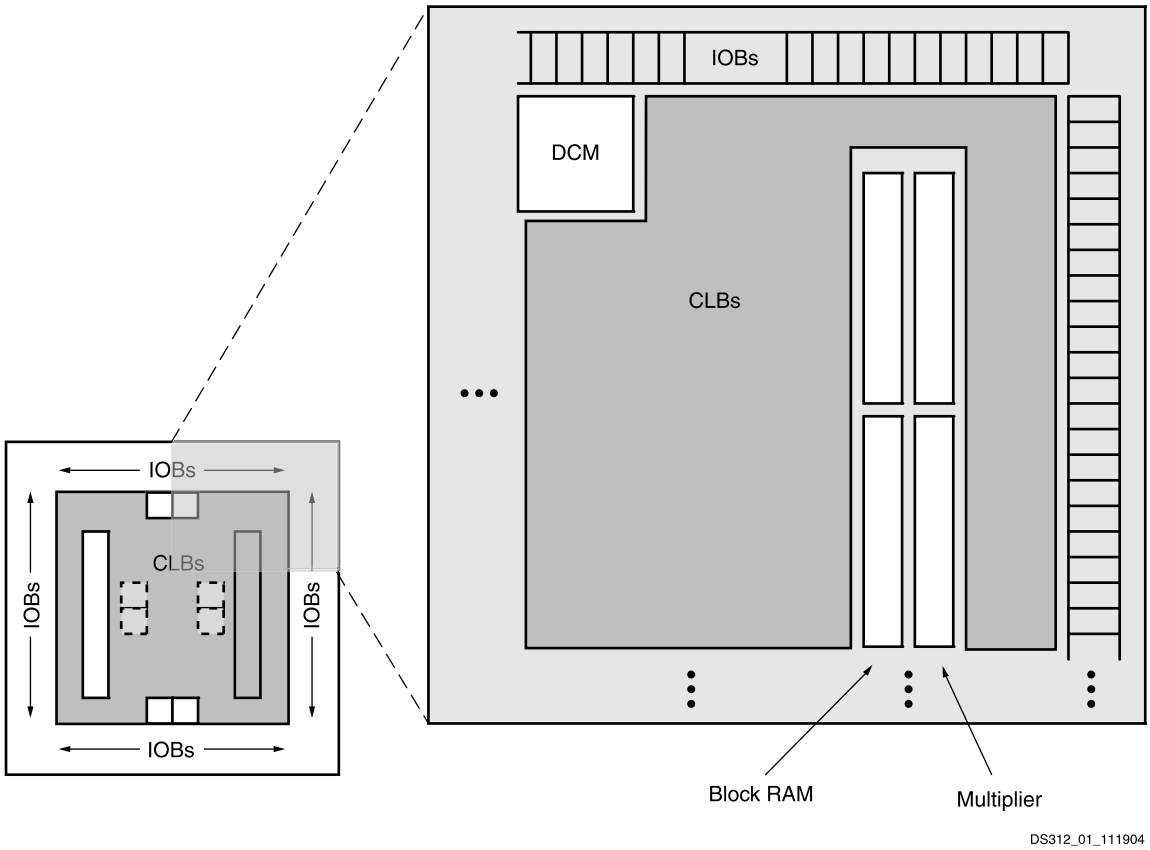
Architectural Overview

The XA Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XA3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XA3S100E has only one DCM at the top and bottom, while the XA3S1200E and XA3S1600E add two DCMs in the middle of the left and right sides.

The XA Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XA3S1200E and XA3S1600E have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XA3S100E has only one DCM at the top and one at the bottom.

Figure 1: **XA Spartan-3E Family Architecture**

Configuration

XA Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

I/O Capabilities

The XA Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

XA Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

XA Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQG100		CPG132		TQG144		PQG208		FTG256		FGG400		FGG484	
Size (mm)	16 x 16		8 x 8		22 x 22		28 x 28		17 x 17		21 x 21		23 x 23	
Device	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XA3S100E	**66** *(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-
XA3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-
XA3S500E	-	-	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	-	-	-	-
XA3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**304** *(72)*	**124** *(20)*	-	-
XA3S1600E	-	-	-	-	-	-	-	-	-	-	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All XA Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4: Pinout Descriptions of DS312.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.

Package Marking

Figure 2 provides a top marking example for XA Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for XA Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for XA Spartan-3E FPGAs in the CPG132 package.

Note: **No marking is shown for stepping.**

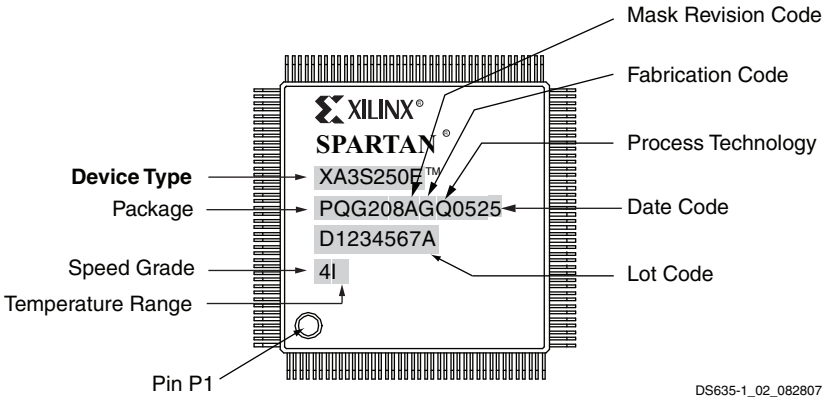


Figure 2: **XA Spartan-3E FPGA QFP Package Marking Example**

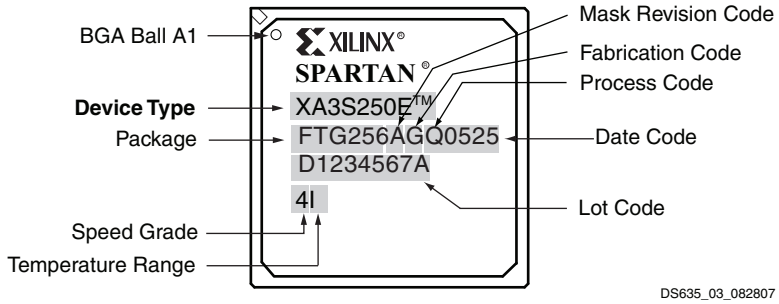


Figure 3: **XA Spartan-3E FPGA BGA Package Marking Example**

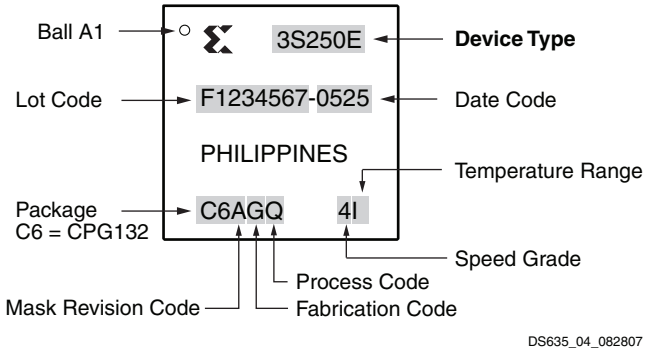
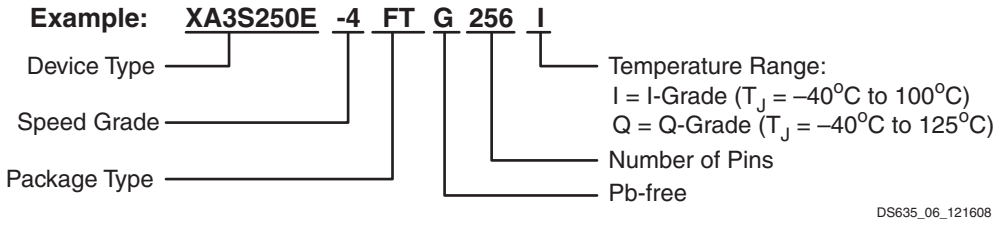


Figure 4: **XA Spartan-3E FPGA CPG132 Package Marking Example**

Ordering Information

XA Spartan-3E FPGAs are available in Pb-free packaging options for all device/package combinations. All devices are in Pb-free packages only, with a “G” character to the ordering code. All devices are available in either I-Grade or Q-Grade temperature ranges. Only the -4 speed grade is available for the XA Spartan-3E family. See Table 2 for valid device/package combinations.

Pb-Free Packaging



Device
XA3S100E
XA3S250E
XA3S500E
XA3S1200E
XA3S1600E

Speed Grade	
-4	Only

Package Type / Number of Pins	
VQG100	100-pin Very Thin Quad Flat Pack (VQFP)
CPG132	132-ball Chip-Scale Package (CSP)
TQG144	144-pin Thin Quad Flat Pack (TQFP)
PQG208	208-pin Plastic Quad Flat Pack (PQFP)
FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)
FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
I	I-Grade (–40°C to 100°C)
Q	Q-Grade (–40°C to 125°C)

Power Supply Specifications

Table 3: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 4: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Table 7: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins *(Continued)***

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_{RPD}(2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	$V_{IN} = V_{CCO}$	0.10	–	0.75	mA
R_{PD}(2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	$V_{IN} = V_{CCO}$ = 3.0V to 3.45V	4.0	–	34.5	kΩ
		$V_{IN} = V_{CCO}$ = 2.3V to 2.7V	3.0	–	27.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.7V to 1.9V	2.3	–	19.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.4V to 1.6V	1.8	–	16.0	kΩ
		$V_{IN} = V_{CCO}$ = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	-	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 6.
2. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.

Table 8: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	I-Grade Maximum	Q-Grade Maximum	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3S100E	36	58	mA
		XA3S250E	104	158	mA
		XA3S500E	145	300	mA
		XA3S1200E	324	500	mA
		XA3S1600E	457	750	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3S100E	1.5	2.0	mA
		XA3S250E	1.5	3.0	mA
		XA3S500E	1.5	3.0	mA
		XA3S1200E	2.5	4.0	mA
		XA3S1600E	2.5	4.0	mA

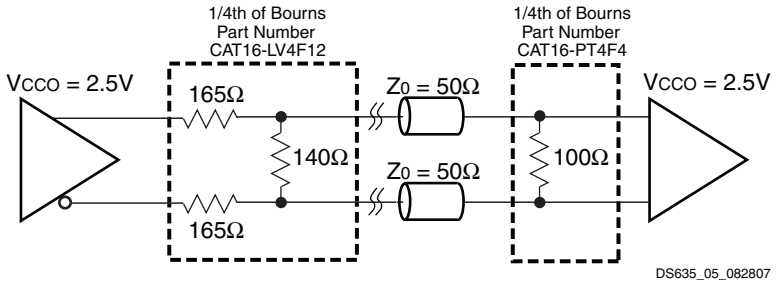


Figure 5: **External Termination Resistors for BLVDS Transmitter and BLVDS Receiver**

Switching Characteristics

I/O Timing

Table 13: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	-4 Speed Grade	Units
				Max	
Clock-to-Output Times					
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	**XA3S100E**	2.79	ns
			XA3S250E	3.45	ns
			XA3S500E	3.46	ns
			XA3S1200E	3.46	ns
			XA3S1600E	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	**XA3S100E**	5.92	ns
			XA3S250E	5.43	ns
			XA3S500E	5.51	ns
			XA3S1200E	5.94	ns
			XA3S1600E	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 17. If the latter is true, *add* the appropriate Output adjustment from Table 18.
3. DCM output jitter is included in all measurements.
4. For minimums, use the values reported by the Xilinx timing analyzer.

Table 15: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade Min	Units
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	6.49	ns
			3	**XA3S250E**	6.85	ns
			2	**XA3S500E**	7.01	ns
			5	**XA3S1200E**	8.67	ns
			4	**XA3S1600E**	7.69	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	–0.76	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	–3.93	ns
			3	**XA3S250E**	–3.51	ns
			2	**XA3S500E**	–3.74	ns
			5	**XA3S1200E**	–4.30	ns
			4	**XA3S1600E**	–4.14	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 17.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 17. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 16: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	-4 Speed Grade	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	**XA3S100E**	5.97	ns
			3	**XA3S250E**	6.33	ns
			2	**XA3S500E**	6.49	ns
			5	**XA3S1200E**	8.15	ns
			4	**XA3S1600E**	7.16	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6 and Table 9.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 17.

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Single-Ended Standards		
LVTTL	0.43	ns
LVCMOS33	0.43	ns
LVCMOS25	0	ns
LVCMOS18	0.98	ns
LVCMOS15	0.63	ns
LVCMOS12	0.27	ns
PCI33_3	0.42	ns
HSTL_I_18	0.12	ns
HSTL_III_18	0.17	ns
SSTL18_I	0.30	ns
SSTL2_I	0.15	ns

Table 17: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	-4 Speed Grade	
Differential Standards		
LVDS_25	0.49	ns
BLVDS_25	0.39	ns
MINI_LVDS_25	0.49	ns
LVPECL_25	0.27	ns
RSDS_25	0.49	ns
DIFF_HSTL_I_18	0.49	ns
DIFF_HSTL_III_18	0.49	ns
DIFF_SSTL18_I	0.30	ns
DIFF_SSTL2_I	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 18: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below: -4 Speed Grade	Units
Single-Ended Standards				
LVTTL	Slow	2 mA	5.41	ns
		4 mA	2.41	ns
		6 mA	1.90	ns
		8 mA	0.67	ns
		12 mA	0.70	ns
		16 mA	0.43	ns
	Fast	2 mA	5.00	ns
		4 mA	1.96	ns
		6 mA	1.45	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS33	Slow	2 mA	5.29	ns
		4 mA	1.89	ns
		6 mA	1.04	ns
		8 mA	0.69	ns
		12 mA	0.42	ns
		16 mA	0.43	ns
	Fast	2 mA	4.87	ns
		4 mA	1.52	ns
		6 mA	0.39	ns
		8 mA	0.34	ns
		12 mA	0.30	ns
		16 mA	0.30	ns
LVCMOS25	Slow	2 mA	4.21	ns
		4 mA	2.26	ns
		6 mA	1.52	ns
		8 mA	1.08	ns
		12 mA	0.68	ns
	Fast	2 mA	3.67	ns
		4 mA	1.72	ns
		6 mA	0.46	ns
		8 mA	0.21	ns
		12 mA	0	ns

Table 18: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below: -4 Speed Grade	Units
LVCMOS18	Slow	2 mA	5.24	ns
		4 mA	3.21	ns
		6 mA	2.49	ns
		8 mA	1.90	ns
	Fast	2 mA	4.15	ns
		4 mA	2.13	ns
		6 mA	1.14	ns
		8 mA	0.75	ns
LVCMOS15	Slow	2 mA	4.68	ns
		4 mA	3.97	ns
		6 mA	3.11	ns
	Fast	2 mA	3.38	ns
		4 mA	2.70	ns
		6 mA	1.53	ns
LVCMOS12	Slow	2 mA	6.63	ns
	Fast	2 mA	4.44	ns
HSTL_I_18			0.34	ns
HSTL_III_18			0.55	ns
PCI33_3			0.46	ns
SSTL18_I			0.25	ns
SSTL2_I			–0.20	ns
Differential Standards				
LVDS_25			–0.55	ns
BLVDS_25			0.04	ns
MINI_LVDS_25			–0.56	ns
LVPECL_25			Input Only	ns
RSDS_25			–0.48	ns
DIFF_HSTL_I_18			0.42	ns
DIFF_HSTL_III_18			0.55	ns
DIFF_SSTL18_I			0.40	ns
DIFF_SSTL2_I			0.44	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 19 and are based on the operating conditions set forth in Table 6, Table 9, and Table 11.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Configurable Logic Block Timing

Table 20: **CLB (SLICEM) Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.60	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.81	-	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	572	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.76	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Clock Buffer/Multiplexer Switching Characteristics

Table 23: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum	Units
		-4 Speed Grade	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	311	MHz

18 x 18 Embedded Multiplier Timing

Table 24: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Combinatorial Delay				
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.88(1)	ns
Clock-to-Output Times				
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.97	ns
Setup Times				
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.39	-	ns
Hold Times				
T_{MSCKD_P}	Data hold time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	-0.97		
T_{MSCKD_A}	Data hold time at the A input before the active transition at the CLK when using the AREG input register(3)	0.04		
T_{MSCKD_B}	Data hold time at the B input before the active transition at the CLK when using the BREG input register(3)	0.05		

Table 25: **Block RAM Timing *(Continued)***

Symbol	Description	-4 Speed Grade		Units
		Min	Max	
Clock Timing				
T_{BPWH}	High pulse width of the CLK signal	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.59	-	ns
Clock Frequency				
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift registers and circular buffers. Write-only or read-only performance is faster.	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.

Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 26 and Table 27) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 28 through Table 31) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 26 and Table 27.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop

Table 26: **Recommended Operating Conditions for the DLL**

Symbol		Description		-4 Speed Grade Min	-4 Speed Grade Max	Units
Input Frequency Ranges						
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	240(3)	MHz
Input Pulse Requirements						
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz	40%	60%	-
			$F_{CLKIN} > 150$ MHz	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation(4)						
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz	-	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	-	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		-	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		-	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 28.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.

Table 27: **Switching Characteristics for the DLL**

Symbol	Description	-4 Speed Grade Min	-4 Speed Grade Max	Units
Output Frequency Ranges				
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	5	240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	10	311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	0.3125	160	MHz
Output Clock Jitter(2,3,4)				
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division	-	±[1% of CLKIN period + 200]	ps

Table 31: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description			Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 6 and Table 30.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 27.

Miscellaneous DCM Timing

Table 32: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
		N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes
		N/A	N/A	minutes

Notes:
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specification. This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Slave Parallel Mode Timing

Table 39: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description			-4 Speed Grade		Units
				Min	Max	
Clock-to-Output Times						
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin			-	12.0	ns
Setup Times						
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the active edge the CCLK pin			11.0	-	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the active edge of the CCLK pin			10.0	-	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before active edge of the CCLK pin			23.0	-	ns
Hold Times						
T_{SMCCD}	The time from the active edge of the CCLK pin to the point when data is last held at the D0-D7 pins			1.0	-	ns
T_{SMCCCS}	The time from the active edge of the CCLK pin to the point when a logic level is last held at the CSO_B pin			0	-	ns
T_{SMWCC}	The time from the active edge of the CCLK pin to the point when a logic level is last held at the RDWR_B pin			0	-	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 6.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Byte Peripheral Interface Configuration Timing

Table 42: **Timing for BPI Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		(see Table 34)		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		(see Table 34)		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	**BPI-UP:** (M[2:0]=<0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0]=<0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 38		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 38		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 38		

Table 43: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/31/07	1.0	Initial Xilinx release.
01/20/09	1.1	• Updated "Key Feature Differences from Commercial XC Devices." • Updated T_{ACC} requirement in Table 43. • Updated description of T_{DCC} and T_{CCD} in Table 42. • Removed Table 45: MultiBoot Trigger Timing.
09/09/09	2.0	• Added package sizes to Table 2, page 4. • Removed Genealogy Viewer Link from "Package Marking," page 5. • Updated data and notes for Table 6, page 8. • Updated test conditions for R_{PU} and maximum value for C_{IN} in Table 7, page 8. • Updated notes for Table 8, page 9. • Updated Max V_{CCO} for LVTTL and LVCMOS33, removed PCIX data, updated V_{IL} Max for LVCMOS18, LVCMOS15, and LVCMOS12, updated V_{IH} Min for LVCMOS12, and added note 6 in Table 9, page 11. • Removed PCIX data, revised note 2, and added note 4 in Table 10, page 12. • Updated figure description of Figure 5, page 14. • Added note 4 to Table 13, page 14. • Removed PC166_3 and PCIX adjustment values from Table 17, page 17. • Deleted Table 18 (duplicate of Table 17, page 17). Subsequent tables renumbered. • Removed PCIX data Table 18, page 18. • Removed PCIX data and removed V_{REF} values for DIFF_HSTL_I_18, DIFF_HSTL_III_18, DIFF_SSTL18_I, and DIFF_SSTL2_I from Table 19, page 19. • Updated T_{DICK} minimum setup time in Table 20, page 20. • Updated notes, references to notes, and revised the maximum clock-to-output times for T_{MSCKP_P} Table 24, page 22. • Added "Spread Spectrum," page 24. • Updated note 3 in Table 26, page 25. • Added note 4 Table 28, page 26. • Updated notes, references to notes, and CLKOUT_PER_JITT_FX data in Table 29, page 27. • Updated MAX_STEPS data in Table 31, page 28. • Updated ConfigRate Setting for T_{CCLK1} to indicate 1 is the default value in Table 34, page 30. • Updated ConfigRate Setting for F_{CCLK1} to indicate 1 is the default value in Table 35, page 30.

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