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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212c7snfp-v2

1.2 Product List

Table 1.5 lists Product List for R8C/2C Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2C Group, Table 1.6 lists Product List for R8C/2D Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2D Group.

Table 1.5 Product List for R8C/2C Group

Current of Dec. 2007

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks		
R5F212C7SNFP	48 Kbytes	2.5 Kbytes	PLQP0080KB-A	N version		
R5F212C8SNFP	64 Kbytes	3 Kbytes	PLQP0080KB-A			
R5F212CASNFP	96 Kbytes	7 Kbytes	PLQP0080KB-A			
R5F212CCSNFP	128 Kbytes	7.5 Kbytes	PLQP0080KB-A			
R5F212C7SDFP	48 Kbytes	2.5 Kbytes	PLQP0080KB-A	D version		
R5F212C8SDFP	64 Kbytes	3 Kbytes	PLQP0080KB-A			
R5F212CASDFP	96 Kbytes	7 Kbytes	PLQP0080KB-A			
R5F212CCSDFP	128 Kbytes	7.5 Kbytes	PLQP0080KB-A			
R5F212C7SNXXXFP	48 Kbytes	2.5 Kbytes	PLQP0080KB-A	N version	Factory programming product ⁽¹⁾	
R5F212C8SNXXXFP	64 Kbytes	3 Kbytes	PLQP0080KB-A			
R5F212CASNXXXFP	96 Kbytes	7 Kbytes	PLQP0080KB-A			
R5F212CCSNXXXFP	128 Kbytes	7.5 Kbytes	PLQP0080KB-A			
R5F212C7SDXXXFP	48 Kbytes	2.5 Kbytes	PLQP0080KB-A	D version		
R5F212C8SDXXXFP	64 Kbytes	3 Kbytes	PLQP0080KB-A			
R5F212CASDXXXFP	96 Kbytes	7 Kbytes	PLQP0080KB-A			
R5F212CCSDXXXFP	128 Kbytes	7.5 Kbytes	PLQP0080KB-A			

NOTE:

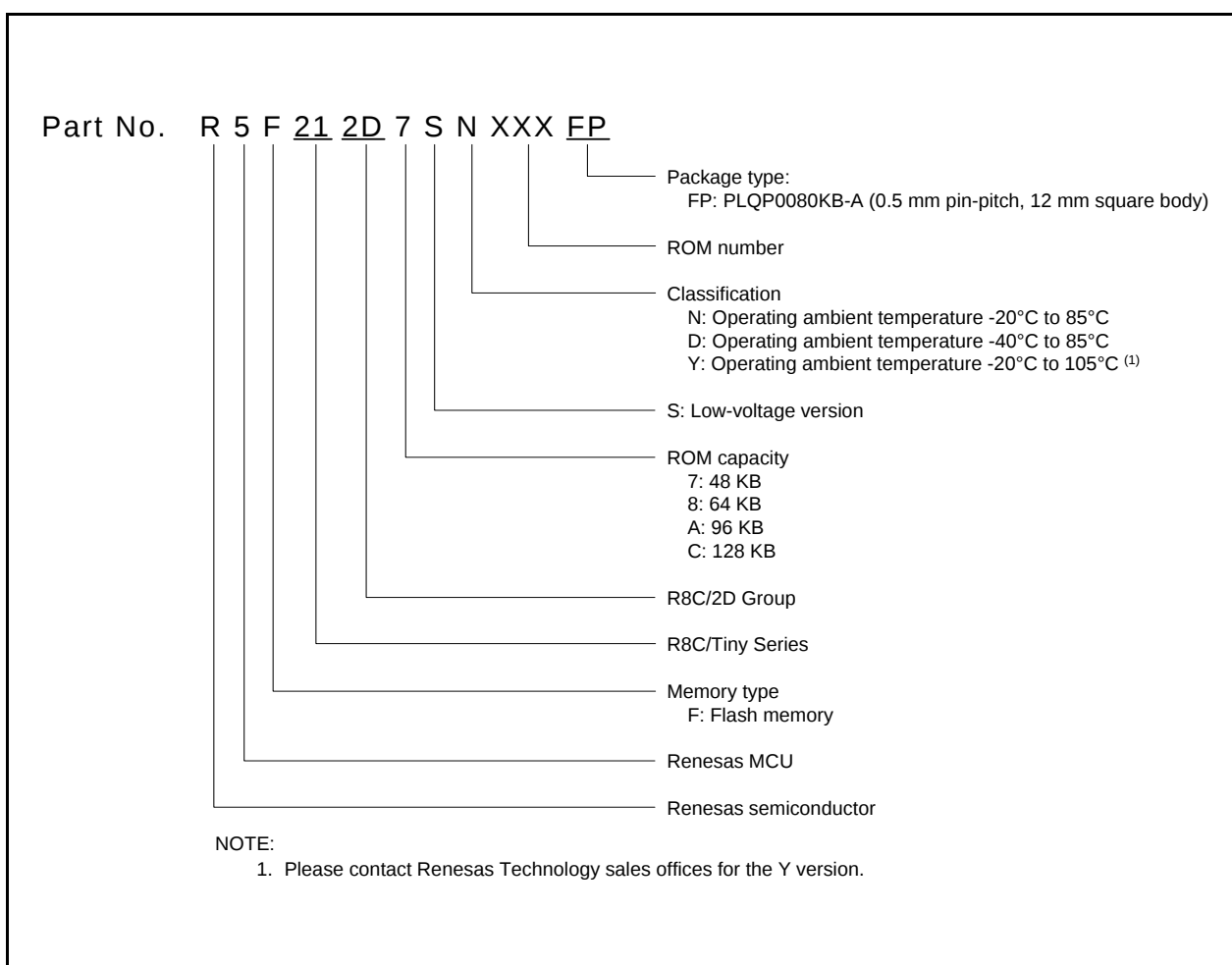
1. The user ROM is programmed before shipment.

Table 1.6 Product List for R8C/2D Group**Current of Dec. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks		
	Program ROM	Data flash					
R5F212D7SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	N version		
R5F212D8SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A			
R5F212DASNFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A			
R5F212DCSNFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A			
R5F212D7SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	D version		
R5F212D8SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A			
R5F212DASDFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A			
R5F212DCSDFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A			
R5F212D7SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	N version	Factory programming product ⁽¹⁾	
R5F212D8SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A			
R5F212DASNXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A			
R5F212DCSNXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A			
R5F212D7SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	D version		
R5F212D8SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A			
R5F212DASDXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A			
R5F212DCSDXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A			

NOTE:

1. The user ROM is programmed before shipment.

**Figure 1.2 Part Number, Memory Size, and Package of R8C/2D Group**

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

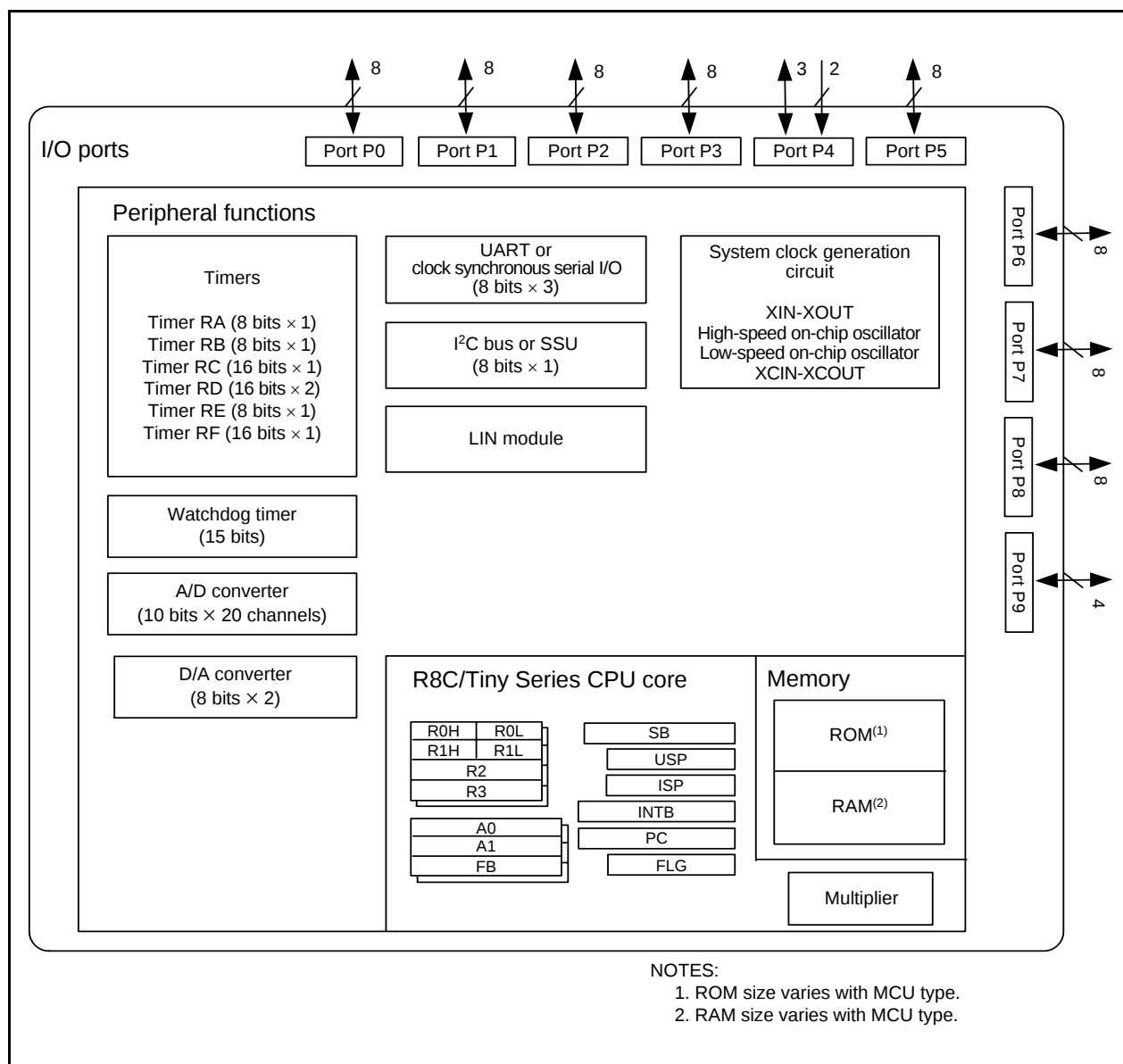


Figure 1.3 Block Diagram

Table 1.7 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter
1		P3_3				SSI		
2		P3_4				SCS	SDA	
3		P5_7						
4		P5_6						
5		P5_5						
6	MODE							
7	XCIN	P4_3						
8	XCOUT	P4_4						
9	RESET							
10	XOUT	P4_7						
11	VSS/AVSS							
12	XIN	P4_6						
13	VCC/AVCC							
14		P5_4		TRCIOD				
15		P5_3		TRCIOC				
16		P5_2		TRCIOB				
17		P5_1		TRCIOA/TRCTRG				
18		P5_0		TRCCLK				
19		P9_3						
20		P9_2						
21		P9_1						
22		P9_0						
23		P2_7		TRDIOD1				
24		P2_6		TRDIOC1				
25		P2_5		TRDIOB1				
26		P2_4		TRDIOA1				
27		P2_3		TRDIOD0				
28		P2_2		TRDIOC0				
29		P2_1		TRDIOB0				
30		P2_0		TRDIOA0/ TRDCLK				
31		P1_7	INT1	TRAIO				
32		P1_6			CLK0			
33		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0			
34		P1_4			TXD0			
35		P8_7						
36		P8_6						
37		P8_5		TRFO12				
38		P8_4		TRFO11				
39		P8_3		TRFO10/TRFI				
40		P8_2		TRFO02				
41		P8_1		TRFO01				
42		P8_0		TRFO00				
43		P6_0		TREO				
44		P4_5	INT0	INT0				
45		P6_6	INT2		TXD1			

NOTE:

1. Can be assigned to the pin in parentheses by a program.

Table 1.10 Pin Functions (2)

Item	Pin Name	I/O Type	Description
A/D converter	AN0 to AN19	I	Analog input pins to A/D converter
D/A converter	DA0 to DA1	O	D/A converter output pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports.
Input port	P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

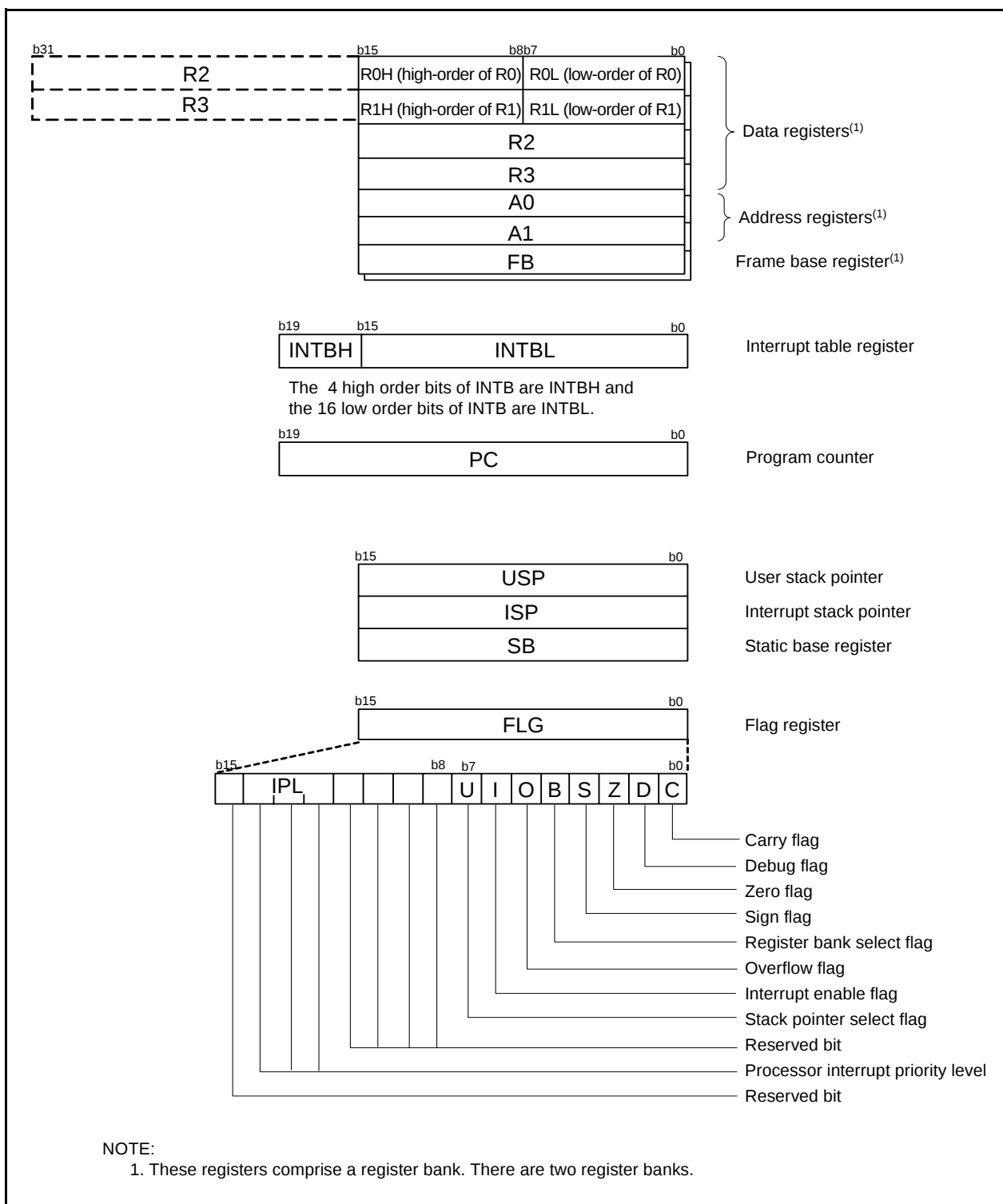


Figure 2.1 CPU Registers

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Operation Enable Register	MSTCR	00h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽⁶⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7	FRA7	When Shipping
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001000b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0039h			
003Ah			
003Eh			
003Fh			

X: Undefined

NOTES:

- The blank regions are reserved. Do not access locations in these regions.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
- The LVD0ON bit in the OFS register is set to 1 and hardware reset.
- Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
- The CSPROINI bit in the OFS register is set to 0.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
02C0h	A/D Register 0	AD0	XXh
02C1h			XXh
02C2h	A/D Register 1	AD1	XXh
02C3h			XXh
02C4h	A/D Register 2	AD2	XXh
02C5h			XXh
02C6h	A/D Register 3	AD3	XXh
02C7h			XXh
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h	A/D Control Register 2	ADCON2	00001000b
02D5h			
02D6h	A/D Control Register 0	ADCON0	00000011b
02D7h	A/D Control Register 1	ADCON1	00h
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h	Port P7 Direction Register	PD7	00h
02E1h			
02E2h	Port P7 Register	P7	XXh
02E3h			
02E4h	Port P8 Direction Register	PD8	00h
02E5h	Port P9 Direction Register	PD9	X0h
02E6h	Port P8 Register	P8	XXh
02E7h	Port P9 Register	P9	XXh
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh	Pull-Up Control Register 2	PUR2	XXX00000b
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	00h
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.6 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	50	400	μs
–	Byte program time (program/erase endurance > 1,000 times)		–	65	–	μs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		–20 ⁽⁸⁾	–	85	°C
–	Data hold time ⁽⁹⁾	Ambient temperature = 55 °C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. –40°C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

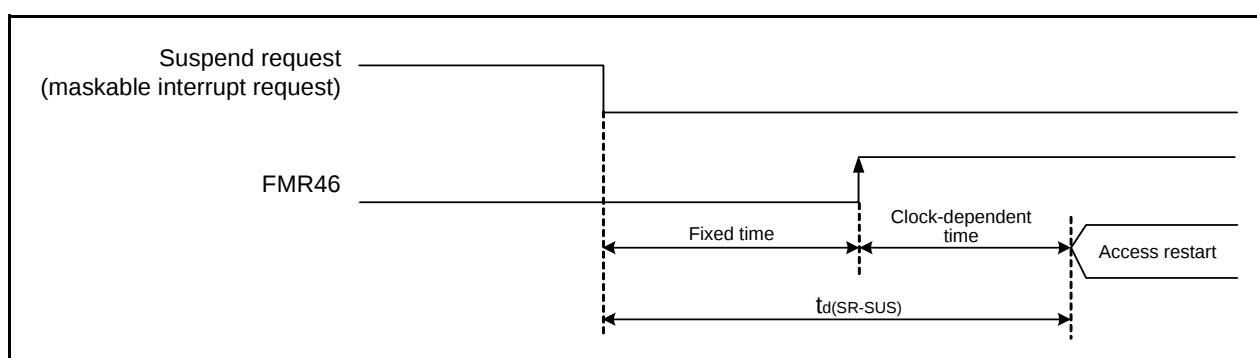


Figure 5.2 Time delay until Suspend

Table 5.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet0	Voltage detection level		2.2	2.3	2.4	V
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	0.9	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	300	μs
Vccmin	MCU operating voltage minimum value		2.2	—	—	V

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level		2.70	2.85	3.00	V
—	Voltage monitor 1 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level		3.3	3.6	3.9	V
—	Voltage monitor 2 interrupt request generation time ⁽²⁾		—	40	—	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	0.6	—	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

NOTES:

1. The measurement condition is Vcc = 2.2 V to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}^{(2)}$	39.2	40	40.8	MHz
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}^{(2)}$	39.0	40	41.0	MHz
		$V_{CC} = 2.2 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}^{(3)}$	35.2	40	44.8	MHz
		$V_{CC} = 2.2 \text{ V to } 5.5 \text{ V}$ $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}^{(3)}$	34.0	40	46.0	MHz
	High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	36.864	–	MHz
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$ $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	–3%	–	3%	%
–	Value in FRA1 register after reset		08h	–	F7h	–
–	Oscillation frequency adjustment unit of high-speed on-chip oscillator	Adjust FRA1 register (value after reset) to –1	–	+0.3	–	MHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	10	100	μs
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	550	–	μA

NOTES:

1. $V_{CC} = 2.2 \text{ to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.
2. These standard values show when the FRA1 register value after reset is assumed.
3. These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	10	100	μs
–	Self power consumption at oscillation	$V_{CC} = 5.0 \text{ V}$, $T_{opr} = 25^{\circ}\text{C}$	–	15	–	μA

NOTE:

1. $V_{CC} = 2.2 \text{ to } 5.5 \text{ V}$, $T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is $V_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ and $T_{opr} = 25^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.15 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12tcyc + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3tcyc + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5tcyc + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input fall time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1tcyc ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5tcyc ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hold time		3tcyc ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3tcyc ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3tcyc ⁽²⁾	–	–	ns
t _{SDAS}	Data input setup time		1tcyc + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

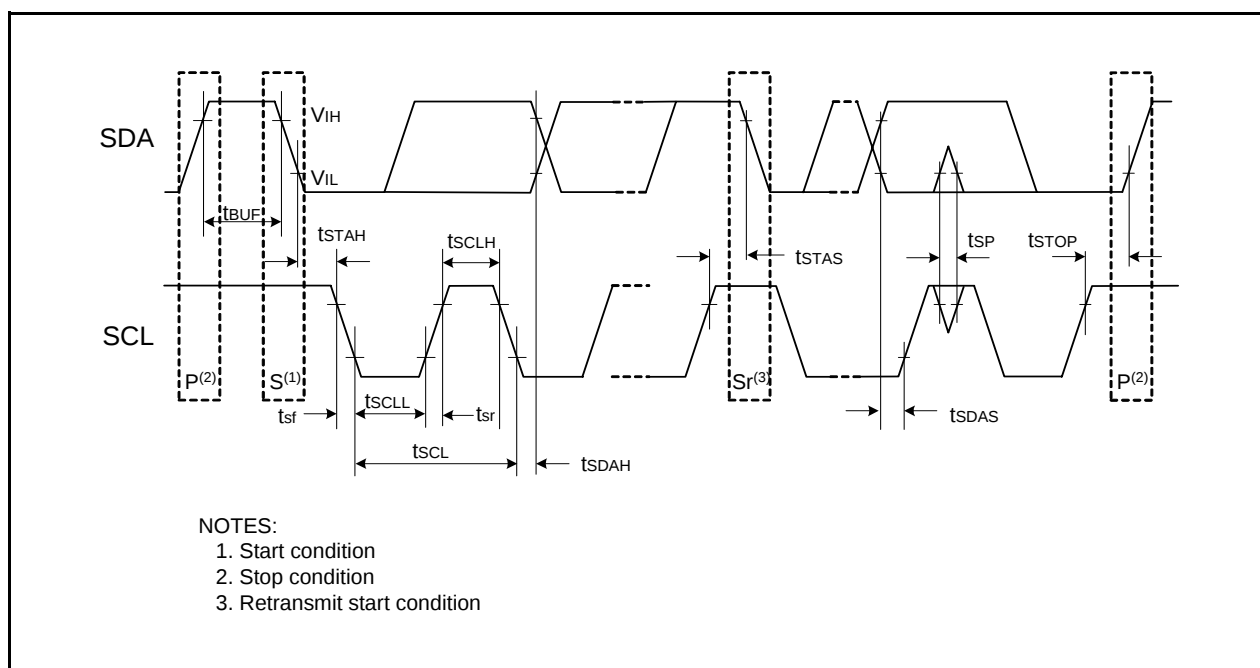
**Figure 5.7 I/O Timing of I²C bus Interface**

Table 5.16 Electrical Characteristics (1) [V_{CC} = 5 V]

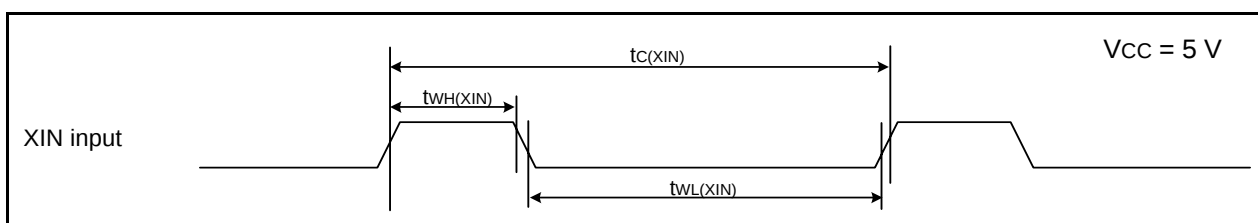
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = –5 mA		V _{CC} – 2.0	–	V _{CC}	V
			I _{OH} = –200 μA		V _{CC} – 0.5	–	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = –20 mA	V _{CC} – 2.0	–	V _{CC}	V
			Drive capacity LOW	I _{OH} = –5 mA	V _{CC} – 2.0	–	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = –1 mA	V _{CC} – 2.0	–	V _{CC}	V
			Drive capacity LOW	I _{OH} = –500 μA	V _{CC} – 2.0	–	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 5 mA		–	–	2.0	V
			I _{OL} = 200 μA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I _{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I _{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I _{OL} = 500 μA	–	–	2.0	V
V _{T+} –V _{T–}	Hysteresis	<u>INT0</u> , <u>INT1</u> , <u>INT2</u> , <u>INT3</u> , K10, K11, K12, K13, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		<u>RESET</u>			0.1	1.0	–	V
I _{IH}	Input "H" current		V _I = 5 V		–	–	5.0	μA
I _{IL}	Input "L" current		V _I = 0 V		–	–	–5.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		30	50	167	kΩ
R _{FXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R _{FXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:

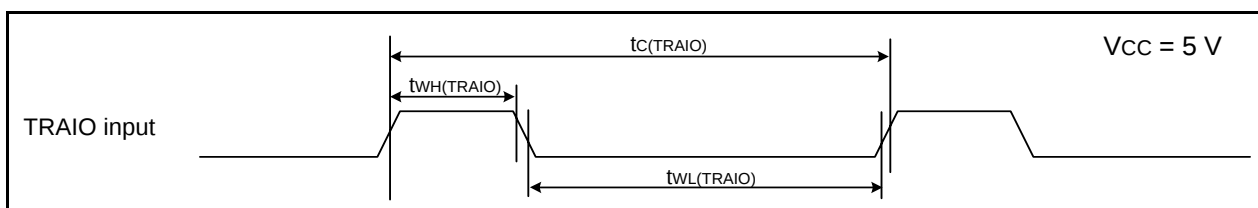
- V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^\circ\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.18 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

**Figure 5.9 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

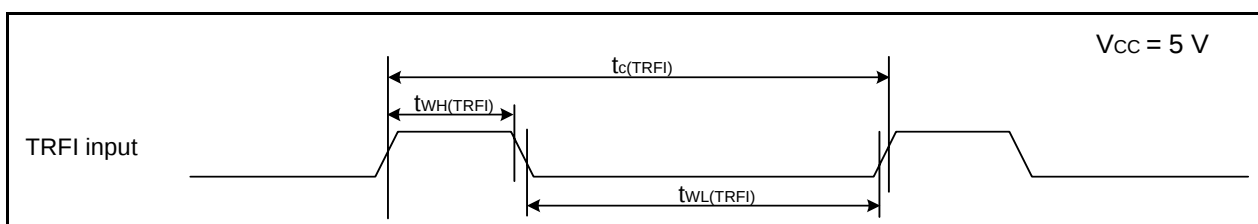
**Figure 5.10 TRFI Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

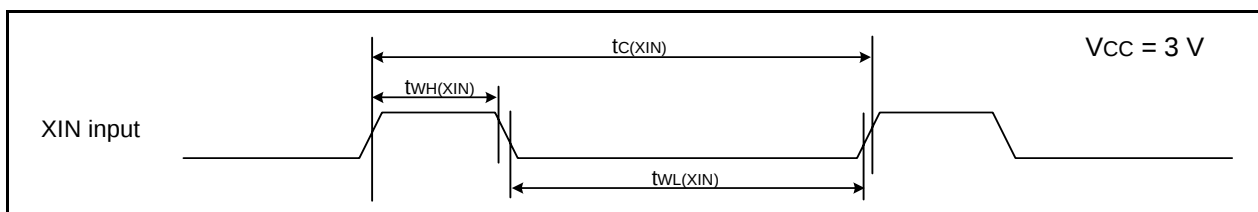
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except P2_0 to P2_7, XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P2_0 to P2_7, XOUT	I _{OL} = 1 mA		—	—	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	—	V
		RESET			0.1	0.4	—	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{IXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	18	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

NOTE:

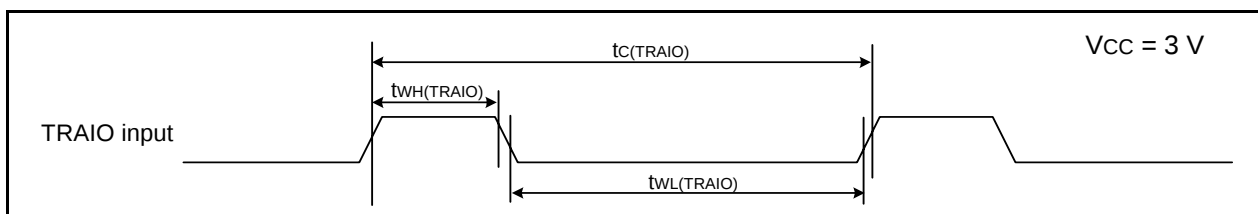
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^\circ\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.25 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.13 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.26 TRAIO Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

**Figure 5.14 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	1200 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	600 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	600 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

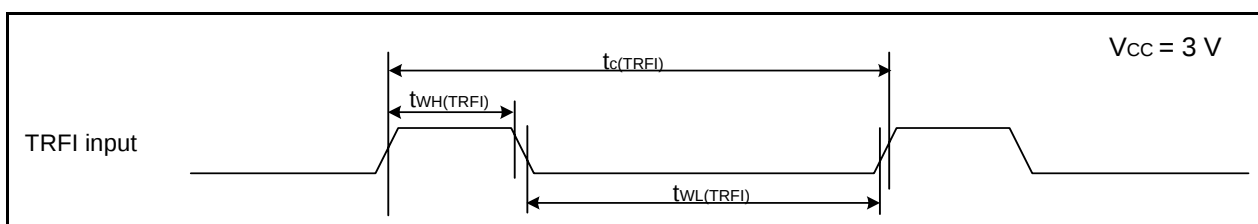
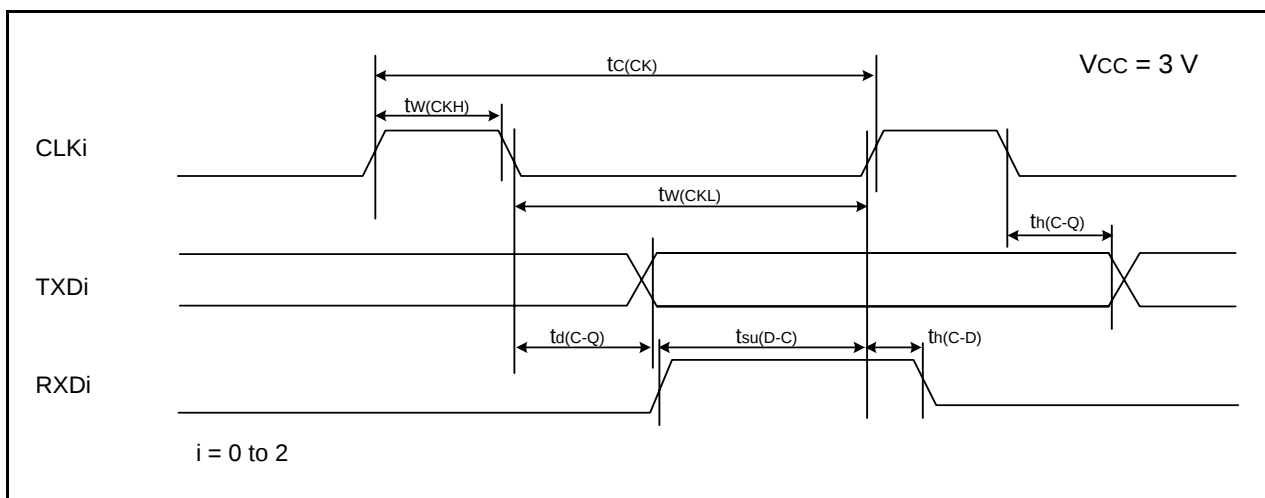
**Figure 5.15 TRFI Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.28 Serial Interface

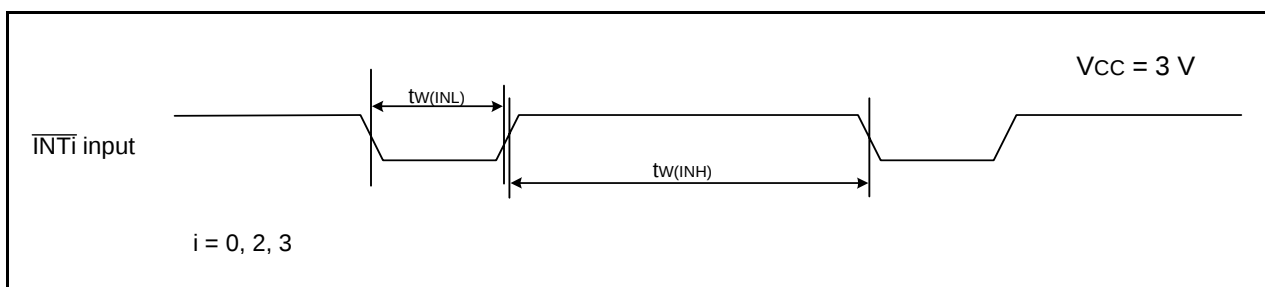
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi Input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

 $i = 0 \text{ to } 2$ **Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.29 External Interrupt $\overline{INTi}$ ($i = 0, 2, 3$) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency $\times$ 3) or the minimum value of standard, whichever is greater.

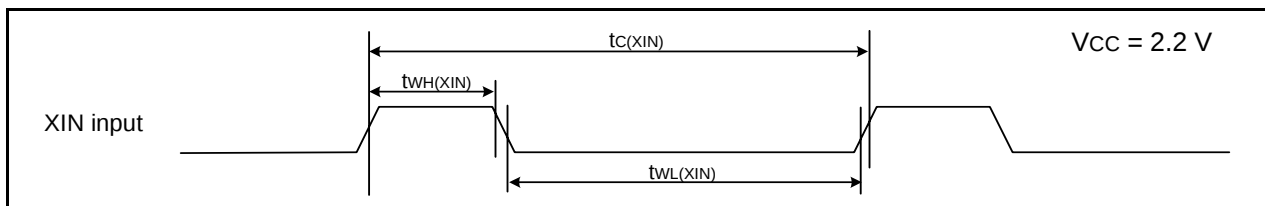
**Figure 5.17 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V**

**Table 5.31 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)**

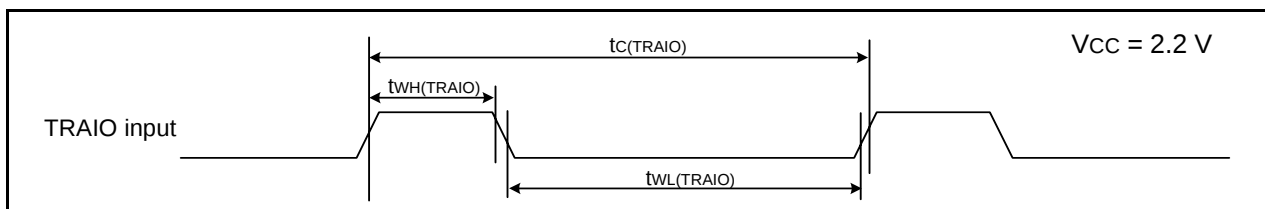
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS}	High-speed clock mode	–	2.5	–	mA
				1	–	mA
		High-speed on-chip oscillator mode	–	4	–	mA
			–	1.7	–	mA
		Low-speed on- chip oscillator mode	–	110	300	μA
		Low-speed clock mode	–	125	350	μA
			–	27	–	μA
		Wait mode	–	20	60	μA
			–	12	40	μA
			–	2.8	–	μA
			–	1.9	–	μA
		Stop mode	–	0.6	3.0	μA
			–	1.60	–	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.32 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.18 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input**

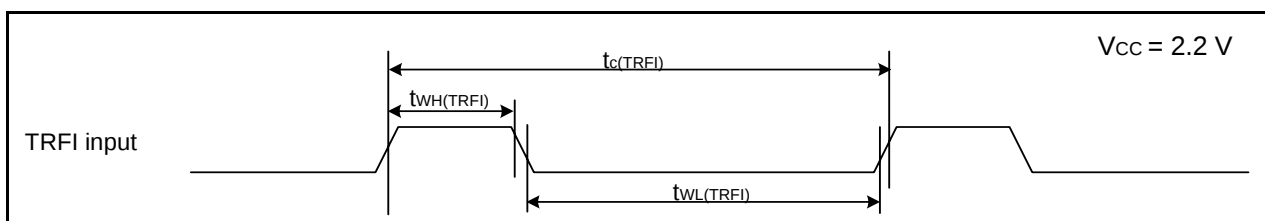
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

**Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.34 TRFI Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	2000 ⁽¹⁾	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	1000 ⁽²⁾	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	1000 ⁽²⁾	–	ns

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

**Figure 5.20 TRFI Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**