Renesas Electronics America Inc - R5F212D8SDFP#V2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f212d8sdfp-v2

1. Overview

1.1 Features

The R8C/2C Group and R8C/2D Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
Furthermore, the R8C/2D Group has on-chip data flash (1 KB × 2 blocks).
The difference between the R8C/2C Group and R8C/2D Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2C Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2D Group.

Table 1.1 Specifications for R8C/2C Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.5 Product List for R8C/2C Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3
I/O Ports	Programmable I/O ports	• Input-only: 2 pins • CMOS I/O ports: 71, selectable pull-up resistor • High current drive ports: 8
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode

Table 1.4 Specifications for R8C/2D Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1, UART2	Clock synchronous serial I/O/UART × 3
Clock Synchronous Serial I/O with Chip Select (SSU)		1 (shared with I2C-bus)
I2C bus(1)		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution × 2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V)
Current consumption		12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version)(2) -20 to 105°C (Y version)(3)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

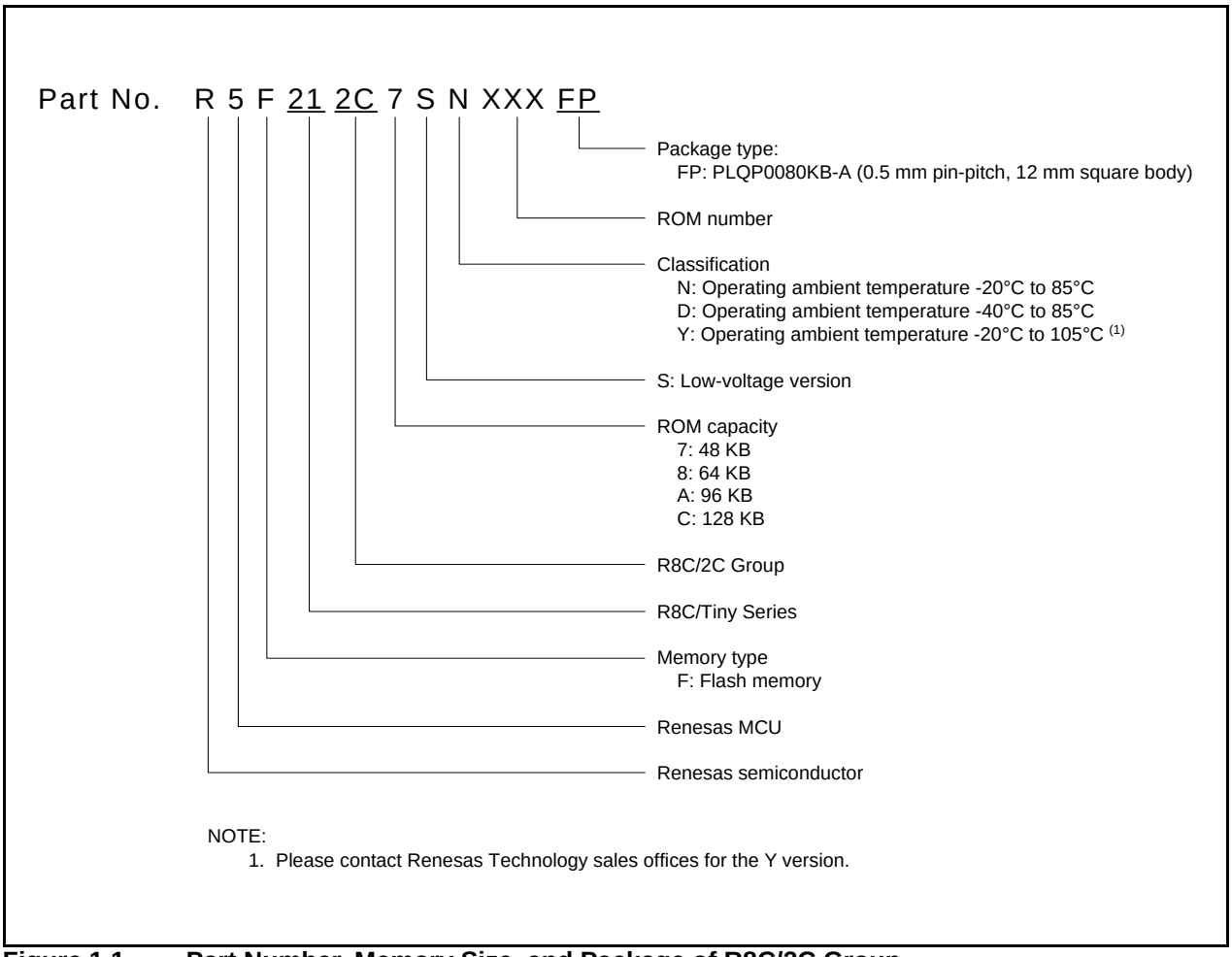


Figure 1.1 Part Number, Memory Size, and Package of R8C/2C Group

Table 1.6 Product List for R8C/2D Group **Current of Dec. 2007**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F212D7SNFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	N version	
R5F212D8SNFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A		
R5F212DASNFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A		
R5F212DCSNFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A		
R5F212D7SDFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	D version	
R5F212D8SDFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A		
R5F212DASDFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A		
R5F212DCSDFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A		
R5F212D7SNXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	N version	Factory programming product(1)
R5F212D8SNXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A		
R5F212DASNXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A		
R5F212DCSNXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A		
R5F212D7SDXXXFP	48 Kbytes	1 Kbyte × 2	2.5 Kbytes	PLQP0080KB-A	D version	
R5F212D8SDXXXFP	64 Kbytes	1 Kbyte × 2	3 Kbytes	PLQP0080KB-A		
R5F212DASDXXXFP	96 Kbytes	1 Kbyte × 2	7 Kbytes	PLQP0080KB-A		
R5F212DCSDXXXFP	128 Kbytes	1 Kbyte × 2	7.5 Kbytes	PLQP0080KB-A		

NOTE:
1. The user ROM is programmed before shipment.

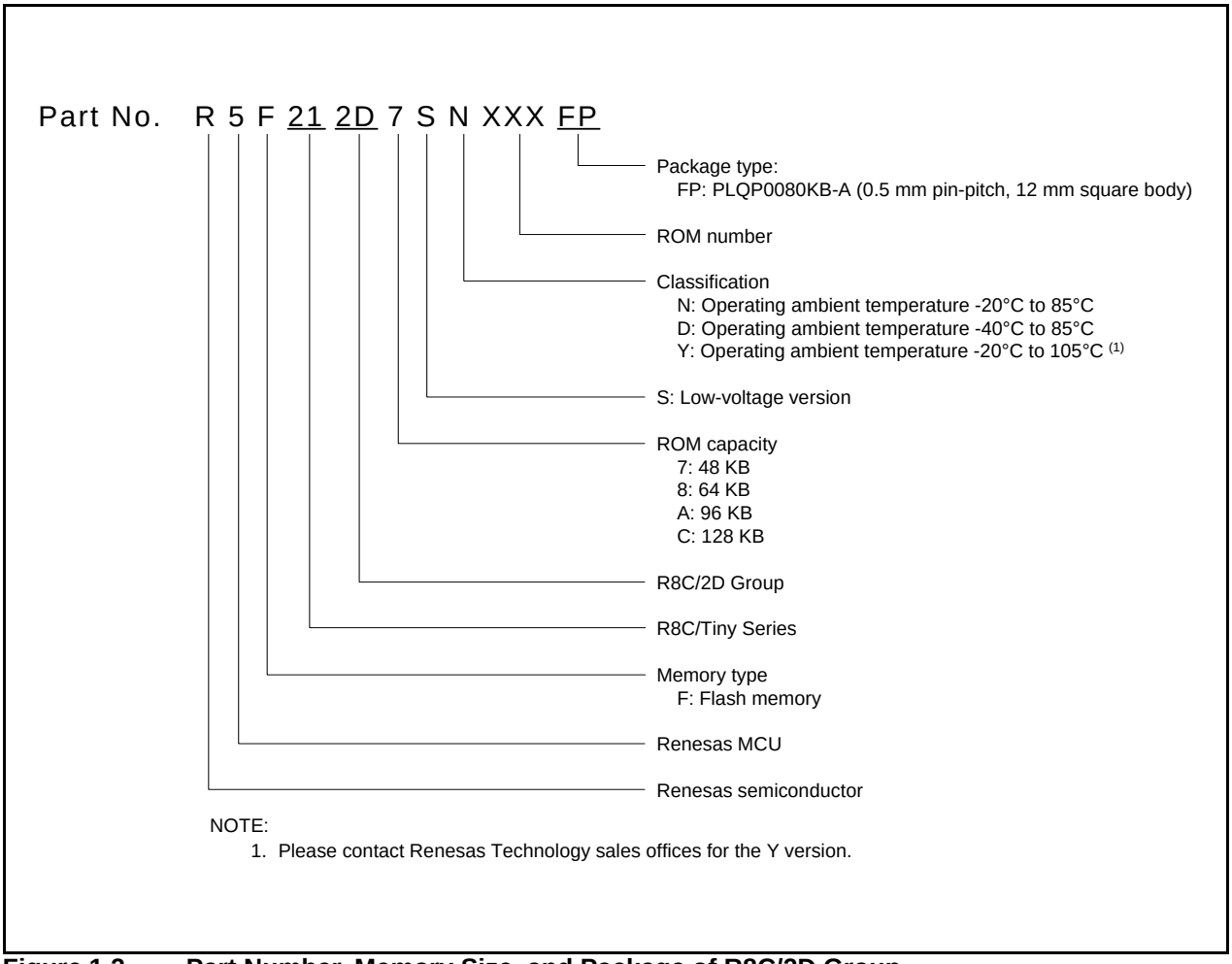


Figure 1.2 Part Number, Memory Size, and Package of R8C/2D Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

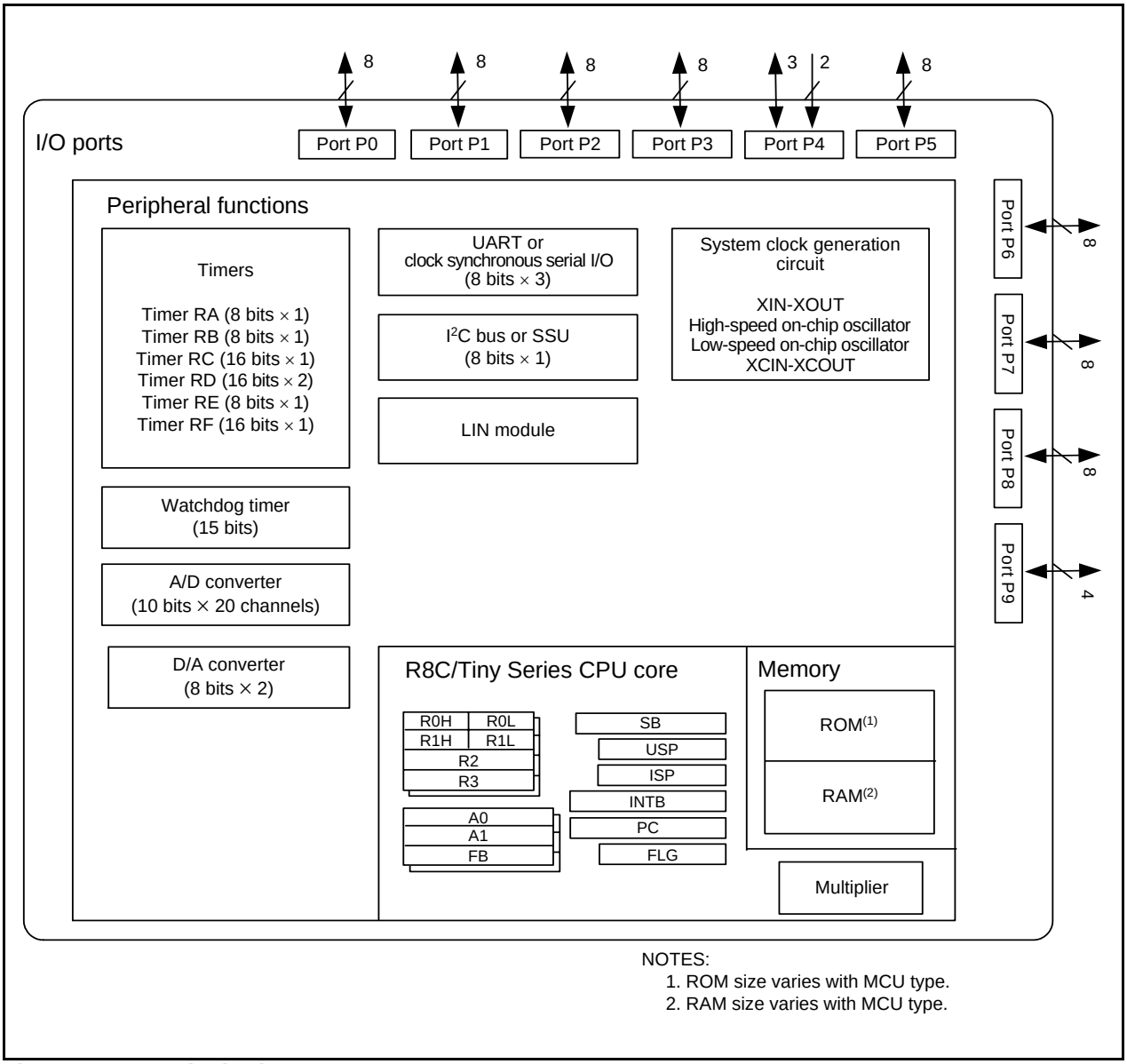
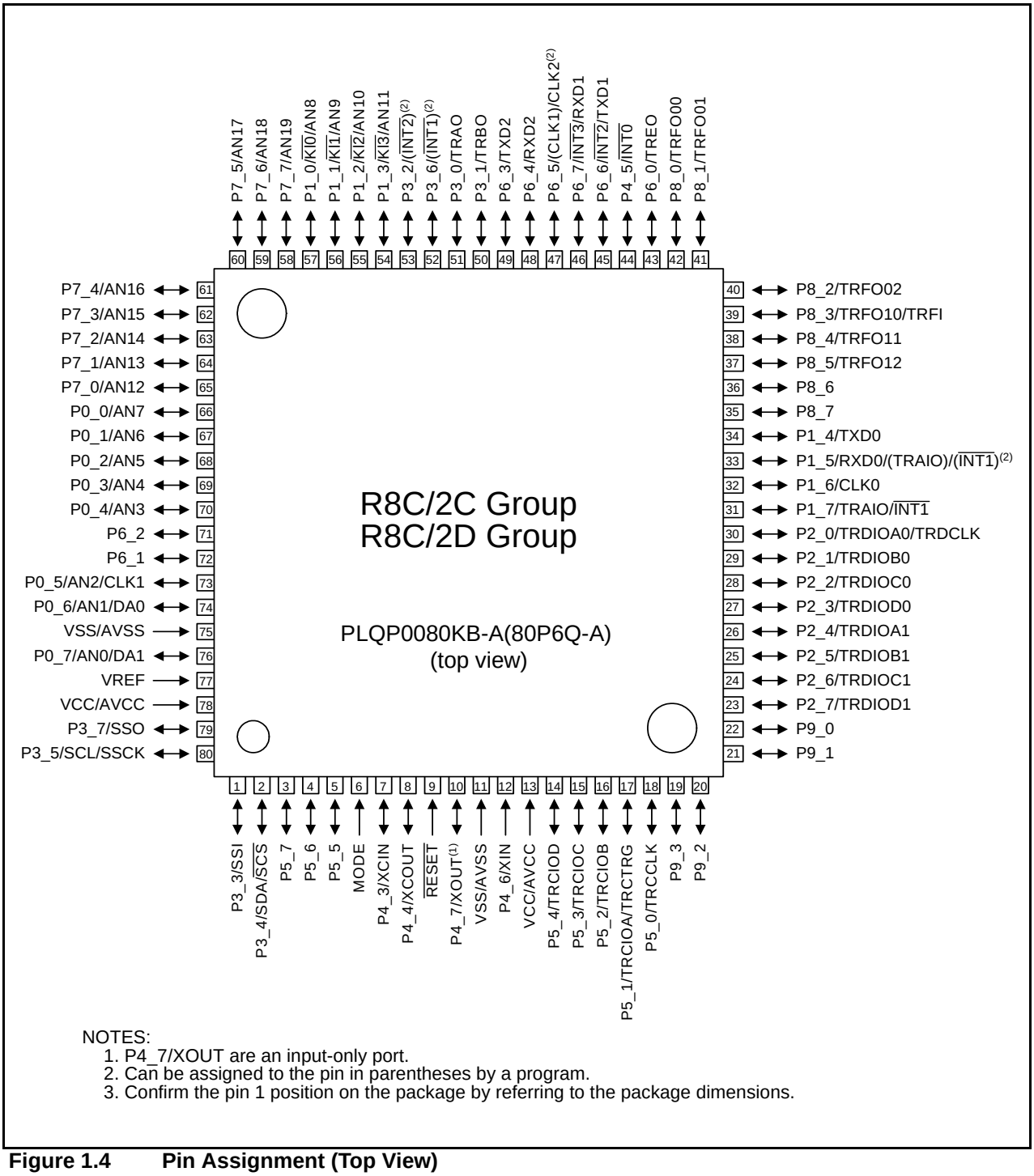


Figure 1.3 Block Diagram

1.4 Pin Assignment

Figure 1.4 shows Pin Assignment (Top View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.



NOTES:
1. P4_7/XOUT are an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignment (Top View)

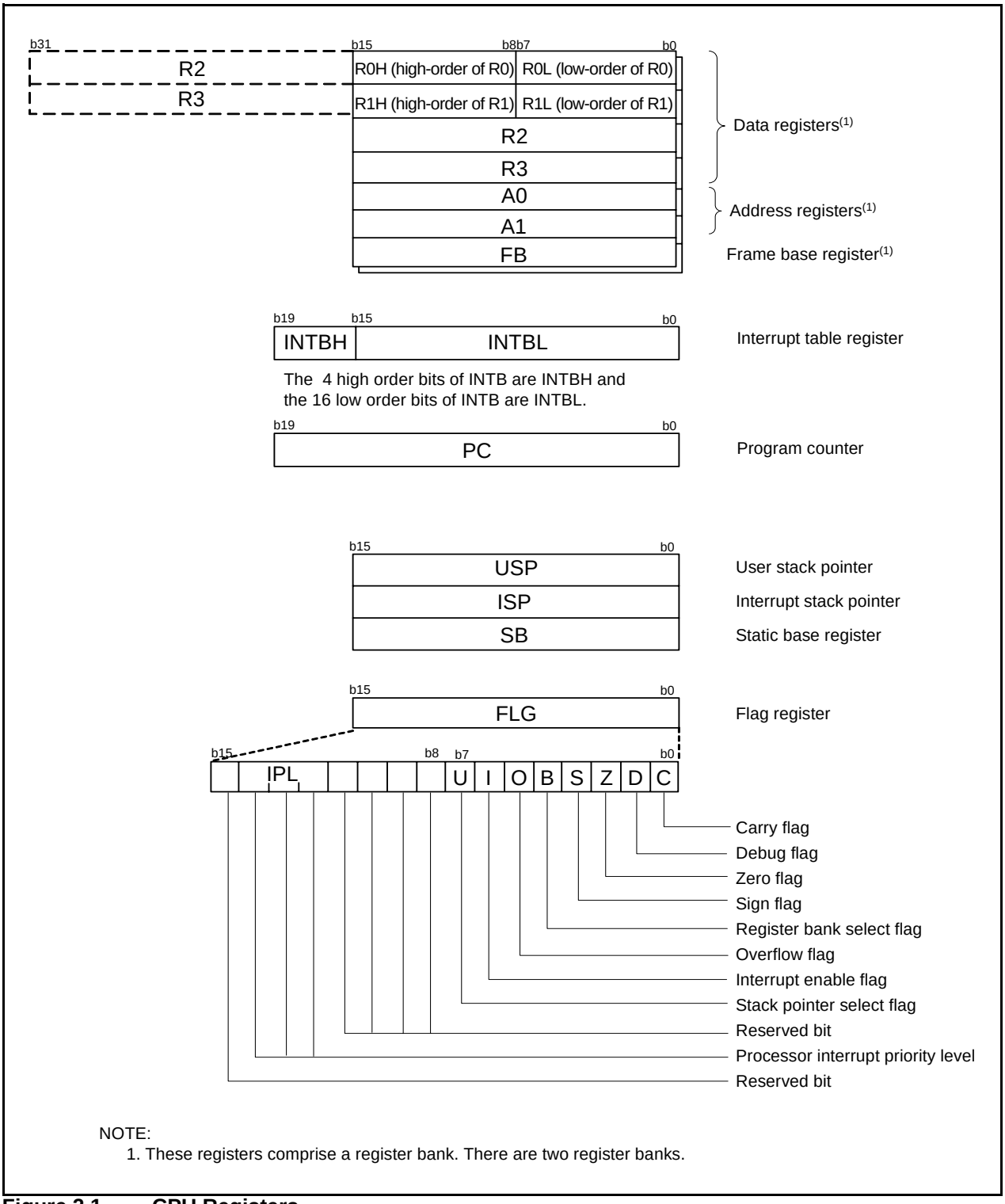
Table 1.7 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter
1		P3_3				SSI		
2		P3_4				$\overline{SCS}$	SDA	
3		P5_7						
4		P5_6						
5		P5_5						
6	MODE							
7	XCIN	P4_3						
8	XCOUT	P4_4						
9	$\overline{RESET}$							
10	XOUT	P4_7						
11	VSS/AVSS							
12	XIN	P4_6						
13	VCC/AVCC							
14		P5_4		TRCIOD				
15		P5_3		TRCIOC				
16		P5_2		TRCIOB				
17		P5_1		TRCIOA/TRCTRG				
18		P5_0		TRCCLK				
19		P9_3						
20		P9_2						
21		P9_1						
22		P9_0						
23		P2_7		TRDIOD1				
24		P2_6		TRDIOC1				
25		P2_5		TRDIOB1				
26		P2_4		TRDIOA1				
27		P2_3		TRDIOD0				
28		P2_2		TRDIOC0				
29		P2_1		TRDIOB0				
30		P2_0		TRDIOA0/ TRDCLK				
31		P1_7	$\overline{INT1}$	TRAIO				
32		P1_6			CLK0			
33		P1_5	($\overline{INT1}$)(1)	(TRAIO)(1)	RXD0			
34		P1_4			TXD0			
35		P8_7						
36		P8_6						
37		P8_5		TRFO12				
38		P8_4		TRFO11				
39		P8_3		TRFO10/TRFI				
40		P8_2		TRFO02				
41		P8_1		TRFO01				
42		P8_0		TRFO00				
43		P6_0		TREO				
44		P4_5	$\overline{INT0}$	$\overline{INT0}$				
45		P6_6	$\overline{INT2}$		TXD1			

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU/IIC Interrupt Control Register[2]	SSUIC / IICIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
02C0h	A/D Register 0	AD0	XXh
02C1h			XXh
02C2h	A/D Register 1	AD1	XXh
02C3h			XXh
02C4h	A/D Register 2	AD2	XXh
02C5h			XXh
02C6h	A/D Register 3	AD3	XXh
02C7h			XXh
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h	A/D Control Register 2	ADCON2	00001000b
02D5h			
02D6h	A/D Control Register 0	ADCON0	00000011b
02D7h	A/D Control Register 1	ADCON1	00h
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h	Port P7 Direction Register	PD7	00h
02E1h			
02E2h	Port P7 Register	P7	XXh
02E3h			
02E4h	Port P8 Direction Register	PD8	00h
02E5h	Port P9 Direction Register	PD9	X0h
02E6h	Port P8 Register	P8	XXh
02E7h	Port P9 Register	P9	XXh
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh	Pull-Up Control Register 2	PUR2	XXX00000b
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	00h

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

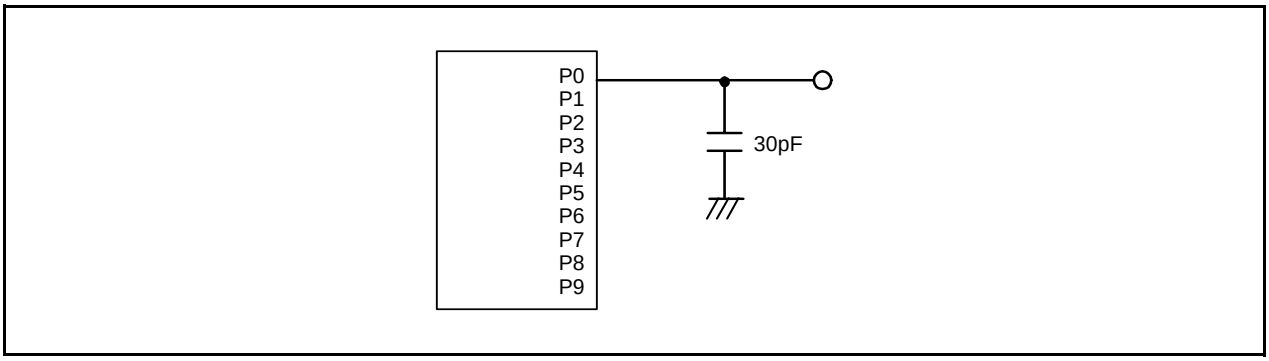


Figure 5.1 Ports P0 to P9 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}	–	–	10	Bit
–	Absolute accuracy	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±3	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 3.3 V	–	–	±2	LSB
		10-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±5	LSB
		8-bit mode	ϕ_{AD} = 5 MHz, V_{ref} = AV_{CC} = 2.2 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AV_{CC}	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	3.3	–	–	µs
		8-bit mode	ϕ_{AD} = 10 MHz, V_{ref} = AV_{CC} = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage(2)			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	0.25	–	10	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.7 to 5.5 V	1	–	10	MHz
		Without sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	0.25	–	5	MHz
		With sample and hold	V_{ref} = AV_{CC} = 2.2 to 5.5 V	1	–	5	MHz

NOTES:
1. V_{CC}/AV_{CC} = Vref = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution		–	–	8	Bit
–	Absolute accuracy		–	–	1.0	%
t_{su}	Setup time		–	–	3	µs
R_O	Output resistor		4	10	20	kΩ
I_{Vref}	Reference power input current	(NOTE 2)	–	–	1.5	mA

NOTES:
1. V_{CC}/AV_{CC} = Vref = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (V_{REF} not connected), I_{Vref} flows into the D/A converters.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/2C Group	100(3)	–	–	times
		R8C/2D Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

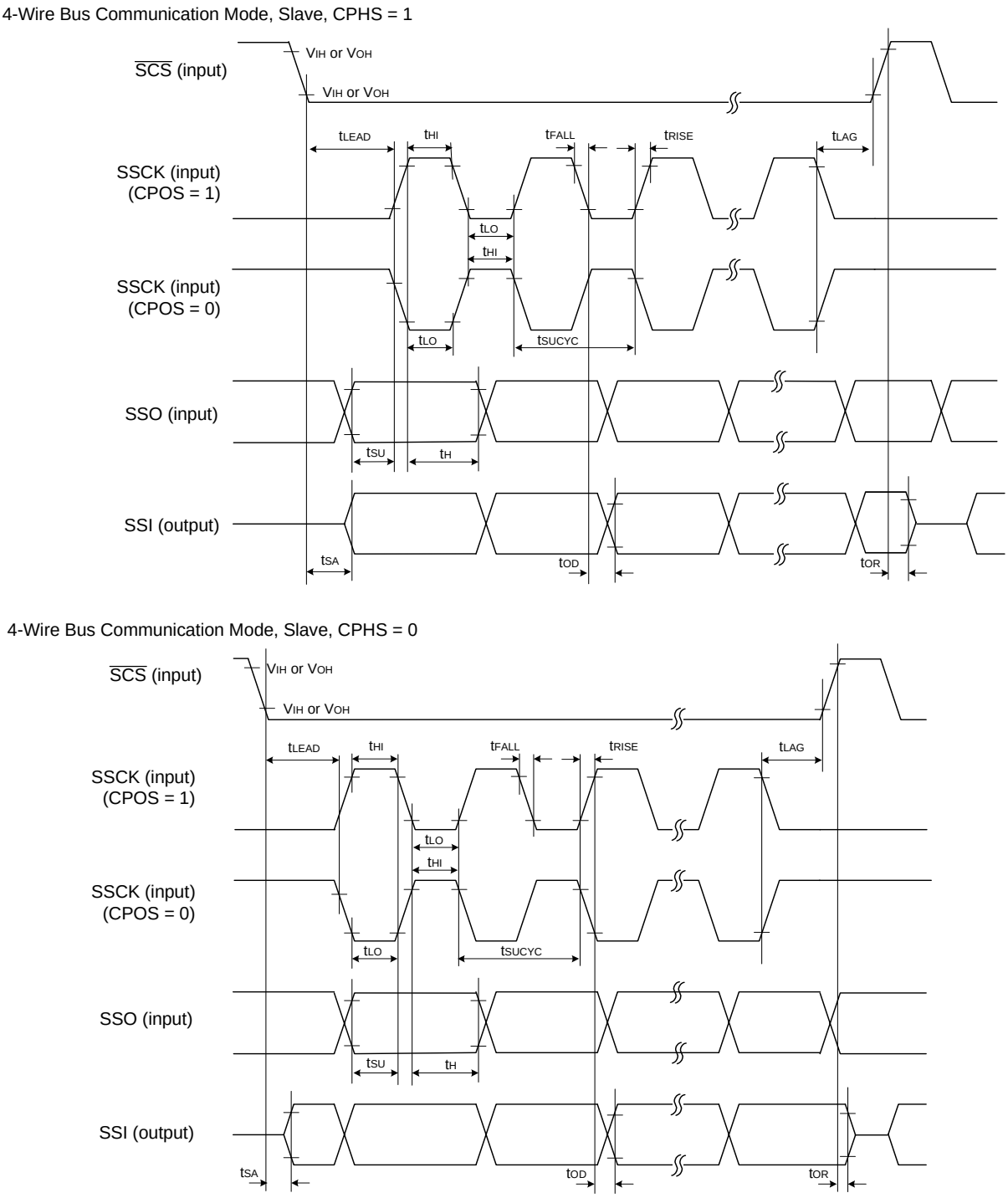


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.16 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = –5 mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA		V_{CC} – 0.5	–	V_{CC}	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = –1 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = –500 μA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V		–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	XIN			–	1.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.23 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except P2_0 to P2_7, XOUT	I_{OH} = –1 mA		Vcc – 0.5	–	Vcc	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OH} = –5 mA	Vcc – 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = –1 mA	Vcc – 0.5	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = –0.1 mA	Vcc – 0.5	–	Vcc	V
			Drive capacity LOW	I_{OH} = –50 µA	Vcc – 0.5	–	Vcc	V
V_{OL}	Output “L” voltage	Except P2_0 to P2_7, XOUT	I_{OL} = 1 mA		–	–	0.5	V
		P2_0 to P2_7	Drive capacity HIGH	I_{OL} = 5 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

NOTE:
1. Vcc =2.7 to 3.3 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5.5	11	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	145	400	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	–	145	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	28	85	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	17	50	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.3	–	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	2.1	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	0.65	3.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	1.65	–	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.32 XIN Input, XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input “H” width	90	–	ns
$t_{WL(XIN)}$	XIN input “L” width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

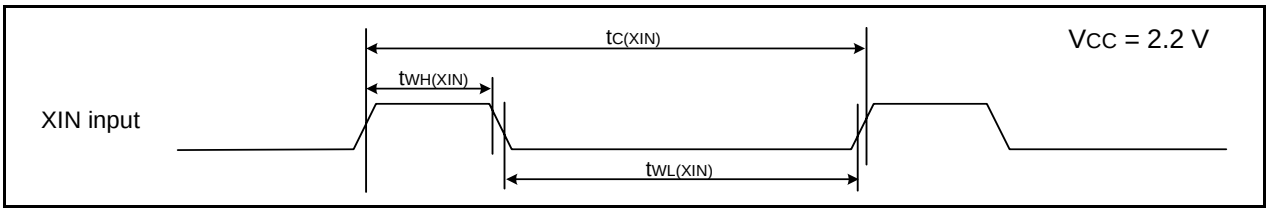


Figure 5.18 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

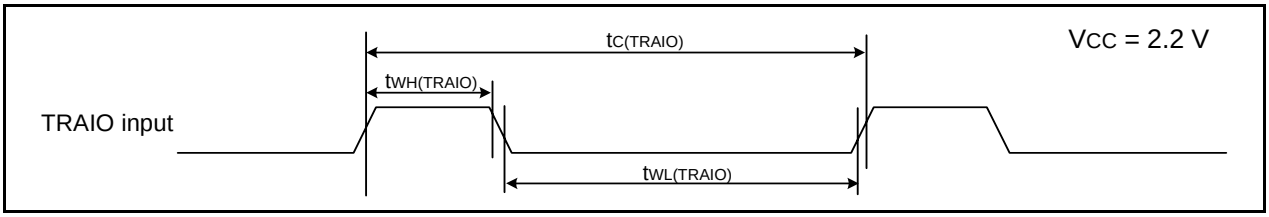


Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 2.2 V

Table 5.34 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	2000(1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	1000(2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	1000(2)	–	ns

NOTES:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

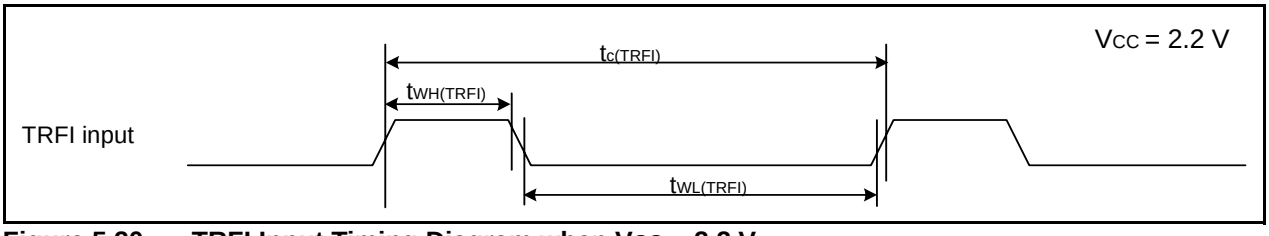
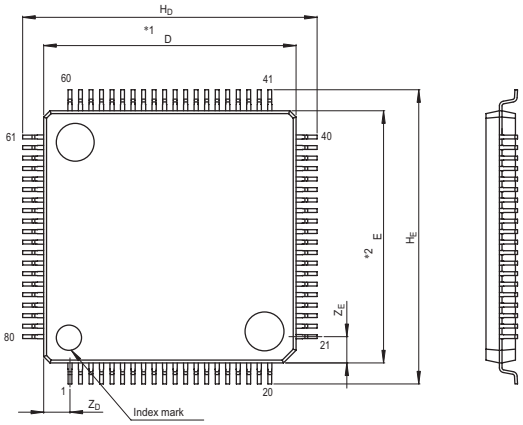


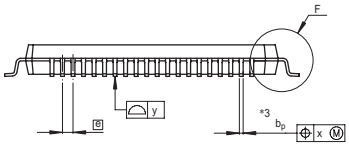
Figure 5.20 TRFI Input Timing Diagram when Vcc = 2.2 V

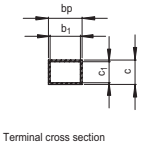
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

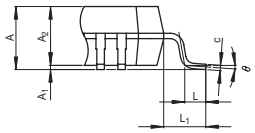
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	R8C/2C Group, R8C/2D Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Apr 03, 2006	–	First Edition issued
0.10	Jun 26, 2006	All pages	Pin name revised CMP0_0 → TRFO00, CMP0_1 → TRFO01, CMP0_2 → TRFO02, CMP1_0 → TRFO10, CMP1_1 → TRFO11, CMP1_2 → TRFO12, TRFIN → TRFI
		2, 4	Table 1.1 Specifications for R8C/2C Group (1) and Table 1.3 Specifications for R8C/2D Group (1); I/O Ports: • Input-only: 3 pins → 2 pins revised Interrupts: • Internal: 17 sources → 23 sources revised
		3, 5	Table 1.2 Specifications for R8C/2C Group (2) and Table 1.4 Specifications for R8C/2D Group (2); ROM Correction Function deleted
		8	Figure 1.3 Block Diagram revised
		9	Figure 1.4 Pin Assignment (Top View) revised
		10, 11	Table 1.7 Pin Name Information by Pin Number (1) and Table 1.8 Pin Name Information by Pin Number (2) revised
		12, 13	Table 1.9 Pin Functions (1) and Table 1.10 Pin Functions (2) revised
		19	Table 4.1 SFR Information (1); • 0008h: Module Standby Control Register, MSTCR, 00h added • 001Ch: “00h” → “00h, 10000000b” revised • NOTE6 added
		20	Table 4.2 SFR Information (2); • 005Fh: Capture Interrupt Control Register, CAPIC, XXXXX000b added
		22	Table 4.4 SFR Information (4); • 00DCh: “00DDh” → “00DCh” revised • 00F5h: “XXXX00XXb” → “00h” revised
		23	Table 4.5 SFR Information (5); • 0105h: LIN Special Function Register, LINCR2, 00h added
		31	Package Dimensions; “Diagrams showing the latest package dimensions ... in the “Packages” section of the Renesas Technology website.” added
0.20	Sep 15, 2006	31 to 54	5. Electrical Characteristics added
0.30	Dec 22, 2006	6	Table 1.5 and Figure 1.1 revised
		7	Table 1.6 and Figure 1.2 revised
		17	Figure 3.1 revised
		18	Figure 3.2 revised
		19	Table 4.1; • 000Ah: “00XXX000b” → “00h” revised • 0008h: “Module Standby Control Register” → “Module Operation Enable Register” revised • 000Fh: “00011111b” → “00X11111b” revised
		37	Table 5.11 revised