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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	201-VFBGA, CSBGA
Supplier Device Package	201-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v2-cs201

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

SRAM and FIFO

IGLOO PLUS devices (except AGLP030 devices) have embedded SRAM blocks along their north side. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in AGLP030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOO PLUS devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO PLUS family contains six CCCs. One CCC (center west side) has a PLL. The AGLP030 device does not have a PLL or CCCs; it contains only inputs to six globals.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

The four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases (for PLL only) is 40 ps × 250 MHz / f_{OUT_CCC}

Global Clocking

IGLOO PLUS devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO PLUS family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO PLUS FPGAs support many different I/O standards.

The I/Os are organized into four banks. All devices in IGLOO PLUS have four banks. The configuration of these banks determines the I/O standards supported.

Power Consumption of Various Internal Resources

***Table 2-15* • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)		
		AGLP125	AGLP060	AGLP030
PAC1	Clock contribution of a Global Rib	4.489	2.696	0.000[1]
PAC2	Clock contribution of a Global Spine	1.991	1.962	3.499
PAC3	Clock contribution of a VersaTile row	1.510	1.523	1.537
PAC4	Clock contribution of a VersaTile used as a sequential module	0.153	0.151	0.151
PAC5	First contribution of a VersaTile used as a sequential module	0.029	0.029	0.029
PAC6	Second contribution of a VersaTile used as a sequential module	0.323	0.323	0.323
PAC7	Contribution of a VersaTile used as a combinatorial module	0.280	0.300	0.278
PAC8	Average contribution of a routing net	1.097	1.081	1.130
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-9.		
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14 on page 2-9.		
PAC11	Average contribution of a RAM block during a read operation	25.00		
PAC12	Average contribution of a RAM block during a write operation	30.00		
PAC13	Dynamic contribution for PLL	2.70		

Note: 1. There is no Center Global Rib present in AGLP030, and thus it starts directly at the spine resulting in 0µW/MHz.

***Table 2-16* • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices For IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)		
		AGLP125	AGLP060	AGLP030
PDC1	Array static power in Active mode	See Table 2-12 on page 2-8		
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-7		
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7		
PDC4	Static PLL contribution	1.84[1]		
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-12 on page 2-8		

Notes:

1. *This is the minimum contribution of the PLL when operating at lowest frequency.*
2. *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or the SmartPower tool in Libero SoC software.*

Table 2-24 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Detailed I/O DC Characteristics

***Table 2-27* • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

***Table 2-28* • I/O Output Buffer Maximum Resistances [1]**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω) [2]	$R_{PULL\text{-}UP}$ (Ω) [3]
3.3 V LVTTL / 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	157.5	163.8
1.2 V LVCMOS Wide Range[4]	100 µA	157.5	163.8

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC_I, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS model on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *Applicable to IGLOO PLUS V2 devices operating at VCCI ≥ VCC.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

Table 2-70 • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-71 • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Fully Registered I/O Buffers with Asynchronous Clear

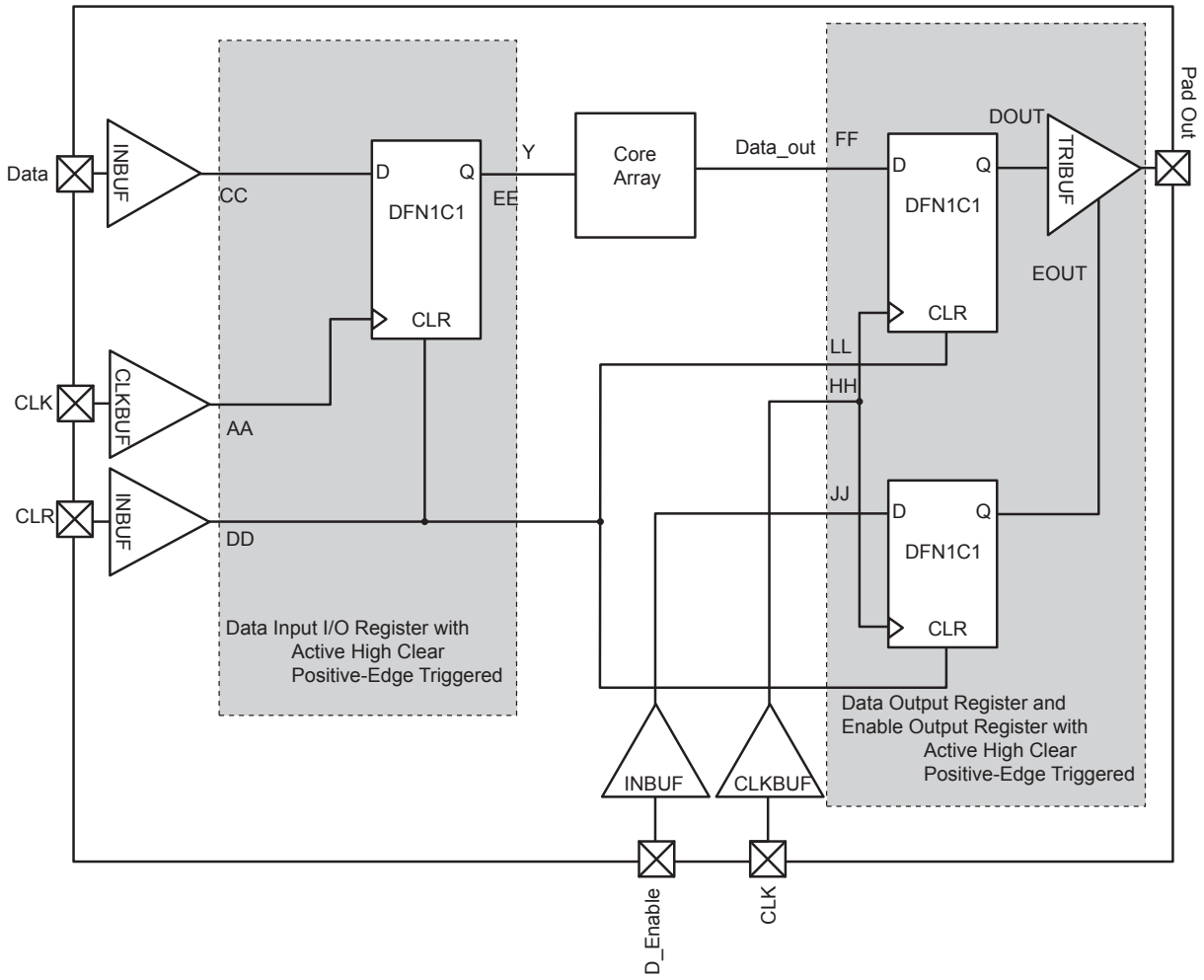


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

Input Register

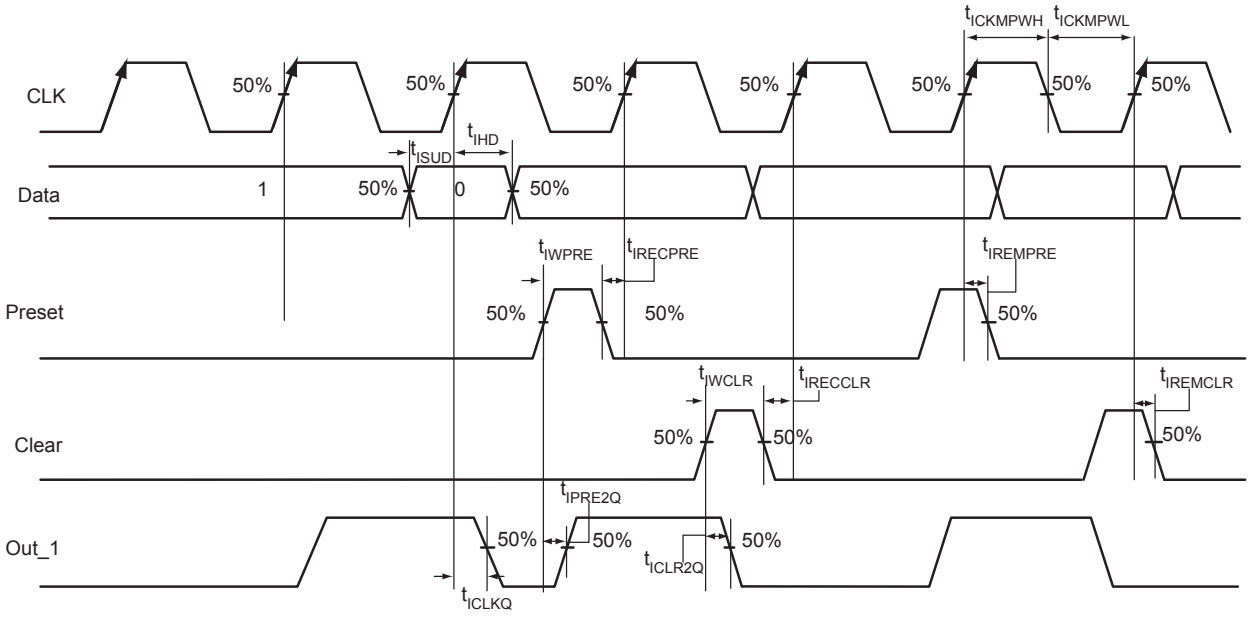


Figure 2-14 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-74 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.41	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.57	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.57	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output Register

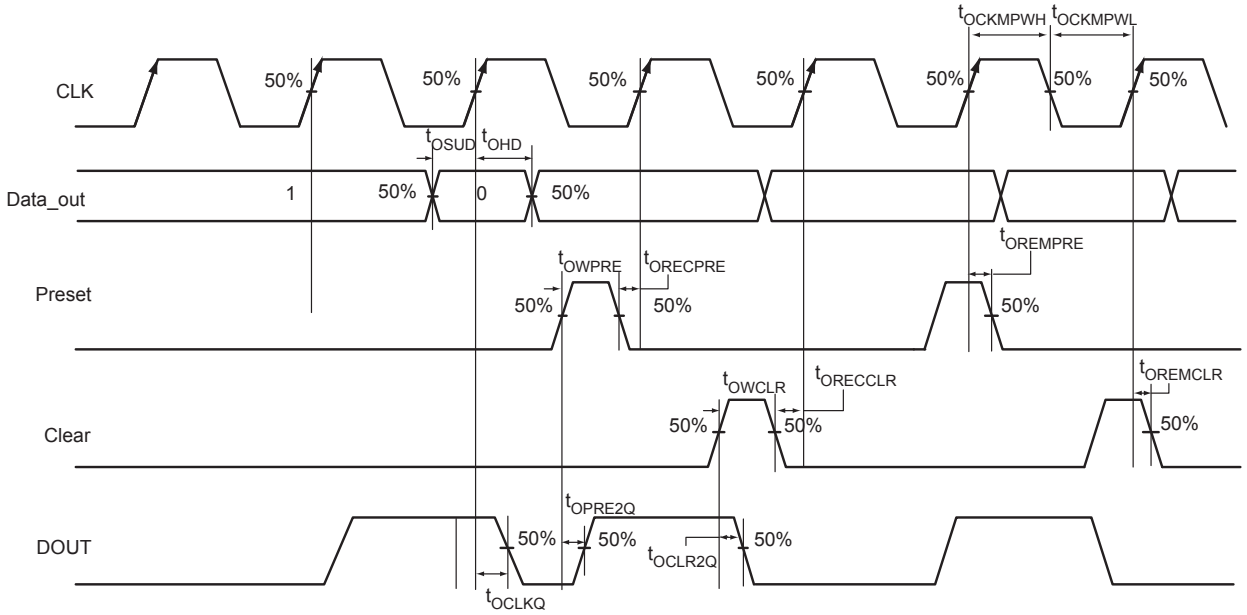


Figure 2-15 • **Output Register Timing Diagram**

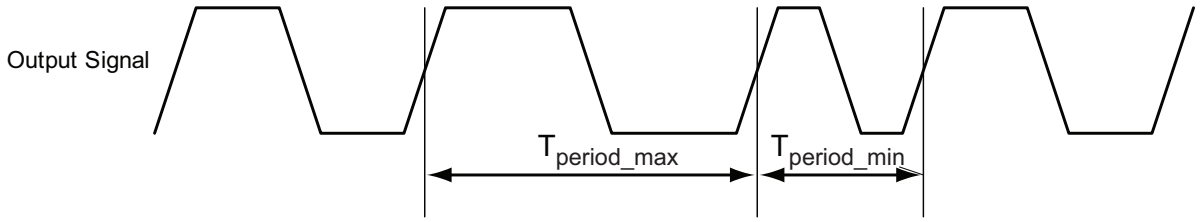
Timing Characteristics

1.5 V DC Core Voltage

Table 2-76 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.66	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.82	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.88	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-22 • **Peak-to-Peak Jitter Definition**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-92 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.68	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{BKS}	BLK setup time	1.37	ns
t_{BKH}	BLK hold time	0.13	ns
t_{DS}	Input data (DIN) setup time	0.59	ns
t_{DH}	Input data (DIN) hold time	0.30	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.94	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.51	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.29	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.24	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.40	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.72	ns
	RESET Low to data out Low on DOUT (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-95 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.29	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.36	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow through)	3.21	ns
	RESET Low to data out Low on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

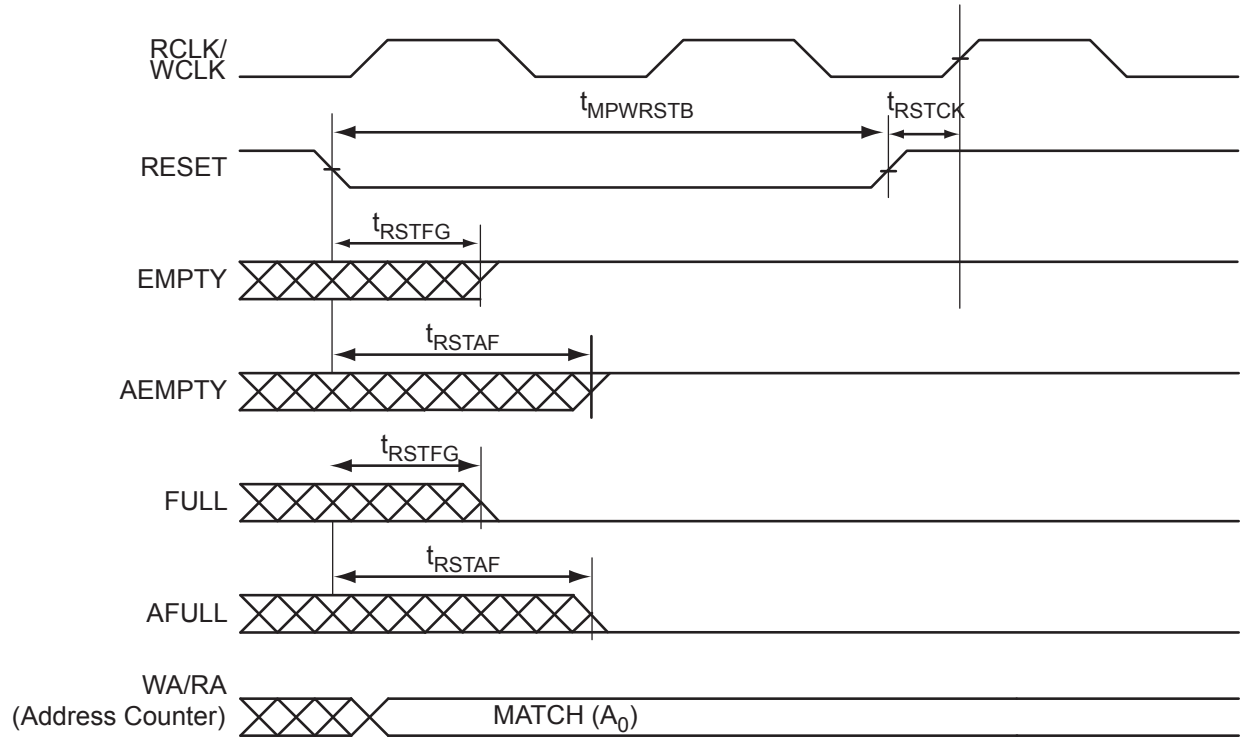


Figure 2-32 • **FIFO Reset**

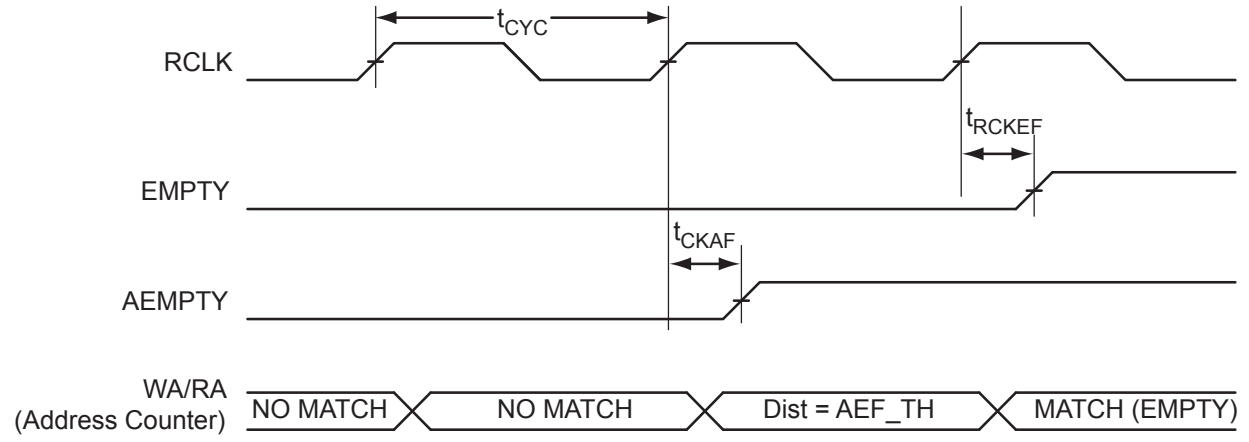


Figure 2-33 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

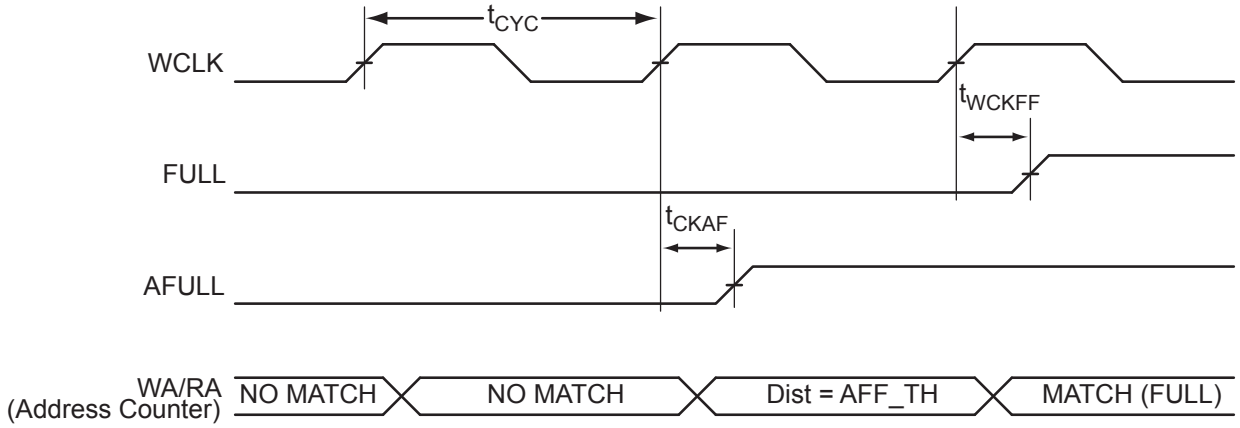


Figure 2-34 • **FIFO FULL Flag and AFULL Flag Assertion**

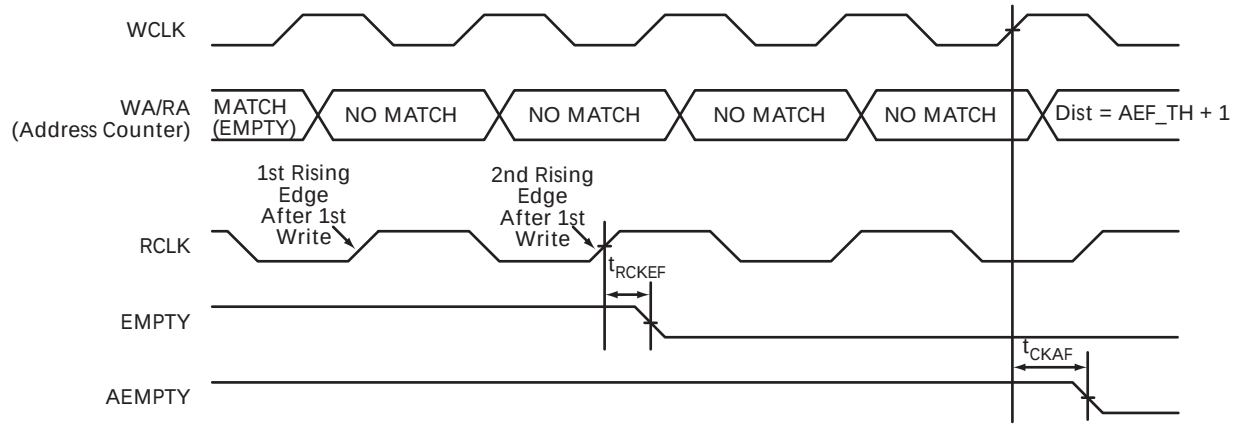


Figure 2-35 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

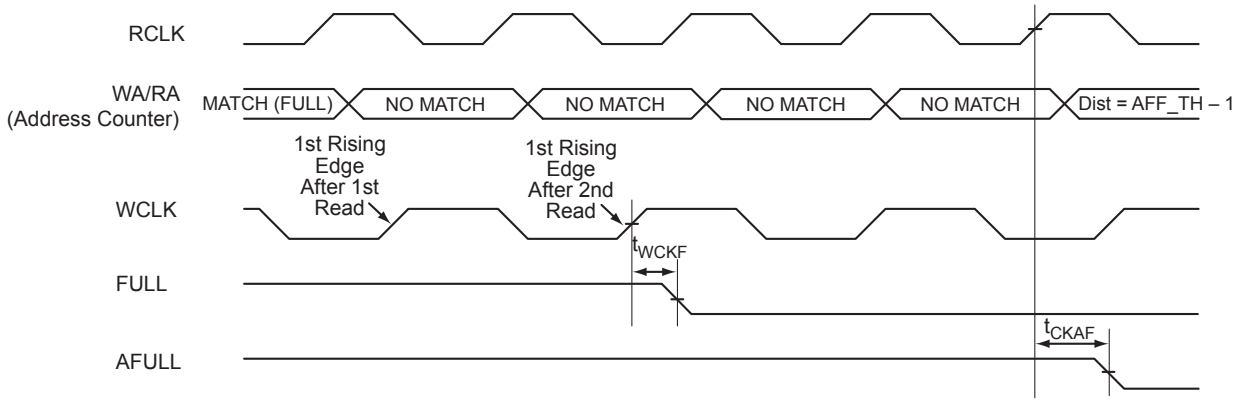


Figure 2-36 • **FIFO FULL Flag and AFULL Flag Deassertion**

Embedded FlashROM Characteristics

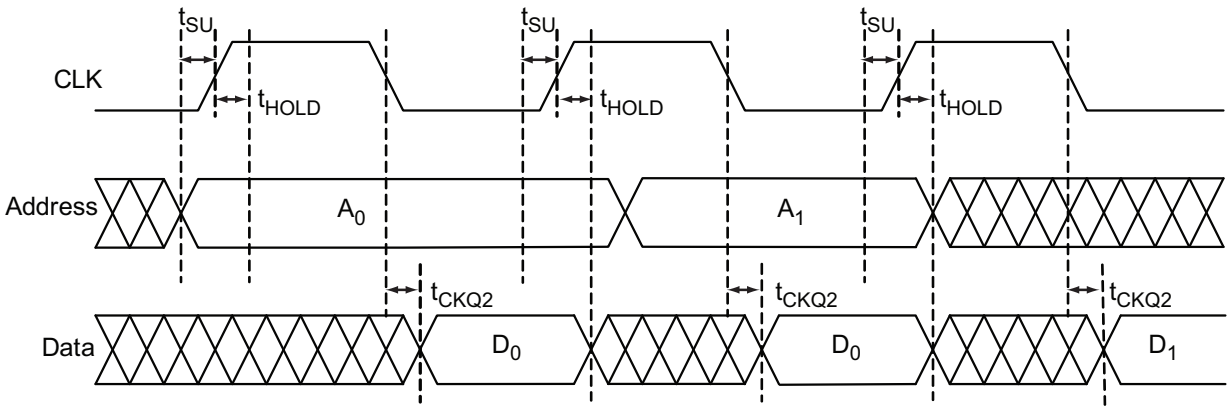


Figure 2-37 • **Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-98 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	17.58	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-99 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	30.94	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

CS281	
Pin Number	**AGLP125 Function**
R15	IO109RSB2
R16	GDA1/IO103RSB1
R18	GDB0/IO102RSB1
R19	GDC0/IO100RSB1
T1	IO171RSB3
T2	GEC0/IO169RSB3
T4	GEB0/IO167RSB3
T5	IO157RSB2
T6	IO158RSB2
T7	IO148RSB2
T8	IO145RSB2
T9	IO143RSB2
T10	GND
T11	IO129RSB2
T12	IO126RSB2
T13	IO125RSB2
T14	IO116RSB2
T15	GDC2/IO107RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO101RSB1
U1	IO160RSB2
U2	GEA1/IO166RSB3
U6	IO151RSB2
U14	IO121RSB2
U18	TRST
U19	GDA0/IO104RSB1
V1	IO159RSB2
V2	VCCIB3
V3	GEC2/IO162RSB2
V4	IO156RSB2
V5	IO153RSB2
V6	GND
V7	IO144RSB2
V8	IO141RSB2
V9	IO140RSB2

CS281	
Pin Number	**AGLP125 Function**
V10	IO133RSB2
V11	IO127RSB2
V12	IO123RSB2
V13	IO120RSB2
V14	GND
V15	IO113RSB2
V16	GDA2/IO105RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO163RSB2
W3	IO155RSB2
W4	IO152RSB2
W5	IO150RSB2
W6	IO147RSB2
W7	IO142RSB2
W8	IO139RSB2
W9	IO136RSB2
W10	VCCIB2
W11	IO128RSB2
W12	IO124RSB2
W13	IO119RSB2
W14	IO115RSB2
W15	IO114RSB2
W16	IO110RSB2
W17	GDB2/IO106RSB2
W18	TCK
W19	GND

CS289	
Pin Number	AGLP030 Function
P2	NC
P3	GND
P4	NC
P5	NC
P6	IO87RSB2
P7	IO80RSB2
P8	GND
P9	IO72RSB2
P10	IO67RSB2
P11	IO61RSB2
P12	NC
P13	VCCIB2
P14	NC
P15	IO60RSB2
P16	IO62RSB2
P17	VJTAG
R1	GND
R2	IO91RSB2
R3	NC
R4	NC
R5	NC
R6	VCCIB2
R7	IO83RSB2
R8	IO78RSB2
R9	IO74RSB2
R10	IO70RSB2
R11	GND
R12	NC
R13	NC
R14	NC
R15	NC
R16	TMS
R17	TRST
T1	IO92RSB3
T2	IO89RSB2
T3	NC
T4	GND

CS289	
Pin Number	AGLP030 Function
T5	NC
T6	IO84RSB2
T7	IO81RSB2
T8	IO76RSB2
T9	VCCIB2
T10	IO69RSB2
T11	IO65RSB2
T12	IO64RSB2
T13	NC
T14	GND
T15	NC
T16	TDI
T17	TDO
U1	FF/IO90RSB2
U2	GND
U3	NC
U4	IO88RSB2
U5	IO86RSB2
U6	IO82RSB2
U7	GND
U8	IO75RSB2
U9	IO73RSB2
U10	IO68RSB2
U11	IO66RSB2
U12	GND
U13	NC
U14	NC
U15	NC
U16	TCK
U17	VPUMP

CS289	
Pin Number	**AGLP125 Function**
P8	GND
P9	IO132RSB2
P10	IO125RSB2
P11	IO126RSB2
P12	IO112RSB2
P13	VCCIB2
P14	IO108RSB2
P15	GDA2/IO105RSB2
P16	GDC2/IO107RSB2
P17	VJTAG
R1	GND
R2	GEA2/IO164RSB2
R3	IO158RSB2
R4	IO155RSB2
R5	IO150RSB2
R6	VCCIB2
R7	IO145RSB2
R8	IO141RSB2
R9	IO134RSB2
R10	IO130RSB2
R11	GND
R12	IO118RSB2
R13	IO116RSB2
R14	IO114RSB2
R15	IO110RSB2
R16	TMS
R17	TRST
T1	GEA1/IO166RSB3
T2	GEC2/IO162RSB2
T3	IO153RSB2
T4	GND
T5	IO147RSB2
T6	IO143RSB2
T7	IO140RSB2
T8	IO139RSB2
T9	VCCIB2
T10	IO131RSB2
T11	IO127RSB2

CS289	
Pin Number	**AGLP125 Function**
T12	IO124RSB2
T13	IO122RSB2
T14	GND
T15	IO115RSB2
T16	TDI
T17	TDO
U1	FF/GEB2/IO163RSB2
U2	GND
U3	IO151RSB2
U4	IO149RSB2
U5	IO146RSB2
U6	IO142RSB2
U7	GND
U8	IO138RSB2
U9	IO136RSB2
U10	IO133RSB2
U11	IO129RSB2
U12	GND
U13	IO123RSB2
U14	IO120RSB2
U15	IO117RSB2
U16	TCK
U17	VPUMP

Revision	Changes	Page
Revision 11 (continued)	The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying IIL and IIH were added. Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366). Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).	2-32
	The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.	2-45 through 2-56
	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM", "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-78

Revision	Changes	Page
Revision 3 (continued)	The table note for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode* to remove the sentence stating that values do not include I/O static contribution.	2-7
	The table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode* was updated to remove VJTAG and VCCI and the statement that values do not include I/O static contribution.	2-7
	The table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode was updated to remove the statement that values do not include I/O static contribution.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO PLUS Flash*Freeze Mode 1 was updated to include VCCPLL. Table note 4 was deleted.	2-8
	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings and Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] were updated to remove static power. The table notes were updated to reflect that power was measured on VCC_I. Table note 2 was added to Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings.	2-9, 2-9
	Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices were updated to change the definition for P_{DC5} from bank static power to bank quiescent power. Table subtitles were added for Table 2-16 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices, Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices, and Table 2-18 • Different Components Contributing to the Static Power Consumption in IGLOO PLUS Devices.	2-10, 2-11
	The "Total Static Power Consumption—P_{STAT}" section was revised.	2-12
	Table 2-32 • Schmitt Trigger Input Hysteresis is new.	2-26
Packaging v1.3	The "CS281" package drawing is new.	4-13
	The "CS281" table for the AGLP125 device is new.	4-13
Revision 3 (continued)	The "CS289" package drawing was incorrect. The graphic was showing the CS281 mechanical drawing and not the CS289 mechanical drawing. This has now been corrected.	4-17
Revision 2 (Jun 2008) Packaging v1.2	The "CS289" table for the AGLP030 device is new.	4-17
Revision 1 (Jun 2008) Packaging v1.1	The "CS289" table for the AGLP060 device is new.	4-20
	The "CS289" table for the AGLP125 device is new.	4-23