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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	201-VFBGA, CSBGA
Supplier Device Package	201-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v2-csg201

Temperature Grade Offerings

Package	AGLP030	AGLP060	AGLP125
CS201	C, I	C, I	–
CS281	–	–	C, I
CS289	C, I	C, I	C, I
VQ128	C, I	–	–
VQ176	–	C, I	–

Notes:
1. *C = Commercial temperature range: 0°C to 85°C junction temperature.*
2. *I = Industrial temperature range: –40°C to 100°C junction temperature.*

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/soc/company/contact/default.aspx.

The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

† The AGLP030 device does not support PLL or SRAM.

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes Low and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO PLUS Device Family User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

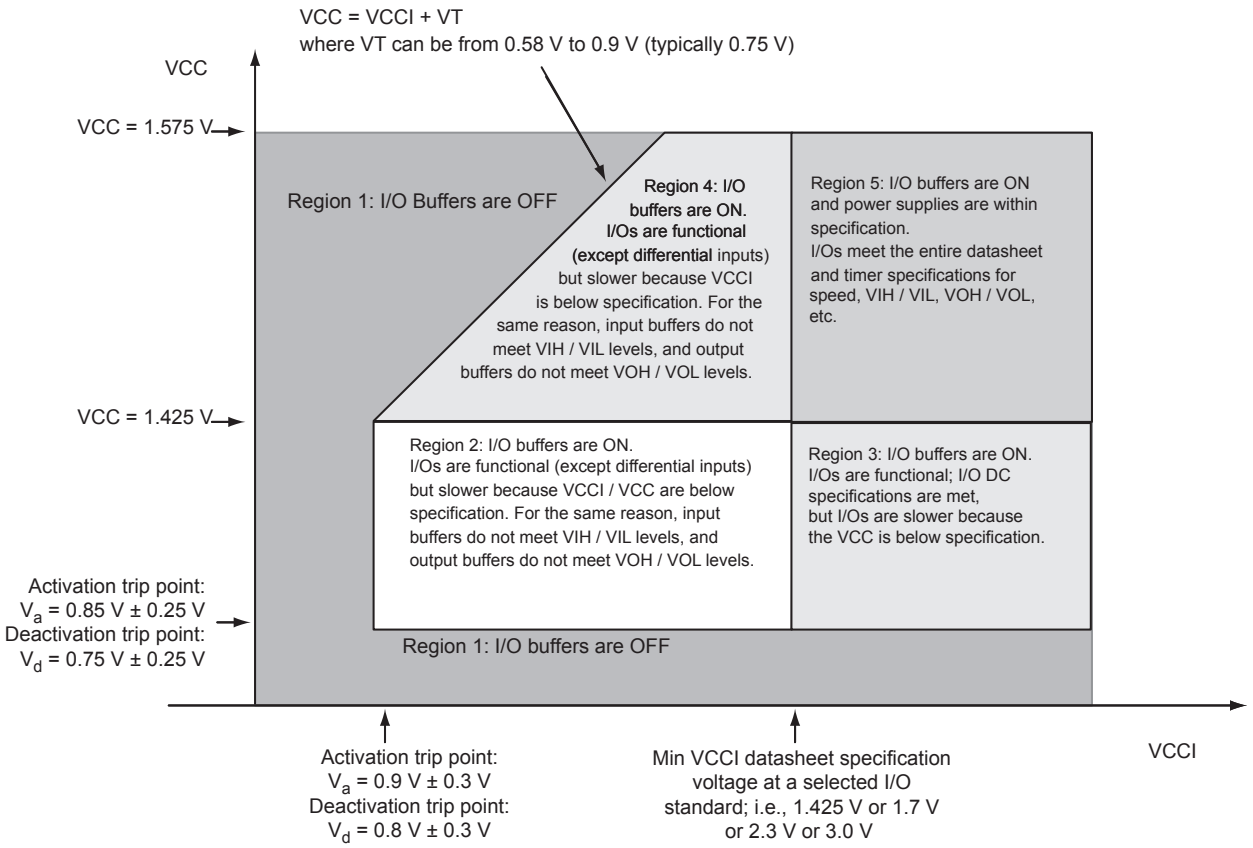

Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microsemi recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Power Supply State per Mode**

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0 V

Table 2-9 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Flash*Freeze Mode***

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V	4	8	13	µA
	1.5 V	6	10	18	µA

*Note: *IDD includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents.*

Table 2-10 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Sleep Mode***

ICCI Current	Core Voltage	AGLP030	AGLP060	AGLP125	Units
VCCI = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	µA
VCCI = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	µA
VCCI = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	µA
VCCI = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	µA
VCCI = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	µA

*Note: *IDD = N_{BANKS} * ICCI*

Table 2-11 • **Quiescent Supply Current (IDD) Characteristics, IGLOO PLUS Shutdown Mode**

	Core Voltage	AGLP030	AGLP060	AGLP125	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	0	µA

Power per I/O Pin

***Table 2-13* • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3 V LVTTL / 3.3 V LVCMOS	3.3	16.26
3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger	3.3	18.95
3.3 V LVCMOS Wide Range[2]	3.3	16.26
3.3 V LVCMOS Wide Range[2] – Schmitt Trigger	3.3	18.95
2.5 V LVCMOS	2.5	4.59
2.5 V LVCMOS – Schmitt Trigger	2.5	6.01
1.8 V LVCMOS	1.8	1.61
1.8 V LVCMOS – Schmitt Trigger	1.8	1.70
1.5 V LVCMOS (JESD8-11)	1.5	0.96
1.5 V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.90
1.2 V LVCMOS[3]	1.2	0.55
1.2 V LVCMOS[3] – Schmitt Trigger	1.2	0.47
1.2 V LVCMOS Wide Range[3]	1.2	0.55
1.2 V LVCMOS Wide Range[3] – Schmitt Trigger	1.2	0.47

Notes:

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

***Table 2-14* • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	127.11
3.3 V LVCMOS Wide Range[3]	5	3.3	127.11
2.5 V LVCMOS	5	2.5	70.71
1.8 V LVCMOS	5	1.8	35.57
1.5 V LVCMOS (JESD8-11)	5	1.5	24.30
1.2 V LVCMOS[4]	5	1.2	15.22
1.2 V LVCMOS Wide Range[4]	5	1.2	15.22

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

– Bit 0 (LSB) = 100%
– Bit 1 = 50%
– Bit 2 = 25%
– …
– Bit 7 (MSB) = 0.78125%
– Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

***Table 2-19* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 2-20* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-34 • Minimum and Maximum DC Input and Output Levels

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

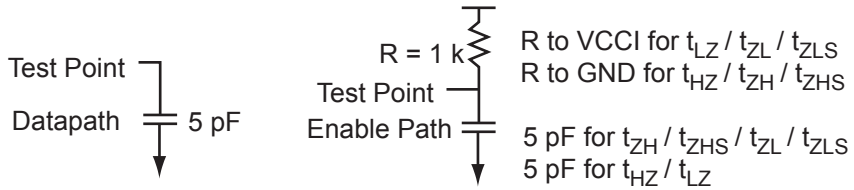

Figure 2-7 • AC Loading

Table 2-35 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-60 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	6.07	0.18	1.16	1.62	0.66	6.19	5.53	2.13	2.02	ns
4 mA	STD	0.97	5.24	0.18	1.16	1.62	0.66	5.34	4.81	2.37	2.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-61 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.65	0.18	1.16	1.62	0.66	2.71	2.43	2.13	2.11	ns
4 mA	STD	0.97	2.29	0.18	1.16	1.62	0.66	2.33	2.00	2.37	2.57	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

Applies to 1.2 V DC Core Voltage

Table 2-62 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	6.57	0.19	1.26	1.80	0.67	6.68	6.01	2.54	2.59	ns
4 mA	STD	0.98	5.72	0.19	1.26	1.80	0.67	5.81	5.27	2.79	3.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-63 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.98	3.08	0.19	1.26	1.80	0.67	3.13	2.82	2.53	2.68	ns
4 mA	STD	0.98	2.71	0.19	1.26	1.80	0.67	2.75	2.39	2.78	3.15	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[3]	IIH[4]
Drive Strength	Equivalent Software Default Drive Strength Option[2]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[5]	Max mA[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to V2 devices only.*
2. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.72	ns
AND2	Y = A · B	t_{PD}	0.86	ns
NAND2	Y = !(A · B)	t_{PD}	1.00	ns
OR2	Y = A + B	t_{PD}	1.26	ns
NOR2	Y = !(A + B)	t_{PD}	1.16	ns
XOR2	Y = A ⊕ B	t_{PD}	1.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.47	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	2.12	ns
MUX2	Y = A !S + B S	t_{PD}	1.24	ns
AND3	Y = A · B · C	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-81 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.26	ns
AND2	Y = A · B	t_{PD}	1.46	ns
NAND2	Y = !(A · B)	t_{PD}	1.78	ns
OR2	Y = A + B	t_{PD}	2.47	ns
NOR2	Y = !(A + B)	t_{PD}	2.17	ns
XOR2	Y = A ⊕ B	t_{PD}	2.62	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.66	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.77	ns
MUX2	Y = A !S + B S	t_{PD}	2.20	ns
AND3	Y = A · B · C	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-61. Table 2-84 to Table 2-89 on page 2-60 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-84* • AGLP030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-85* • AGLP060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.72	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.38	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-92 • RAM4K9
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.68	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{BKS}	BLK setup time	1.37	ns
t_{BKH}	BLK hold time	0.13	ns
t_{DS}	Input data (DIN) setup time	0.59	ns
t_{DH}	Input data (DIN) hold time	0.30	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	2.94	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	1.51	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.29	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.24	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.40	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.72	ns
	RESET Low to data out Low on DOUT (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-96 • FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.68	ns
	RESET Low to Data Out Low on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-97* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.30	ns
t_{DH}	Input Data (WD) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	3.41	ns
	RESET Low to Data Out Low on RD (pipelined)	3.41	ns
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

CS201	
Pin Number	AGLP030 Function
H14	IO45RSB1
H15	IO43RSB1
J1	GEA0/IO107RSB3
J2	IO105RSB3
J3	IO104RSB3
J4	IO102RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	NC
J13	NC
J14	IO52RSB1
J15	IO50RSB1
K1	IO103RSB3
K2	IO101RSB3
K3	IO99RSB3
K4	IO100RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	NC
K13	IO57RSB1
K14	IO49RSB1
K15	IO53RSB1
L1	IO96RSB3
L2	IO98RSB3
L3	IO95RSB3
L4	IO94RSB3
L12	NC
L13	NC
L14	IO51RSB1

CS201	
Pin Number	AGLP030 Function
L15	IO58RSB1
M1	IO93RSB3
M2	IO92RSB3
M3	IO97RSB3
M4	GND
M5	NC
M6	IO79RSB2
M7	IO77RSB2
M8	IO72RSB2
M9	IO70RSB2
M10	IO61RSB2
M11	IO59RSB2
M12	GND
M13	NC
M14	IO55RSB1
M15	IO56RSB1
N1	NC
N2	NC
N3	GND
N4	NC
N5	IO88RSB2
N6	IO81RSB2
N7	IO75RSB2
N8	IO68RSB2
N9	IO66RSB2
N10	IO65RSB2
N11	IO71RSB2
N12	IO63RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	NC
P2	NC
P3	NC
P4	NC

CS201	
Pin Number	AGLP030 Function
P5	IO87RSB2
P6	IO86RSB2
P7	IO84RSB2
P8	IO80RSB2
P9	IO74RSB2
P10	IO73RSB2
P11	IO76RSB2
P12	IO67RSB2
P13	IO64RSB2
P14	VPUMP
P15	TRST
R1	NC
R2	NC
R3	IO91RSB2
R4	FF/IO90RSB2
R5	IO89RSB2
R6	IO83RSB2
R7	IO82RSB2
R8	IO85RSB2
R9	IO78RSB2
R10	IO69RSB2
R11	IO62RSB2
R12	IO60RSB2
R13	TMS
R14	TDI
R15	TCK

CS201	
Pin Number	AGLP060 Function
A1	IO150RSB3
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	IO08RSB0
A5	IO11RSB0
A6	IO15RSB0
A7	IO17RSB0
A8	IO18RSB0
A9	IO22RSB0
A10	IO26RSB0
A11	IO29RSB0
A12	GBC1/IO31RSB0
A13	GBA2/IO36RSB1
A14	IO41RSB1
A15	NC
B1	IO151RSB3
B2	GAB2/IO154RSB3
B3	IO06RSB0
B4	IO09RSB0
B5	IO13RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO25RSB0
B11	IO24RSB0
B12	IO27RSB0
B13	IO37RSB1
B14	IO46RSB1
B15	IO42RSB1
C1	IO155RSB3
C2	GAA2/IO156RSB3
C3	GND
C4	GAA1/IO01RSB0
C5	GAB1/IO03RSB0

CS201	
Pin Number	AGLP060 Function
C6	IO07RSB0
C7	IO16RSB0
C8	IO21RSB0
C9	IO28RSB0
C10	GBB1/IO33RSB0
C11	GBA1/IO35RSB0
C12	GBB2/IO38RSB1
C13	GND
C14	IO48RSB1
C15	IO39RSB1
D1	IO146RSB3
D2	IO144RSB3
D3	IO148RSB3
D4	GND
D5	GAB0/IO02RSB0
D6	GAC1/IO05RSB0
D7	IO14RSB0
D8	IO19RSB0
D9	GBC0/IO30RSB0
D10	GBB0/IO32RSB0
D11	GBA0/IO34RSB0
D12	GND
D13	GBC2/IO40RSB1
D14	IO51RSB1
D15	IO44RSB1
E1	IO142RSB3
E2	IO149RSB3
E3	IO153RSB3
E4	GAC2/IO152RSB3
E12	IO43RSB1
E13	IO49RSB1
E14	GCC0/IO53RSB1
E15	GCB0/IO55RSB1
F1	IO141RSB3
F2	GFC1/IO140RSB3

CS201	
Pin Number	AGLP060 Function
F3	IO145RSB3
F4	IO147RSB3
F6	GND
F7	VCC
F8	VCCIB0
F9	VCCIB0
F10	VCCIB0
F12	IO47RSB1
F13	IO45RSB1
F14	GCC1/IO52RSB1
F15	GCA1/IO56RSB1
G1*	VCOMPLF
G2	GFB0/IO137RSB3
G3	GFC0/IO139RSB3
G4	IO143RSB3
G6	VCCIB3
G7	GND
G8	VCC
G9	GND
G10	GND
G12	IO50RSB1
G13	GCB1/IO54RSB1
G14	GCC2/IO60RSB1
G15	GCA2/IO58RSB1
H1*	VCCPLF
H2	GFA1/IO136RSB3
H3	GFB1/IO138RSB3
H4	NC
H6	VCCIB3
H7	GND
H8	VCC
H9	GND
H10	VCCIB1
H12	GCB2/IO59RSB1
H13	GCA0/IO57RSB1

*Note: *Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.*

CS281	
Pin Number	AGLP125 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO77RSB1
H16	GCB0/IO82RSB1
H18	GCA1/IO83RSB1
H19	GCA2/IO85RSB1
J1	VCOMPLF
J2	GFA0/IO189RSB3
J4	VCCPLF
J5	GFC0/IO193RSB3
J7	GFA2/IO188RSB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO79RSB1
J15	GCA0/IO84RSB1
J16	GCB2/IO86RSB1
J18	IO76RSB1
J19	IO78RSB1
K1	VCCIB3
K2	GFA1/IO190RSB3
K4	GND
K5	IO19RSB0
K7	IO197RSB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO87RSB1

CS281	
Pin Number	AGLP125 Function
K15	IO89RSB1
K16	GND
K18	IO88RSB1
K19	VCCIB1
L1	GFB2/IO187RSB3
L2	IO185RSB3
L4	GFC2/IO186RSB3
L5	IO184RSB3
L7	IO199RSB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO95RSB1
L15	IO91RSB1
L16	NC
L18	IO90RSB1
L19	NC
M1	IO180RSB3
M2	IO179RSB3
M4	IO181RSB3
M5	IO183RSB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO122RSB2
M16	IO93RSB1
M18	IO92RSB1
M19	NC
N1	IO178RSB3
N2	IO175RSB3

CS281	
Pin Number	AGLP125 Function
N4	IO182RSB3
N5	IO161RSB2
N7	GEA2/IO164RSB2
N8	VCCIB2
N9	IO137RSB2
N10	IO135RSB2
N11	IO131RSB2
N12	VCCIB2
N13	VPUMP
N15	IO117RSB2
N16	IO96RSB1
N18	IO98RSB1
N19	IO94RSB1
P1	IO174RSB3
P2	GND
P3	IO176RSB3
P4	IO177RSB3
P5	GEA0/IO165RSB3
P15	IO111RSB2
P16	IO108RSB2
P17	GDC1/IO99RSB1
P18	GND
P19	IO97RSB1
R1	IO173RSB3
R2	IO172RSB3
R4	GEC1/IO170RSB3
R5	GEB1/IO168RSB3
R6	IO154RSB2
R7	IO149RSB2
R8	IO146RSB2
R9	IO138RSB2
R10	IO134RSB2
R11	IO132RSB2
R12	IO130RSB2
R13	IO118RSB2
R14	IO112RSB2

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the IGLOO PLUS datasheet.

Revision	Changes	Page
Revision 17 (December 2015)	Updated Commercial and Industrial temperature range to show junction temperature in "IGLOO PLUS Ordering Information" section and "Temperature Grade Offerings" section (SAR 73547).	1-III, 1-IV
	Removed Ambient temperature parameter in Table 2-2 • Recommended Operating Conditions[1,2] (SAR 73547).	2-2
	Table notes are added to Table 2-2 • Recommended Operating Conditions[1,2] stating that: • VMV pins must be connected to the corresponding VCCI pins. • Software default junction temperature range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial.	2-2
	Updated Table 2-5 • Package Thermal Resistivities (SAR 60078).	2-6
	Added 2 mA drive strength information in the following tables (SAR 57182): • Table 2-36 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage • Table 2-37 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage • Table 2-38 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage • Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-28, 2-28, 2-28, 2-29
	Fixed typo for "VQ128" section in "Package Pin Assignments" section	4-1
Revision 16 (December 2012)	The "IGLOO PLUS Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43175).	III
	The note in Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42566).	2-61, 2-62
	Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 15 (October 2012)	Values updated for IGLOO PLUS V2 or V5 Devices, 1.5 V Core Supply Voltage in Table 2-15 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices and for IGLOO PLUS V2 Devices, 1.2 V Core Supply Voltage in Table 2-17 • Different Components Contributing to Dynamic Power Consumption in IGLOO PLUS Devices (SAR 31988). Also added a new Note to the two tables.	2-10, 2-11
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40277).	N/A
Revision 14 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2

Revision	Changes	Page
Revision 12 (continued)	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide* (SAR 34733).	2-12
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37107).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34887).	2-27
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36963).	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34820). The value for serial clock was missing from these tables and has been restored. The value and units for input cycle-to-cycle jitter were incorrect and have been restored. The note to Table 2-90 • IGLOO PLUS CCC/PLL Specification giving specifications for which measurements done was corrected from VCC/VCCPLL = 1.14 V to VCC/VCCPLL = 1.425 V. The Delay Range in Block: Programmable Delay 2 value in Table 2-91 • IGLOO PLUS CCC/PLL Specification was corrected from 0.025 to 0.863 (SAR 37058).	2-61, 2-62
	Figure 2-28 • Write Access after Read onto Same Address was deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34868). The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-32 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35748).	2-65, 2-68, 2-74, 2-76
	The "Pin Descriptions and Packaging" chapter has been added (SAR 34769).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34769).	4-1
Revision 11 (July 2010)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO PLUS Device Status" table indicates the status for each device in the family.	N/A
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-6
	Conditional statements regarding hot insertion were removed from the description of VI in Table 2-1 • Absolute Maximum Ratings, since all IGLOO PLUS devices are hot insertion enabled.	2-1

Revision	Changes	Page
Revision 10 (Apr 2009) Product Brief v1.5 DC and Switching Characteristics Advance v0.5	The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
Revision 9 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage.	I
	The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new.	1-7
Revision 8 (Jan 2009) Packaging v1.5	The "CS201" pin table was revised to add a note regarding pins G1 and H1.	4-8
Revision 7 (Dec 2008) Product Brief v1.3	A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL."	I
	Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 mm^2.	II
Revision 6 (Oct 2008) DC and Switching Characteristics Advance v0.4	Data was revised significantly in the following tables: Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage	2-22, 2-33
Revision 5 (Aug 2008) Product Brief v1.2	The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table.	I to IV
Packaging v1.4	The "VQ128" package drawing and pin table are new.	4-2
	The "VQ176" package drawing and pin table are new.	4-5
Revision 4 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 3 (Jun 2008) DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set.	N/A
	Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC.	2-2
	Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted.	2-3