# Microchip Technology - AGLP030V2-VQG128 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 792 |
| Total RAM Bits | - |
| Number of I/O | 101 |
| Number of Gates | 30000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 128-TQFP |
| Supplier Device Package | 128-VTQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/aglp030v2-vqg128 |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Security

Nonvolatile, flash-based IGLOO PLUS devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO PLUS devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO PLUS devices (except AGLP030) utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO PLUS devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO PLUS devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO PLUS devices with AES-based security provide a high level of protection for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO PLUS family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO PLUS family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO PLUS device provides the best available security for programmable logic designs.

## Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO PLUS FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

The IGLOO PLUS devices can be operated with a 1.2 V or 1.5 V single-voltage supply for core and I/Os, eliminating the need for additional supplies while minimizing total power consumption.

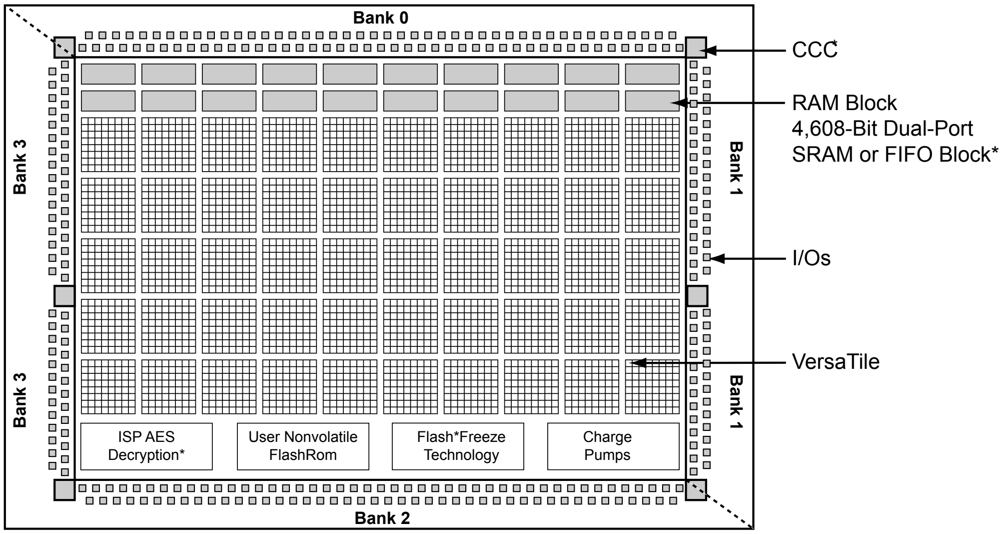
## Instant On

Flash-based IGLOO PLUS devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO PLUS devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO PLUS device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO PLUS devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO PLUS flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs), and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead, it retains all necessary information to resume operation immediately.

## Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based IGLOO PLUS devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm.




Note: *Not supported by AGLP030 devices

**Figure 1-1 • IGLOO PLUS Device Architecture Overview with Four I/O Banks (AGLP030, AGLP060, and AGLP125)**

## Flash*Freeze Technology

The IGLOO PLUS device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Alternatively, they can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. Refer to Figure 1-2 for an illustration of entering/exiting Flash*Freeze mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

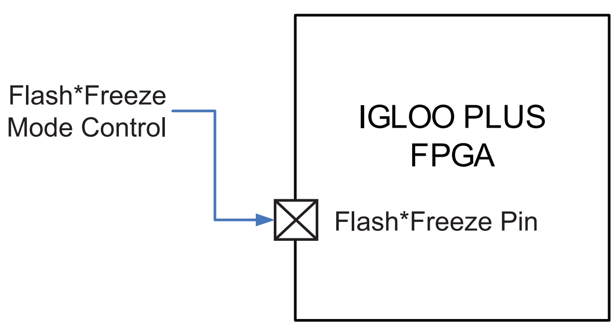



**Figure 1-2 • IGLOO PLUS Flash*Freeze Mode**

# 2 – IGLOO PLUS DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI | DC I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI[1] | I/O input voltage | –0.3 V to 3.6 V | V |
| $T_{STG}$ [2] | Storage temperature | –65 to +150 | °C |
| $T_J$ [2] | Junction temperature | +125 | °C |

*Notes:*

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

## Power per I/O Pin

**Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**

| | VCCI (V) | Dynamic Power PAC9 (µW/MHz) [1] |
|---|---|---|
| **Single-Ended** | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 3.3 | 16.26 |
| 3.3 V LVTTL / 3.3 V LVCMOS – Schmitt Trigger | 3.3 | 18.95 |
| 3.3 V LVCMOS Wide Range[2] | 3.3 | 16.26 |
| 3.3 V LVCMOS Wide Range[2] – Schmitt Trigger | 3.3 | 18.95 |
| 2.5 V LVCMOS | 2.5 | 4.59 |
| 2.5 V LVCMOS – Schmitt Trigger | 2.5 | 6.01 |
| 1.8 V LVCMOS | 1.8 | 1.61 |
| 1.8 V LVCMOS – Schmitt Trigger | 1.8 | 1.70 |
| 1.5 V LVCMOS (JESD8-11) | 1.5 | 0.96 |
| 1.5 V LVCMOS (JESD8-11) – Schmitt Trigger | 1.5 | 0.90 |
| 1.2 V LVCMOS[3] | 1.2 | 0.55 |
| 1.2 V LVCMOS[3] – Schmitt Trigger | 1.2 | 0.47 |
| 1.2 V LVCMOS Wide Range[3] | 1.2 | 0.55 |
| 1.2 V LVCMOS Wide Range[3] – Schmitt Trigger | 1.2 | 0.47 |

*Notes:*

1. *PAC9 is the total dynamic power measured on VCCI.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

**Table 2-14 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**

| | $C_{LOAD}$ (pF) | VCCI (V) | Dynamic Power PAC10 (µW/MHz)[2] |
|---|---|---|---|
| **Single-Ended** | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 5 | 3.3 | 127.11 |
| 3.3 V LVCMOS Wide Range[3] | 5 | 3.3 | 127.11 |
| 2.5 V LVCMOS | 5 | 2.5 | 70.71 |
| 1.8 V LVCMOS | 5 | 1.8 | 35.57 |
| 1.5 V LVCMOS (JESD8-11) | 5 | 1.5 | 24.30 |
| 1.2 V LVCMOS[4] | 5 | 1.2 | 15.22 |
| 1.2 V LVCMOS Wide Range[4] | 5 | 1.2 | 15.22 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PAC10 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO PLUS V2 devices only, operating at VCCI ≥ VCC.*

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

### *Methodology*

#### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### Total Static Power Consumption—$P_{STAT}$

$P_{STAT}$ = (PDC1 or PDC2 or PDC3) + $N_{BANKS}$ * PDC5

$N_{BANKS}$ is the number of I/O banks powered in the design.

#### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

#### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (PAC1 + N_{SPINE}*PAC2 + N_{ROW}*PAC3 + N_{S\text{-}CELL}* PAC4) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

#### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Combinatorial Cells Contribution—$P_{C-CELL}$

$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$

$N_{C-CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Routing Net Contribution—$P_{NET}$

$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$

$N_{S-CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C-CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Input Buffer Contribution—$P_{INPUTS}$

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-19 on page 2-14.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-20 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### RAM Contribution—$P_{MEMORY}$

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$

$N_{BLOCKS}$ is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

$\beta_2$ is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

$\beta_3$ is the RAM enable rate for write operations—guidelines are provided in Table 2-20 on page 2-14.

### PLL Contribution—$P_{PLL}$

$P_{PLL} = PDC4 + PAC1_3 * F_{CLKOUT}$

$F_{CLKOUT}$ is the output clock frequency.[1]

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY)}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.31 | 0.19 | 0.99 | 1.37 | 0.67 | 2.34 | 1.86 | 2.65 | 3.38 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 5 pF | – | 0.98 | 3.21 | 0.19 | 1.32 | 1.92 | 0.67 | 3.21 | 2.52 | 3.73 | 4.73 | ns |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | 5 pF | – | 0.98 | 2.29 | 0.19 | 1.19 | 1.40 | 0.67 | 2.32 | 1.94 | 2.65 | 3.27 | ns |
| 1.8 V LVCMOS | 8 mA | 8 mA | High | 5 pF | – | 0.98 | 2.45 | 0.19 | 1.12 | 1.61 | 0.67 | 2.48 | 2.16 | 2.71 | 3.16 | ns |
| 1.5 V LVCMOS | 4 mA | 4 mA | High | 5 pF | – | 0.98 | 2.71 | 0.19 | 1.26 | 1.80 | 0.67 | 2.75 | 2.39 | 2.78 | 3.15 | ns |
| 1.2 V LVCMOS | 2 mA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |
| 1.2 V LVCMOS Wide Range[3] | 100 µA | 2 mA | High | 5 pF | – | 0.98 | 3.38 | 0.19 | 1.57 | 2.34 | 0.67 | 3.26 | 2.78 | 2.99 | 3.24 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Characteristics

### *Applies to 1.5 V DC Core Voltage*

***Table 2-36* • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 4 mA | STD | 0.97 | 3.94 | 0.18 | 0.85 | 1.15 | 0.66 | 4.02 | 3.46 | 1.82 | 1.87 | ns |
| 6 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 8 mA | STD | 0.97 | 3.20 | 0.18 | 0.85 | 1.15 | 0.66 | 3.27 | 2.94 | 2.04 | 2.27 | ns |
| 12 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |
| 16 mA | STD | 0.97 | 2.72 | 0.18 | 0.85 | 1.15 | 0.66 | 2.78 | 2.57 | 2.20 | 2.53 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-37* • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 4 mA | STD | 0.97 | 2.36 | 0.18 | 0.85 | 1.15 | 0.66 | 2.41 | 1.90 | 1.82 | 1.98 | ns |
| 6 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 8 mA | STD | 0.97 | 1.96 | 0.18 | 0.85 | 1.15 | 0.66 | 2.01 | 1.56 | 2.04 | 2.38 | ns |
| 12 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |
| 16 mA | STD | 0.97 | 1.76 | 0.18 | 0.85 | 1.15 | 0.66 | 1.80 | 1.39 | 2.20 | 2.64 | ns |

*Notes:*

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Software default selection highlighted in gray.*

### *Applies to 1.2 V DC Core Voltage*

***Table 2-38* • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 4 mA | STD | 0.98 | 4.56 | 0.19 | 0.99 | 1.37 | 0.67 | 4.63 | 3.98 | 2.26 | 2.57 | ns |
| 6 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 1.37 | 0.67 | 3.96 | 3.45 | 2.49 | 2.98 | ns |
| 8 mA | STD | 0.98 | 3.80 | 0.19 | 0.99 | 137 | 0.67 | 3.86 | 3.45 | 2.49 | 2.98 | ns |
| 12 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |
| 16 mA | STD | 0.98 | 3.31 | 0.19 | 0.99 | 1.37 | 0.67 | 3.36 | 3.07 | 2.65 | 3.25 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Output Register

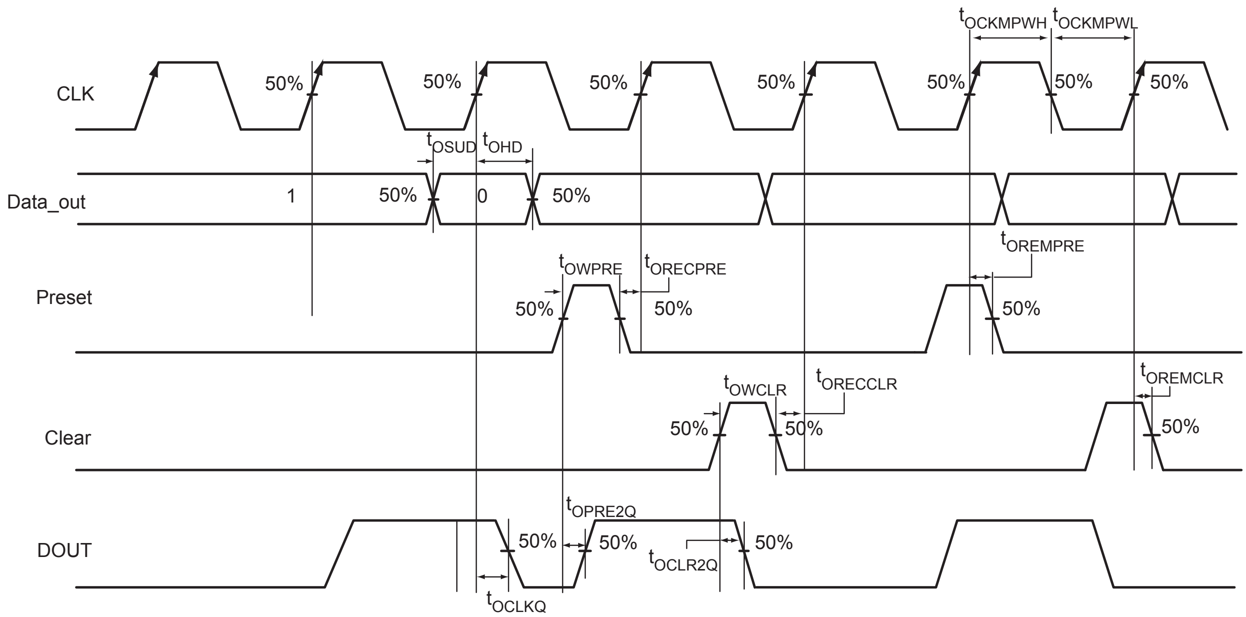



***Figure 2-15 •*** **Output Register Timing Diagram**

### Timing Characteristics

#### *1.5 V DC Core Voltage*

***Table 2-76 •*** **Output Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | 0.66 | ns |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | 0.33 | ns |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | 0.00 | ns |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | 0.82 | ns |
| $t_{OPRE2Q}$ | Asynchronous Preset-to-Q of the Output Data Register | 0.88 | ns |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OREMPRE}$ | Asynchronous Preset Removal Time for the Output Data Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Data Register | 0.24 | ns |
| $t_{OWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Data Register | 0.19 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output Data Register | 0.31 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-79 • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.06 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 0.52 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.25 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.36 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{OERECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

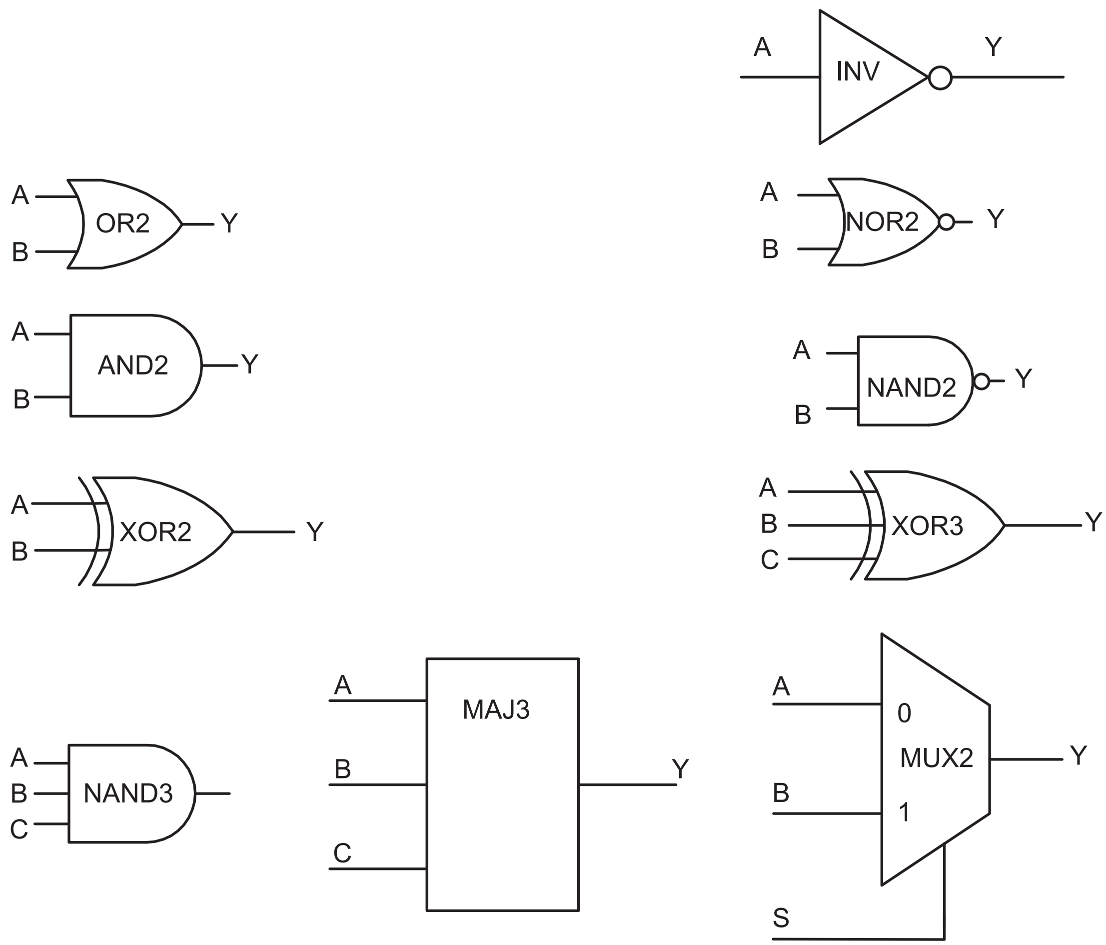



***Figure 2-17 •* Sample of Combinatorial Cells**

### 1.2 V DC Core Voltage

***Table 2-83*** **• Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 1.61 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 1.17 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 1.29 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.87 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.89 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.24 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.46 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.95 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.95 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

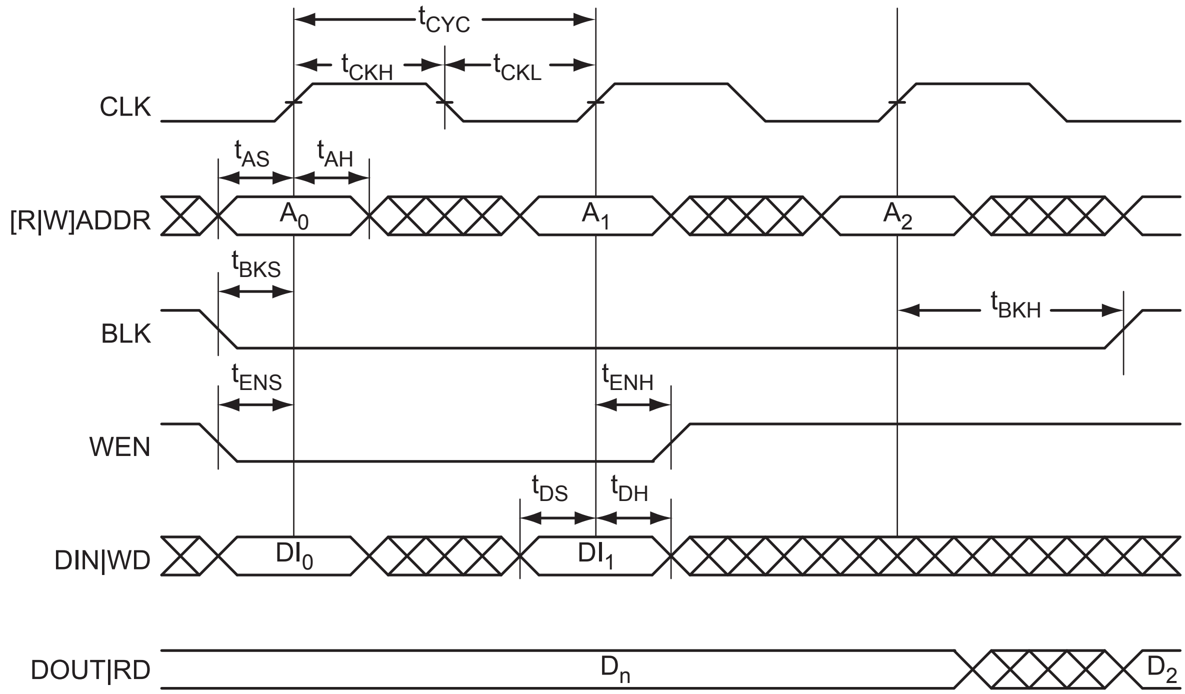



***Figure 2-26* • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

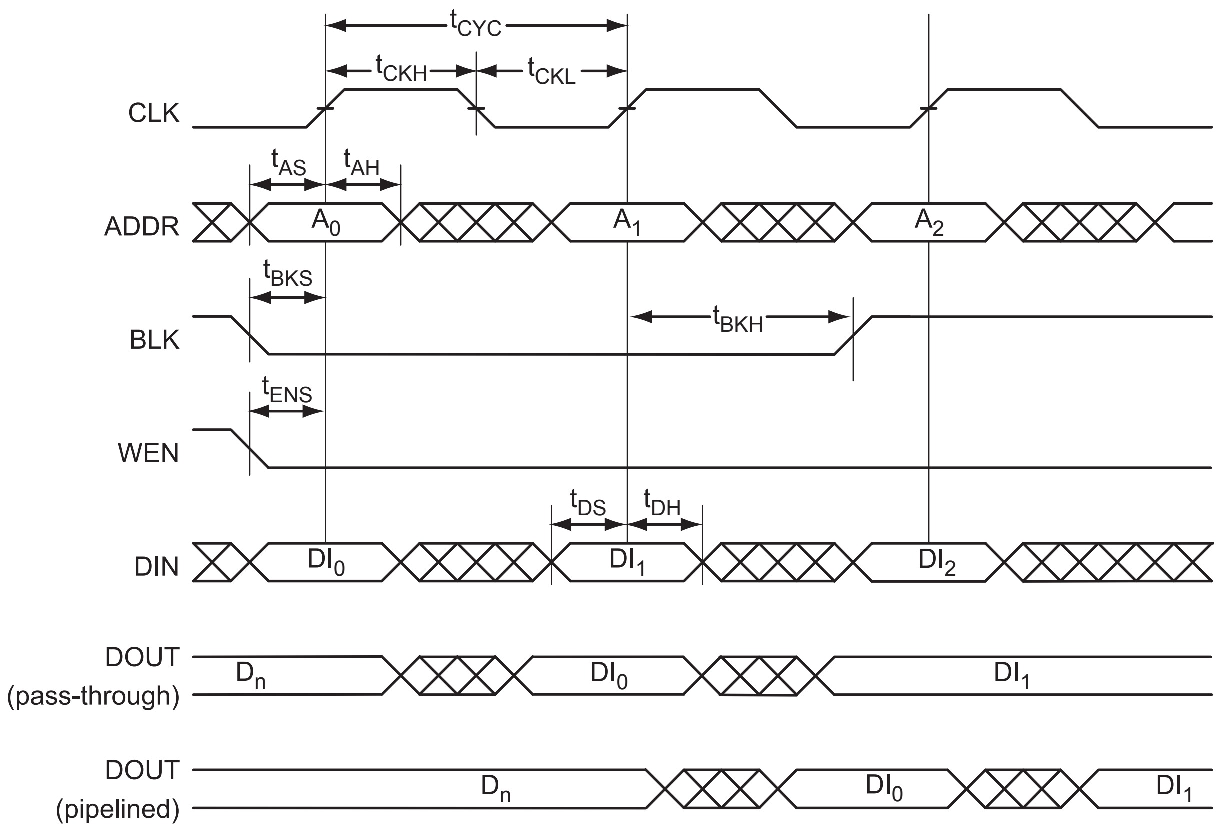



***Figure 2-27* • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

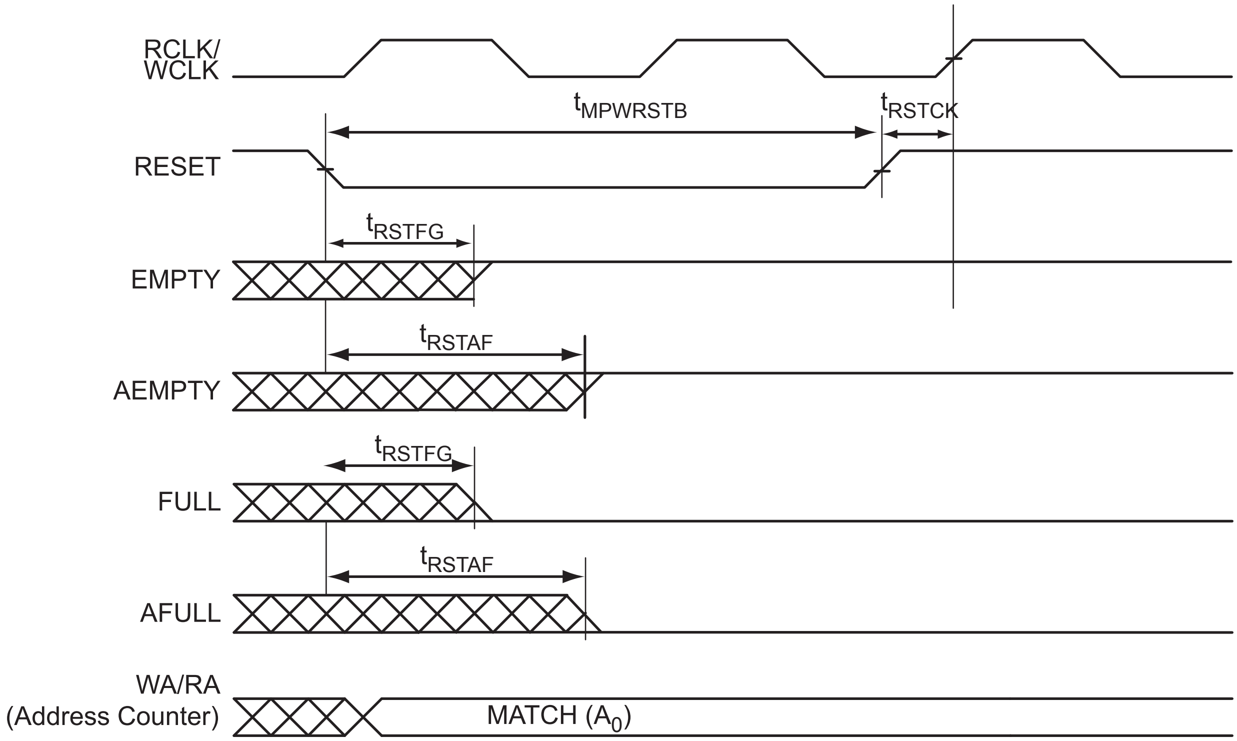



***Figure 2-32*** **• FIFO Reset**

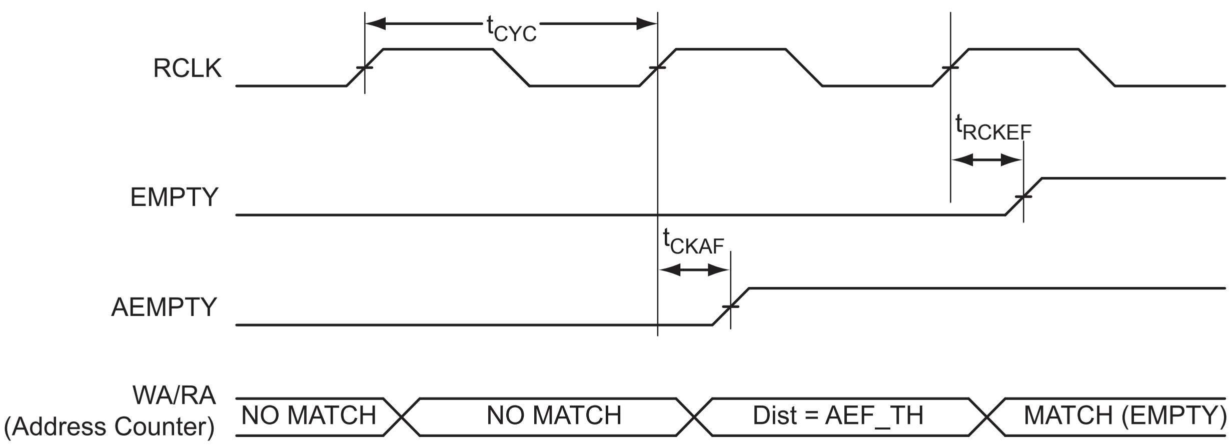



***Figure 2-33*** **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

# JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

## Timing Characteristics

### 1.5 V DC Core Voltage

***Table 2-100* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.00 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 2.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.00 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 2.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 8.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 25.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 15 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 0.58 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### 1.2 V DC Core Voltage

***Table 2-101* • JTAG 1532**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DISU}$ | Test Data Input Setup Time | 1.50 | ns |
| $t_{DIHD}$ | Test Data Input Hold Time | 3.00 | ns |
| $t_{TMSSU}$ | Test Mode Select Setup Time | 1.50 | ns |
| $t_{TMDHD}$ | Test Mode Select Hold Time | 3.00 | ns |
| $t_{TCK2Q}$ | Clock to Q (data out) | 11.00 | ns |
| $t_{RSTB2Q}$ | Reset to Q (data out) | 30.00 | ns |
| $F_{TCKMAX}$ | TCK Maximum Frequency | 9.00 | MHz |
| $t_{TRSTREM}$ | ResetB Removal Time | 1.18 | ns |
| $t_{TRSTREC}$ | ResetB Recovery Time | 0.00 | ns |
| $t_{TRSTMPW}$ | ResetB Minimum Pulse | TBD | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

| VQ128 | |
|---|---|
| Pin Number | AGLP030 Function |
| 106 | IO26RSB0 |
| 107 | IO25RSB0 |
| 108 | IO23RSB0 |
| 109 | IO22RSB0 |
| 110 | IO21RSB0 |
| 111 | IO19RSB0 |
| 112 | IO18RSB0 |
| 113 | VCC |
| 114 | IO17RSB0 |
| 115 | IO16RSB0 |
| 116 | IO14RSB0 |
| 117 | IO13RSB0 |
| 118 | IO12RSB0 |
| 119 | IO10RSB0 |
| 120 | IO09RSB0 |
| 121 | VCCIB0 |
| 122 | GND |
| 123 | IO07RSB0 |
| 124 | IO05RSB0 |
| 125 | IO03RSB0 |
| 126 | IO02RSB0 |
| 127 | IO01RSB0 |
| 128 | IO00RSB0 |

| CS201 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| A1 | IO150RSB3 |
| A2 | GAA0/IO00RSB0 |
| A3 | GAC0/IO04RSB0 |
| A4 | IO08RSB0 |
| A5 | IO11RSB0 |
| A6 | IO15RSB0 |
| A7 | IO17RSB0 |
| A8 | IO18RSB0 |
| A9 | IO22RSB0 |
| A10 | IO26RSB0 |
| A11 | IO29RSB0 |
| A12 | GBC1/IO31RSB0 |
| A13 | GBA2/IO36RSB1 |
| A14 | IO41RSB1 |
| A15 | NC |
| B1 | IO151RSB3 |
| B2 | GAB2/IO154RSB3 |
| B3 | IO06RSB0 |
| B4 | IO09RSB0 |
| B5 | IO13RSB0 |
| B6 | IO10RSB0 |
| B7 | IO12RSB0 |
| B8 | IO20RSB0 |
| B9 | IO23RSB0 |
| B10 | IO25RSB0 |
| B11 | IO24RSB0 |
| B12 | IO27RSB0 |
| B13 | IO37RSB1 |
| B14 | IO46RSB1 |
| B15 | IO42RSB1 |
| C1 | IO155RSB3 |
| C2 | GAA2/IO156RSB3 |
| C3 | GND |
| C4 | GAA1/IO01RSB0 |
| C5 | GAB1/IO03RSB0 |

| CS201 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| C6 | IO07RSB0 |
| C7 | IO16RSB0 |
| C8 | IO21RSB0 |
| C9 | IO28RSB0 |
| C10 | GBB1/IO33RSB0 |
| C11 | GBA1/IO35RSB0 |
| C12 | GBB2/IO38RSB1 |
| C13 | GND |
| C14 | IO48RSB1 |
| C15 | IO39RSB1 |
| D1 | IO146RSB3 |
| D2 | IO144RSB3 |
| D3 | IO148RSB3 |
| D4 | GND |
| D5 | GAB0/IO02RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | IO14RSB0 |
| D8 | IO19RSB0 |
| D9 | GBC0/IO30RSB0 |
| D10 | GBB0/IO32RSB0 |
| D11 | GBA0/IO34RSB0 |
| D12 | GND |
| D13 | GBC2/IO40RSB1 |
| D14 | IO51RSB1 |
| D15 | IO44RSB1 |
| E1 | IO142RSB3 |
| E2 | IO149RSB3 |
| E3 | IO153RSB3 |
| E4 | GAC2/IO152RSB3 |
| E12 | IO43RSB1 |
| E13 | IO49RSB1 |
| E14 | GCC0/IO53RSB1 |
| E15 | GCB0/IO55RSB1 |
| F1 | IO141RSB3 |
| F2 | GFC1/IO140RSB3 |

| CS201 | |
|---|---|
| **Pin Number** | **AGLP060 Function** |
| F3 | IO145RSB3 |
| F4 | IO147RSB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCCIB0 |
| F9 | VCCIB0 |
| F10 | VCCIB0 |
| F12 | IO47RSB1 |
| F13 | IO45RSB1 |
| F14 | GCC1/IO52RSB1 |
| F15 | GCA1/IO56RSB1 |
| G1* | VCOMPLF |
| G2 | GFB0/IO137RSB3 |
| G3 | GFC0/IO139RSB3 |
| G4 | IO143RSB3 |
| G6 | VCCIB3 |
| G7 | GND |
| G8 | VCC |
| G9 | GND |
| G10 | GND |
| G12 | IO50RSB1 |
| G13 | GCB1/IO54RSB1 |
| G14 | GCC2/IO60RSB1 |
| G15 | GCA2/IO58RSB1 |
| H1* | VCCPLF |
| H2 | GFA1/IO136RSB3 |
| H3 | GFB1/IO138RSB3 |
| H4 | NC |
| H6 | VCCIB3 |
| H7 | GND |
| H8 | VCC |
| H9 | GND |
| H10 | VCCIB1 |
| H12 | GCB2/IO59RSB1 |
| H13 | GCA0/IO57RSB1 |

*Note:* **Pin numbers G1 and H1 must be connected to ground because a PLL is not supported for AGLP060-CS/G201.*

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| A1 | GAB1/IO03RSB0 |
| A2 | NC |
| A3 | NC |
| A4 | GND |
| A5 | IO10RSB0 |
| A6 | IO14RSB0 |
| A7 | IO16RSB0 |
| A8 | IO18RSB0 |
| A9 | GND |
| A10 | IO23RSB0 |
| A11 | IO27RSB0 |
| A12 | NC |
| A13 | NC |
| A14 | GND |
| A15 | NC |
| A16 | NC |
| A17 | GBC0/IO30RSB0 |
| B1 | GAA1/IO01RSB0 |
| B2 | GND |
| B3 | NC |
| B4 | NC |
| B5 | IO07RSB0 |
| B6 | NC |
| B7 | VCCIB0 |
| B8 | IO17RSB0 |
| B9 | IO19RSB0 |
| B10 | IO24RSB0 |
| B11 | IO28RSB0 |
| B12 | VCCIB0 |
| B13 | NC |
| B14 | NC |
| B15 | NC |
| B16 | GBC1/IO31RSB0 |
| B17 | GND |
| C1 | IO155RSB3 |
| C2 | GAA0/IO00RSB0 |
| C3 | GAC0/IO04RSB0 |
| C4 | NC |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| C5 | VCCIB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO21RSB0 |
| C10 | GND |
| C11 | IO29RSB0 |
| C12 | NC |
| C13 | NC |
| C14 | NC |
| C15 | GND |
| C16 | GBA0/IO34RSB0 |
| C17 | IO39RSB1 |
| D1 | IO150RSB3 |
| D2 | IO151RSB3 |
| D3 | GND |
| D4 | GAB0/IO02RSB0 |
| D5 | NC |
| D6 | NC |
| D7 | NC |
| D8 | GND |
| D9 | IO20RSB0 |
| D10 | IO25RSB0 |
| D11 | NC |
| D12 | NC |
| D13 | GND |
| D14 | GBB0/IO32RSB0 |
| D15 | GBA1/IO35RSB0 |
| D16 | IO37RSB1 |
| D17 | IO42RSB1 |
| E1 | VCCIB3 |
| E2 | IO147RSB3 |
| E3 | GAC2/IO152RSB3 |
| E4 | GAA2/IO156RSB3 |
| E5 | GAC1/IO05RSB0 |
| E6 | NC |
| E7 | IO06RSB0 |
| E8 | IO11RSB0 |

| CS289 | |
|---|---|
| Pin Number | AGLP060 Function |
| E9 | IO22RSB0 |
| E10 | IO26RSB0 |
| E11 | VCCIB0 |
| E12 | NC |
| E13 | GBB1/IO33RSB0 |
| E14 | GBA2/IO36RSB1 |
| E15 | GBB2/IO38RSB1 |
| E16 | VCCIB1 |
| E17 | IO44RSB1 |
| F1 | GFC1/IO140RSB3 |
| F2 | IO142RSB3 |
| F3 | IO149RSB3 |
| F4 | VCCIB3 |
| F5 | GAB2/IO154RSB3 |
| F6 | IO153RSB3 |
| F7 | NC |
| F8 | IO08RSB0 |
| F9 | IO12RSB0 |
| F10 | NC |
| F11 | NC |
| F12 | NC |
| F13 | GBC2/IO40RSB1 |
| F14 | GND |
| F15 | IO43RSB1 |
| F16 | IO46RSB1 |
| F17 | IO45RSB1 |
| G1 | GFC0/IO139RSB3 |
| G2 | GND |
| G3 | IO144RSB3 |
| G4 | IO145RSB3 |
| G5 | IO146RSB3 |
| G6 | IO148RSB3 |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO48RSB1 |

| CS289 | |
|---|---|
| Pin Number | AGLP125 Function |
| A1 | GAB1/IO03RSB0 |
| A2 | IO11RSB0 |
| A3 | IO08RSB0 |
| A4 | GND |
| A5 | IO19RSB0 |
| A6 | IO24RSB0 |
| A7 | IO26RSB0 |
| A8 | IO30RSB0 |
| A9 | GND |
| A10 | IO35RSB0 |
| A11 | IO38RSB0 |
| A12 | IO40RSB0 |
| A13 | IO42RSB0 |
| A14 | GND |
| A15 | IO48RSB0 |
| A16 | IO54RSB0 |
| A17 | GBC0/IO57RSB0 |
| B1 | GAA1/IO01RSB0 |
| B2 | GND |
| B3 | IO06RSB0 |
| B4 | IO13RSB0 |
| B5 | IO15RSB0 |
| B6 | IO21RSB0 |
| B7 | VCCIB0 |
| B8 | IO28RSB0 |
| B9 | IO31RSB0 |
| B10 | IO37RSB0 |
| B11 | IO39RSB0 |
| B12 | VCCIB0 |
| B13 | IO44RSB0 |
| B14 | IO46RSB0 |
| B15 | IO49RSB0 |
| B16 | GBC1/IO58RSB0 |
| B17 | GND |
| C1 | IO210RSB3 |
| C2 | GAA0/IO00RSB0 |
| C3 | GAC0/IO04RSB0 |
| C4 | IO09RSB0 |

| CS289 | |
|---|---|
| Pin Number | AGLP125 Function |
| C5 | VCCIB0 |
| C6 | IO17RSB0 |
| C7 | IO23RSB0 |
| C8 | IO27RSB0 |
| C9 | IO33RSB0 |
| C10 | GND |
| C11 | IO43RSB0 |
| C12 | IO45RSB0 |
| C13 | IO50RSB0 |
| C14 | IO52RSB0 |
| C15 | GND |
| C16 | GBA0/IO61RSB0 |
| C17 | IO68RSB1 |
| D1 | IO204RSB3 |
| D2 | IO205RSB3 |
| D3 | GND |
| D4 | GAB0/IO02RSB0 |
| D5 | IO07RSB0 |
| D6 | IO10RSB0 |
| D7 | IO18RSB0 |
| D8 | GND |
| D9 | IO34RSB0 |
| D10 | IO41RSB0 |
| D11 | IO47RSB0 |
| D12 | IO55RSB0 |
| D13 | GND |
| D14 | GBB0/IO59RSB0 |
| D15 | GBA1/IO62RSB0 |
| D16 | IO66RSB1 |
| D17 | IO70RSB1 |
| E1 | VCCIB3 |
| E2 | IO200RSB3 |
| E3 | GAC2/IO207RSB3 |
| E4 | GAA2/IO211RSB3 |
| E5 | GAC1/IO05RSB0 |
| E6 | IO12RSB0 |
| E7 | IO16RSB0 |
| E8 | IO22RSB0 |

| CS289 | |
|---|---|
| Pin Number | AGLP125 Function |
| E9 | IO32RSB0 |
| E10 | IO36RSB0 |
| E11 | VCCIB0 |
| E12 | IO56RSB0 |
| E13 | GBB1/IO60RSB0 |
| E14 | GBA2/IO63RSB1 |
| E15 | GBB2/IO65RSB1 |
| E16 | VCCIB1 |
| E17 | IO73RSB1 |
| F1 | GFC1/IO194RSB3 |
| F2 | IO196RSB3 |
| F3 | IO202RSB3 |
| F4 | VCCIB3 |
| F5 | GAB2/IO209RSB3 |
| F6 | IO208RSB3 |
| F7 | IO14RSB0 |
| F8 | IO20RSB0 |
| F9 | IO25RSB0 |
| F10 | IO29RSB0 |
| F11 | IO51RSB0 |
| F12 | IO53RSB0 |
| F13 | GBC2/IO67RSB1 |
| F14 | GND |
| F15 | IO75RSB1 |
| F16 | IO71RSB1 |
| F17 | IO77RSB1 |
| G1 | GFC0/IO193RSB3 |
| G2 | GND |
| G3 | IO198RSB3 |
| G4 | IO203RSB3 |
| G5 | IO201RSB3 |
| G6 | IO206RSB3 |
| G7 | GND |
| G8 | GND |
| G9 | VCC |
| G10 | GND |
| G11 | GND |
| G12 | IO72RSB1 |

| Revision | Changes | Page |
|---|---|---|
| **Revision 10 (Apr 2009)**<br>Product Brief v1.5<br>DC and Switching Characteristics Advance v0.5 | The –F speed grade is no longer offered for IGLOO PLUS devices. References to it have been removed from the document. The speed grade column and note regarding –F speed grade were removed from "IGLOO PLUS Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed. | III, IV |
| **Revision 9 (Feb 2009)**<br>Product Brief v1.4 | The "Advanced I/O" section was revised to add two bullets regarding support of wide range power supply voltage. | I |
| | The "I/Os with Advanced I/O Standards" section was revised to add 3.0 V wide range to the list of supported voltages. The "Wide Range I/O Support" section is new. | 1-7 |
| **Revision 8 (Jan 2009)**<br>Packaging v1.5 | The "CS201" pin table was revised to add a note regarding pins G1 and H1. | 4-8 |
| **Revision 7 (Dec 2008)**<br>Product Brief v1.3 | A note was added to IGLOO PLUS Devices: "AGLP060 in CS201 does not support the PLL." | I |
| | Table 2 • IGLOO PLUS FPGAs Package Size Dimensions was updated to change the nominal size of VQ176 from 100 to 400 $mm^2$. | II |
| **Revision 6 (Oct 2008)**<br>DC and Switching Characteristics Advance v0.4 | Data was revised significantly in the following tables:<br>Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V<br>Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings, STD Speed Grade Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V<br>Table 2-50 • 2.5 LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage<br>Table 2-51 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage | 2-22, 2-33 |
| **Revision 5 (Aug 2008)**<br>Product Brief v1.2 | The VQ128 and VQ176 packages were added to Table 1 • IGLOO PLUS Product Family, the "I/Os Per Package [1]" table, Table 2 • IGLOO PLUS FPGAs Package Size Dimensions, "IGLOO PLUS Ordering Information", and the "Temperature Grade Offerings" table. | I to IV |
| Packaging v1.4 | The "VQ128" package drawing and pin table are new. | 4-2 |
| | The "VQ176" package drawing and pin table are new. | 4-5 |
| **Revision 4 (Jul 2008)**<br>Product Brief v1.1<br>DC and Switching Characteristics Advance v0.3 | As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V. | N/A |
| **Revision 3 (Jun 2008)**<br>DC and Switching Characteristics Advance v0.2 | Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. | N/A |
| | Table note 3 was updated in Table 2-2 • Recommended Operating Conditions[1,2] to add the sentence, "VCCI should be at the same voltage within a given I/O bank." References to table notes 5, 6, 7, and 8 were added. Reference to table note 3 was removed from VPUMP Operation and placed next to VCC. | 2-2 |
| | Table 2-4 • Overshoot and Undershoot Limits [1] was revised to remove "as measured on quiet I/Os" from the title. Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was deleted. | 2-3 |