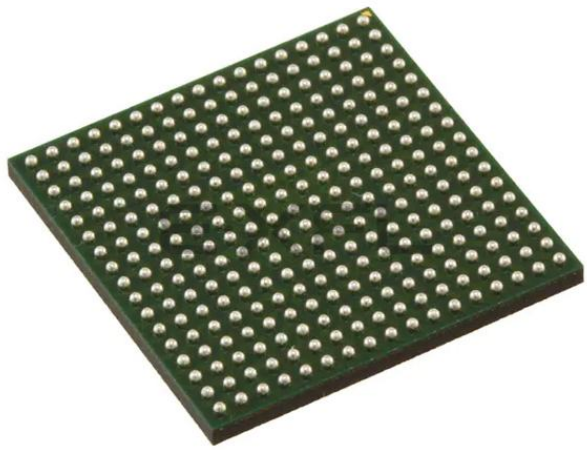


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v5-cs289

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

† The AGLP030 device does not support PLL or SRAM.

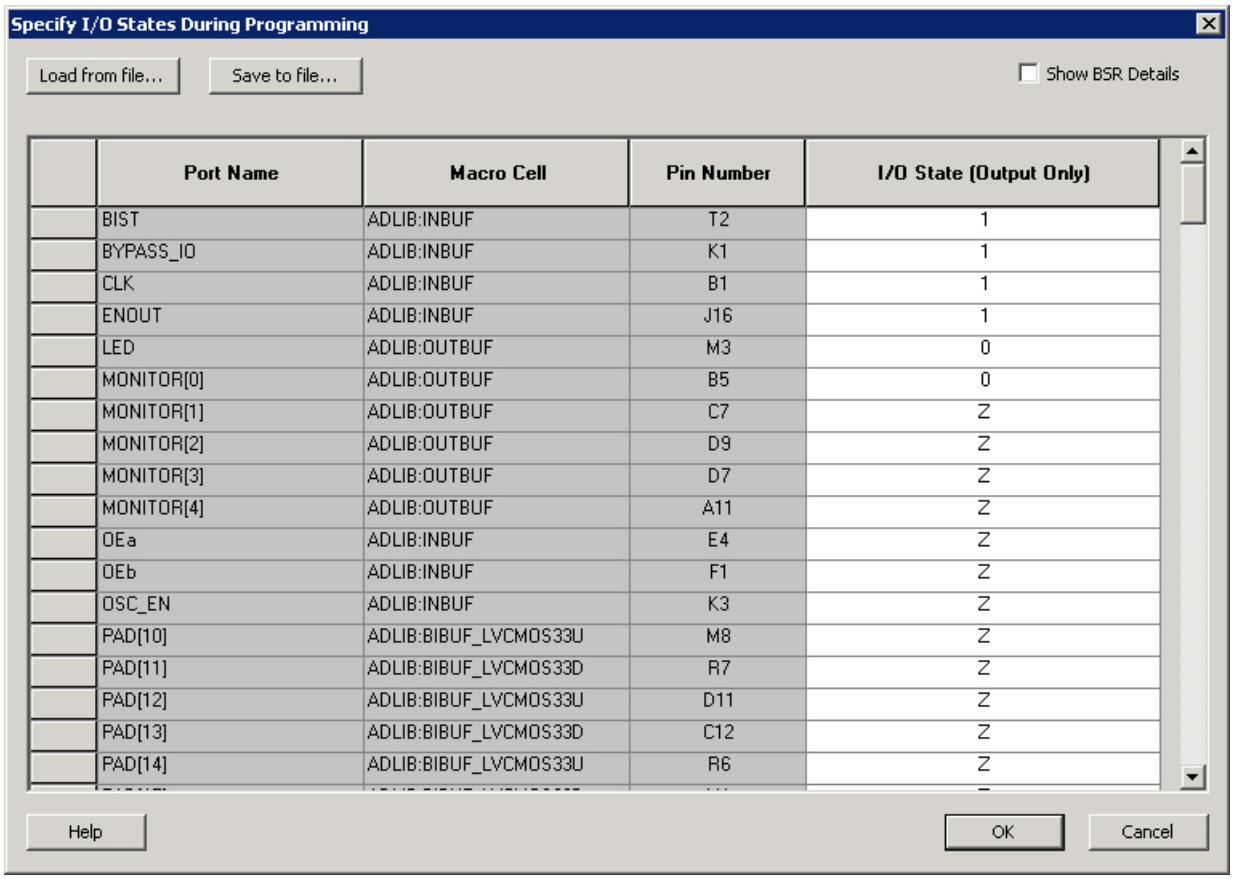


Figure 1-4 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – IGLOO PLUS DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
V_I[1]	I/O input voltage	–0.3 V to 3.6 V	V
T_{STG}[2]	Storage temperature	–65 to +150	°C
T_J[2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

P_{STAT} = (PDC1 or PDC2 or PDC3) + N_{BANKS} * PDC5

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

P_{CLOCK} = (PAC1 + N_{SPINE}*PAC2 + N_{ROW}*PAC3 + $N_{S\text{-}CELL}$* PAC4) * F_{CLK}

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19 on page 2-14.

F_{CLK} is the global clock signal frequency.

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax - VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	**IOSL (mA)***	**IOSH (mA)***
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 µA	26	20

*Note: *T_J = 100°C*

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range[1]		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[3]	IIH[4]
Drive Strength	Equivalent Software Default Drive Strength Option[2]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[5]	Max mA[5]	µA[6]	µA[6]
100 µA	2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *Applicable to V2 devices only.*
2. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
5. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
6. *Currents are measured at 85°C junction temperature.*
7. *Software default selection highlighted in gray.*

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.*

Fully Registered I/O Buffers with Asynchronous Clear

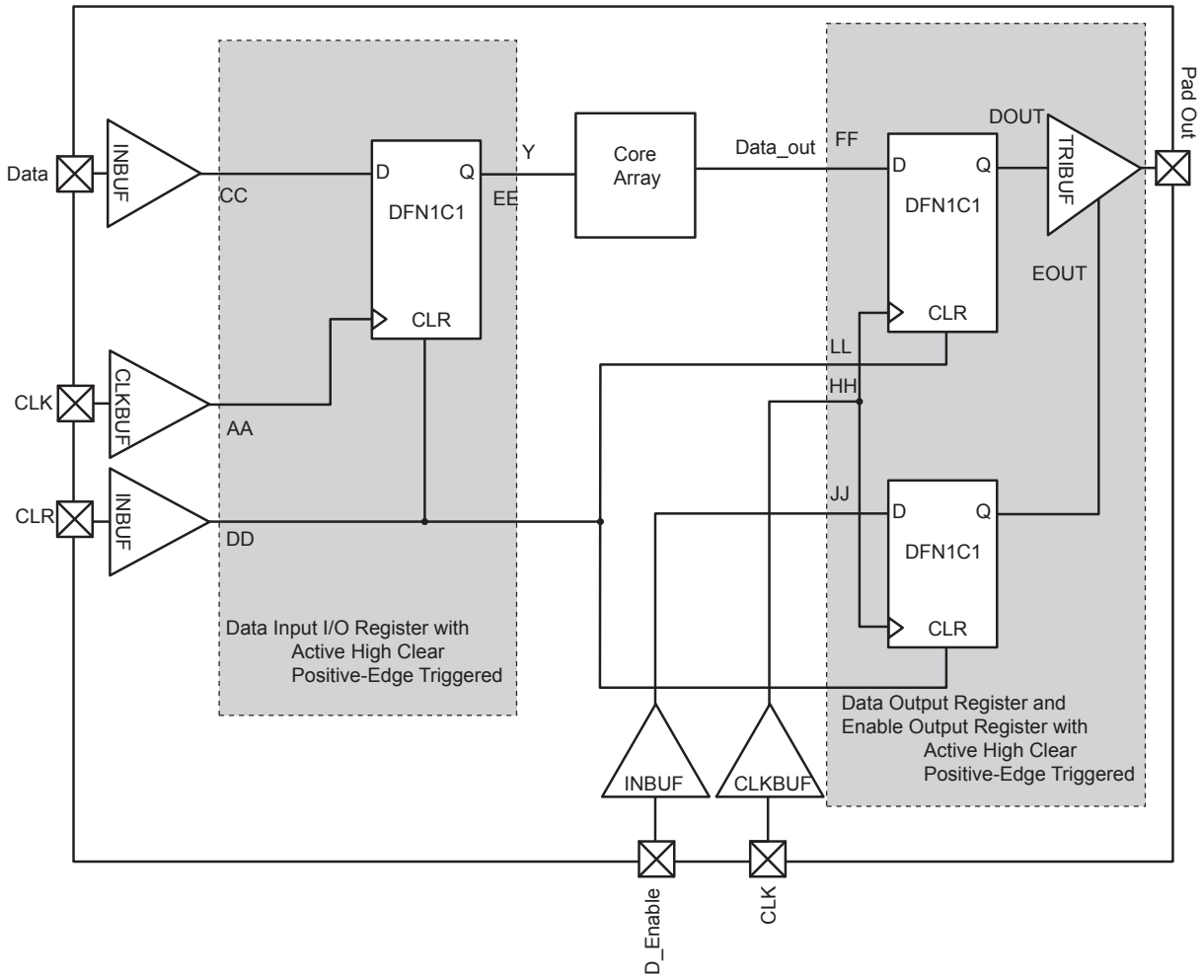


Figure 2-13 • **Timing Model of the Registered I/O Buffers with Asynchronous Clear**

1.2 V DC Core Voltage

Table 2-75 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.66	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.43	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.86	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.86	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

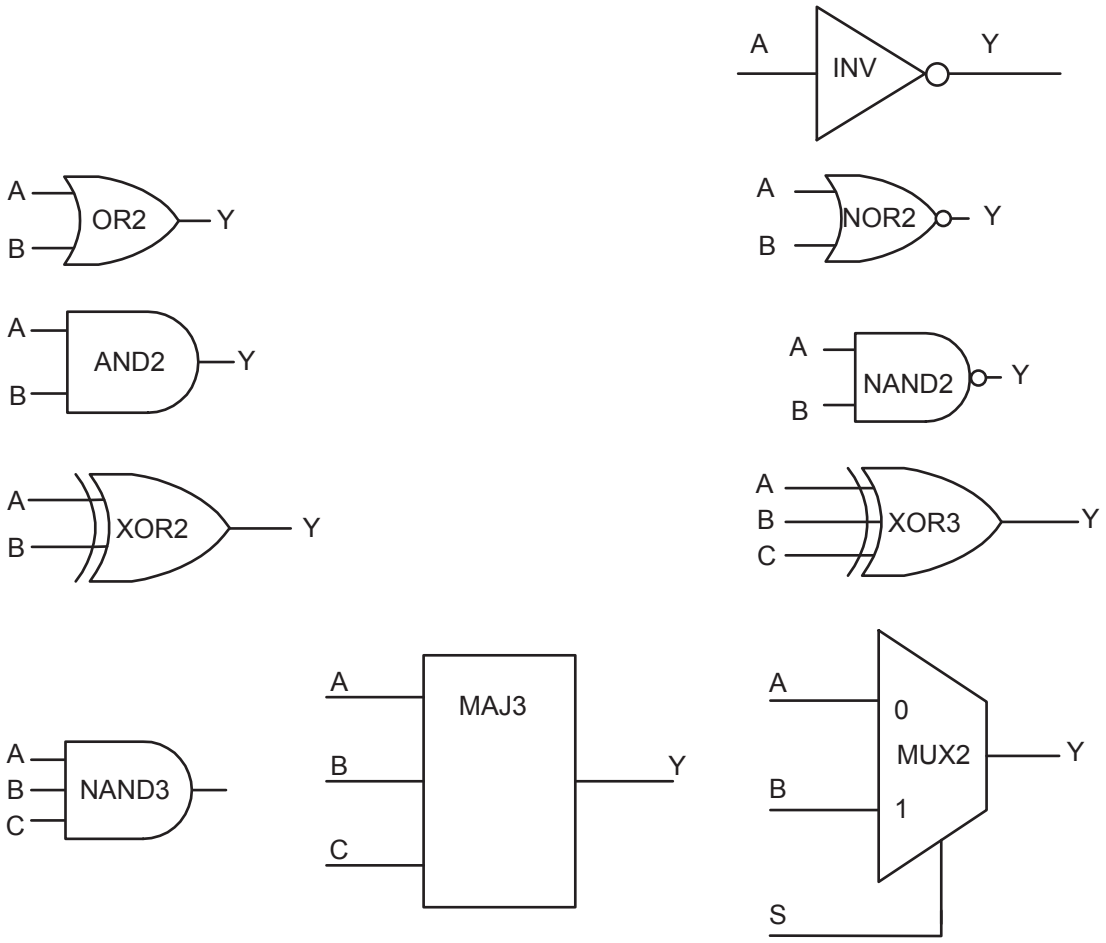


Figure 2-17 • **Sample of Combinatorial Cells**

1.2 V DC Core Voltage

***Table 2-83* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Global Resource Characteristics

AGLP125 Clock Tree Topology

Clock delays are device-specific. Figure 2-21 is an example of a global tree used for clock routing. The global tree presented in Figure 2-21 is driven by a CCC located on the west side of the AGLP125 device. It is used to drive all D-flip-flops in the device.

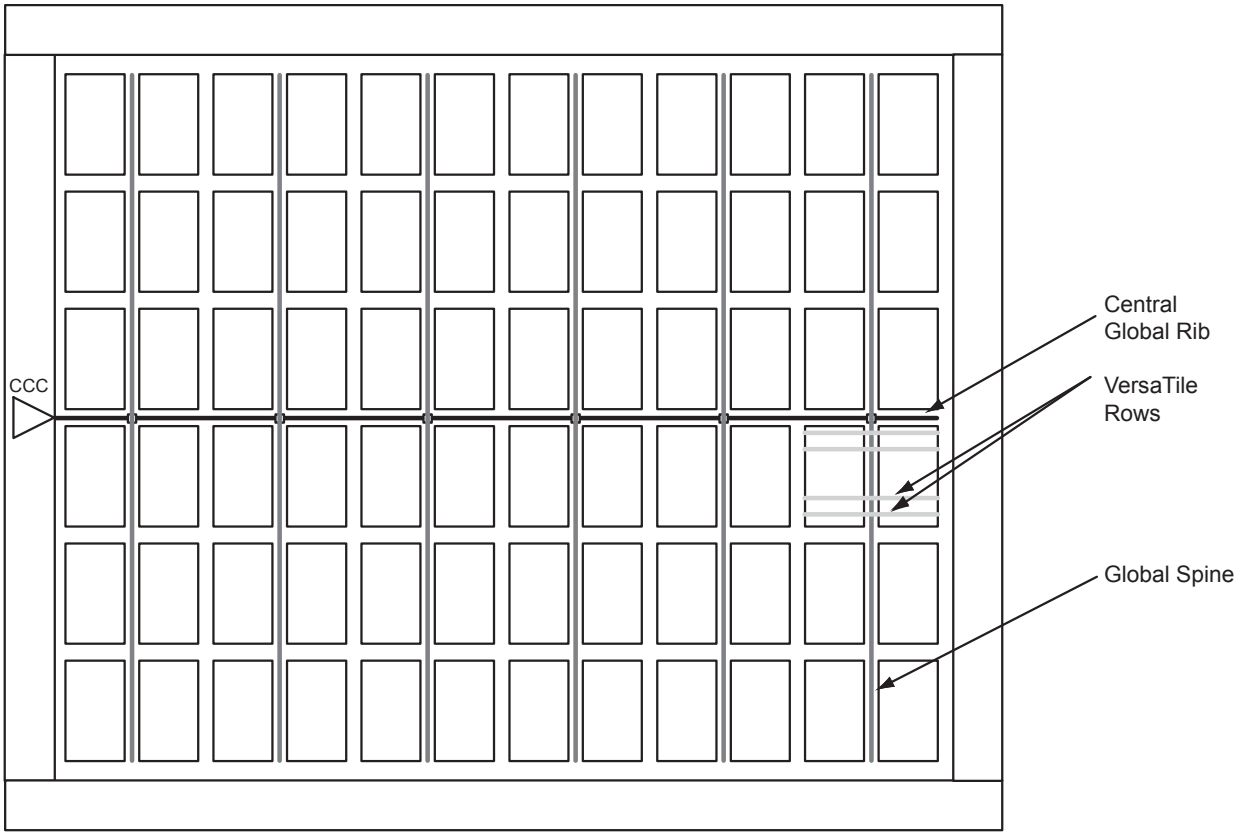


***Figure 2-21* • Example of Global Tree Use in an AGLP125 Device for Clock Routing**

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-90 • IGLOO PLUS CCC/PLL Specification
For IGLOO PLUS V2 or V5 devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	0.60%	0.80%	1.20%
50 MHz to 250 MHz	2.50%	4.00%	6.00%	12.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions. For specific junction temperature and voltage supply, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support a PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate, VCC/VCCPLL = 1.425 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide.*

Table 2-91 • IGLOO PLUS CCC/PLL Specification
For IGLOO PLUS V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4,5]			60	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			.25	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.863		20.86	ns
Delay Range in Block: Fixed Delay [1, 2]		5.7		ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT}[7]	Maximum Peak-to-Peak Period Jitter[7,8,9]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16
0.75 MHz to 50 MHz	0.50%	1.20%	2.00%	3.00%
50 MHz to 160 MHz	2.50%	5.00%	7.00%	15.00%

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for deratings.*
2. *T_J = 25°C, VCC = 1.2 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the online help associated with the core for more information.*
4. *Maximum value obtained for a STD speed grade device in Worst Case Commercial Conditions.For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-6 for derating values.*
5. *The AGLP030 device does not support PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*
7. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the per cent jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, regardless of the output divider settings.*
8. *Measurements are done with LVTTL 3.3 V, 8 mA, I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.*
9. *SSO are outputs that are synchronous to a single clock domain, and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO PLUS FPGA Fabric User's Guide*

Embedded SRAM and FIFO Characteristics

SRAM

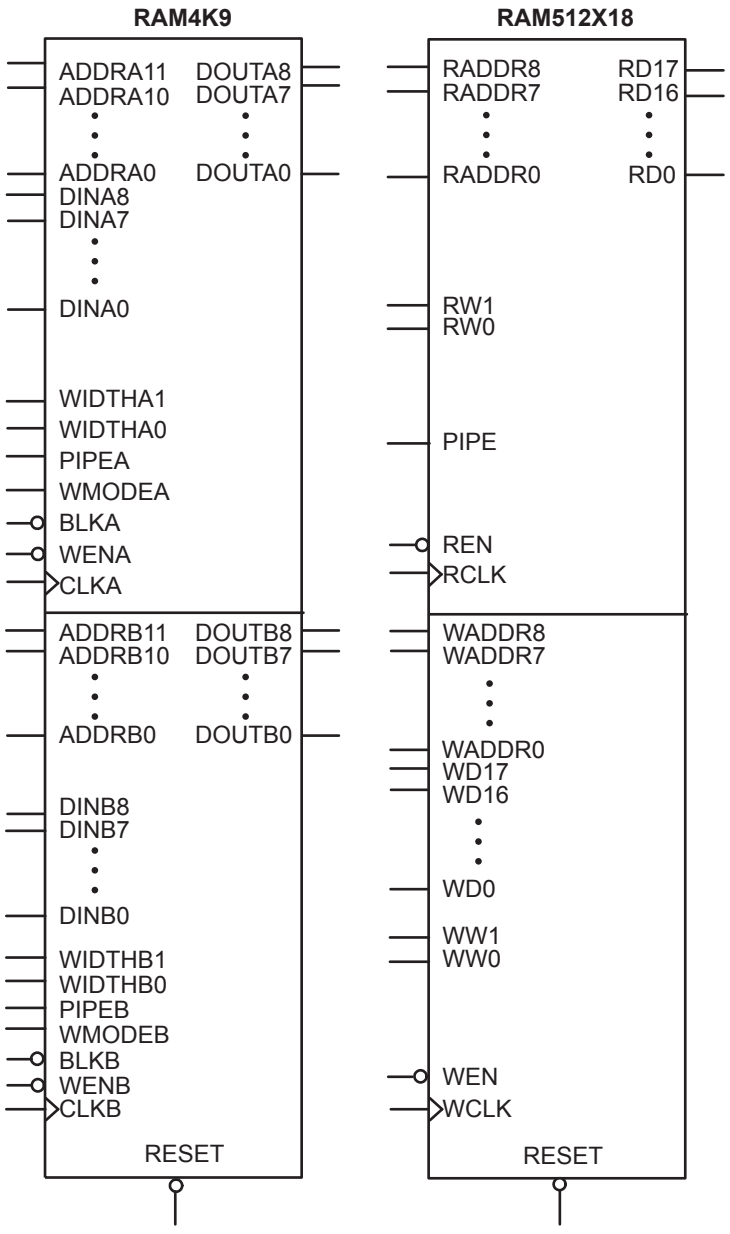


Figure 2-23 • **RAM Models**

Timing Characteristics

1.5 V DC Core Voltage

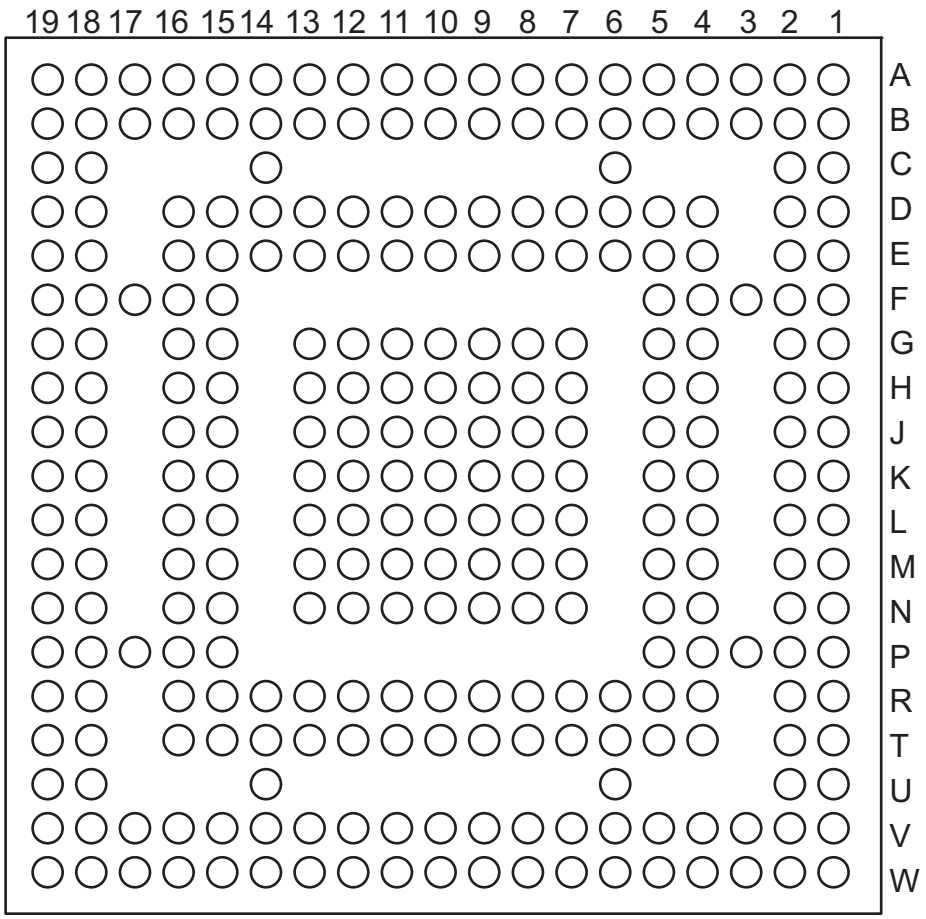
Table 2-96 • FIFO

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	1.68	ns
	RESET Low to Data Out Low on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

CS281



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx

CS289	
Pin Number	AGLP030 Function
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0

CS289	
Pin Number	AGLP030 Function
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC

CS289	
Pin Number	AGLP030 Function
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

CS289	
Pin Number	AGLP030 Function
P2	NC
P3	GND
P4	NC
P5	NC
P6	IO87RSB2
P7	IO80RSB2
P8	GND
P9	IO72RSB2
P10	IO67RSB2
P11	IO61RSB2
P12	NC
P13	VCCIB2
P14	NC
P15	IO60RSB2
P16	IO62RSB2
P17	VJTAG
R1	GND
R2	IO91RSB2
R3	NC
R4	NC
R5	NC
R6	VCCIB2
R7	IO83RSB2
R8	IO78RSB2
R9	IO74RSB2
R10	IO70RSB2
R11	GND
R12	NC
R13	NC
R14	NC
R15	NC
R16	TMS
R17	TRST
T1	IO92RSB3
T2	IO89RSB2
T3	NC
T4	GND

CS289	
Pin Number	AGLP030 Function
T5	NC
T6	IO84RSB2
T7	IO81RSB2
T8	IO76RSB2
T9	VCCIB2
T10	IO69RSB2
T11	IO65RSB2
T12	IO64RSB2
T13	NC
T14	GND
T15	NC
T16	TDI
T17	TDO
U1	FF/IO90RSB2
U2	GND
U3	NC
U4	IO88RSB2
U5	IO86RSB2
U6	IO82RSB2
U7	GND
U8	IO75RSB2
U9	IO73RSB2
U10	IO68RSB2
U11	IO66RSB2
U12	GND
U13	NC
U14	NC
U15	NC
U16	TCK
U17	VPUMP

Revision	Changes	Page
Revision 12 (continued)	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—P_{CLOCK}" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO PLUS FPGA Fabric User's Guide* (SAR 34733).	2-12
	t_{DOUT} was corrected to t_{DIN} in Figure 2-4 • Input Buffer Timing Model and Delays (example) (SAR 37107).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34887).	2-27
	Minimum pulse width High and Low values were added to the tables in the "Global Tree Timing Characteristics" section. The maximum frequency for global clock parameter was removed from these tables because a frequency on the global is only an indication of what the global network can do. There are other limiters such as the SRAM, I/Os, and PLL. SmartTime software should be used to determine the design frequency (SAR 36963).	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 34820). The value for serial clock was missing from these tables and has been restored. The value and units for input cycle-to-cycle jitter were incorrect and have been restored. The note to Table 2-90 • IGLOO PLUS CCC/PLL Specification giving specifications for which measurements done was corrected from VCC/VCCPLL = 1.14 V to VCC/VCCPLL = 1.425 V. The Delay Range in Block: Programmable Delay 2 value in Table 2-91 • IGLOO PLUS CCC/PLL Specification was corrected from 0.025 to 0.863 (SAR 37058).	2-61, 2-62
	Figure 2-28 • Write Access after Read onto Same Address was deleted. Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34868). The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-32 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SAR 35748).	2-65, 2-68, 2-74, 2-76
	The "Pin Descriptions and Packaging" chapter has been added (SAR 34769).	3-1
	Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 34769).	4-1
Revision 11 (July 2010)	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO PLUS Device Status" table indicates the status for each device in the family.	N/A
	The "Reprogrammable Flash Technology" section was revised to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	The "I/Os with Advanced I/O Standards" section was revised to add definitions for hot-swap and cold-sparing.	1-6
	Conditional statements regarding hot insertion were removed from the description of VI in Table 2-1 • Absolute Maximum Ratings, since all IGLOO PLUS devices are hot insertion enabled.	2-1