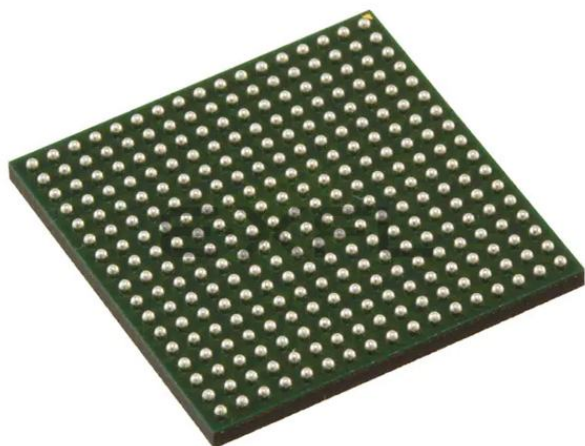




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	120
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	289-TFBGA, CSBGA
Supplier Device Package	289-CSP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v5-csg289

The IGLOO PLUS family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO PLUS family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO PLUS flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO PLUS FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO PLUS family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130 nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO PLUS family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO PLUS architecture provides granularity comparable to standard-cell ASICs. The IGLOO PLUS device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO PLUS core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

[†] The AGLP030 device does not support PLL or SRAM.

Each I/O module contains several input, output, and output enable registers.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO PLUS devices support JEDEC-defined wide range I/O operation. IGLOO PLUS devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-4 on page 1-8](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 – I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming Z -Tri-State: I/O is tristated

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-19 on page 2-14](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-20 on page 2-14](#).

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-20 on page 2-14](#).

PLL Contribution— P_{PLL}

$$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.¹

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($PAC13 * F_{CLKOUT}$ product) to the total PLL contribution.

- Bit 0 (LSB) = 100%
- Bit 1 = 50%
- Bit 2 = 25%
- ...
- Bit 7 (MSB) = 0.78125%
- Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-19 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-20 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

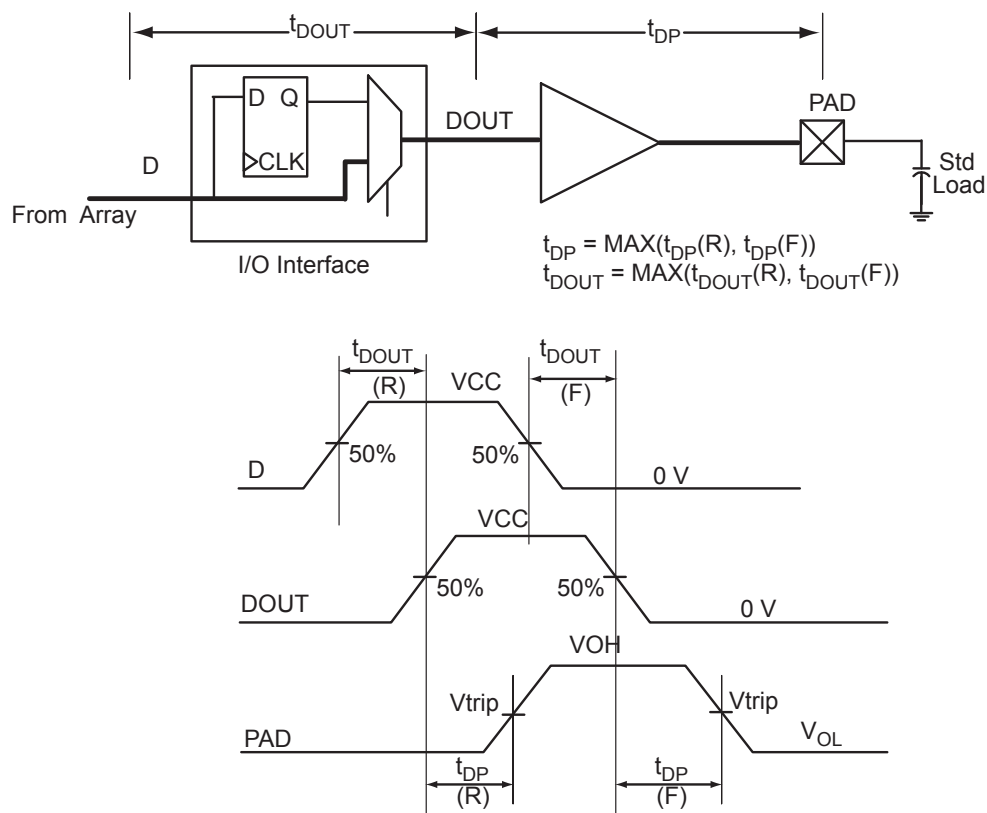


Figure 2-5 • Output Buffer Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ³	100 μ A	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS ⁴	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Notes:

1. Currents are measured at 85°C junction temperature.
2. Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 μ A drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

Applies to 1.2 V DC Core Voltage

Table 2-44 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	6.68	0.19	1.32	1.92	0.67	6.68	5.74	3.13	3.47	ns
100 μA	6 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	8 mA	STD	0.98	5.51	0.19	1.32	1.92	0.67	5.51	4.94	3.48	4.11	ns
100 μA	12 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns
100 μA	16 mA	STD	0.98	4.75	0.19	1.32	1.92	0.67	4.75	4.36	3.73	4.52	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-45 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 μA	4 mA	STD	0.98	4.16	0.19	1.32	1.92	0.67	4.16	3.32	3.12	3.66	ns
100 μA	6 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	8 mA	STD	0.98	3.54	0.19	1.32	1.92	0.67	3.54	2.79	3.48	4.31	ns
100 μA	12 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns
100 μA	16 mA	STD	0.98	3.21	0.19	1.32	1.92	0.67	3.21	2.52	3.73	4.73	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
3. Software default selection highlighted in gray.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-46 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10
12 mA	−0.3	0.7	1.7	3.6	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

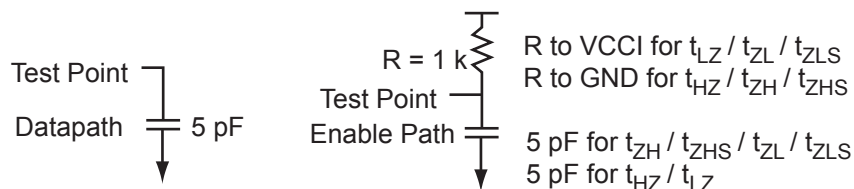


Figure 2-8 • AC Loading

Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = V_{trip}. See Table 2-23 on page 2-20 for a complete table of trip points.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-58 • Minimum and Maximum DC Input and Output Levels

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	−0.3	0.35 * VCCI	0.7 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

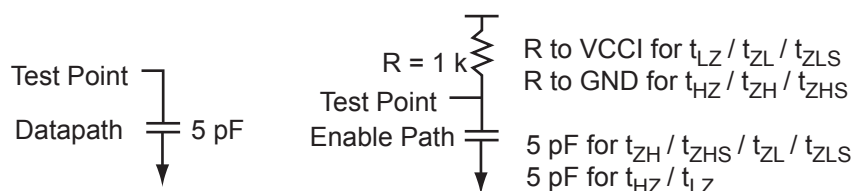


Figure 2-10 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = V_{trip} . See [Table 2-23 on page 2-20](#) for a complete table of trip points.

1.2 V LVCMOS Wide Range

Table 2-68 • Minimum and Maximum DC Input and Output Levels

1.2 V LVCMOS Wide Range ¹		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ³	IIH ⁴
Drive Strength	Equivalent Software Default Drive Strength Option ²	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁵	Max. mA ⁵	μA ⁶	μA ⁶
100 μA	2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. Applicable to V2 devices only.
2. The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3 \text{ V} < V_{IN} < V_{IL}$.
4. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
5. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
6. Currents are measured at 85°C junction temperature.
7. Software default selection highlighted in gray.

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-23 on page 2-20 for a complete table of trip points.

Table 2-72 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t_{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t_{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t_{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
t_{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-12 on page 2-41 for more information.

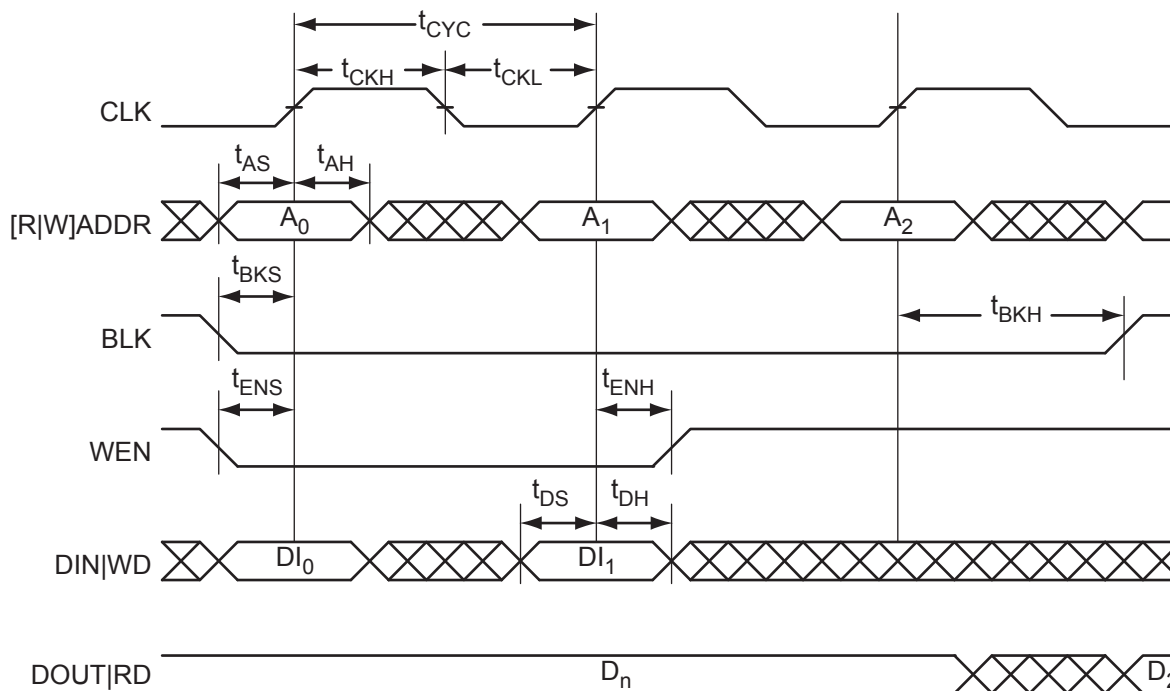


Figure 2-26 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

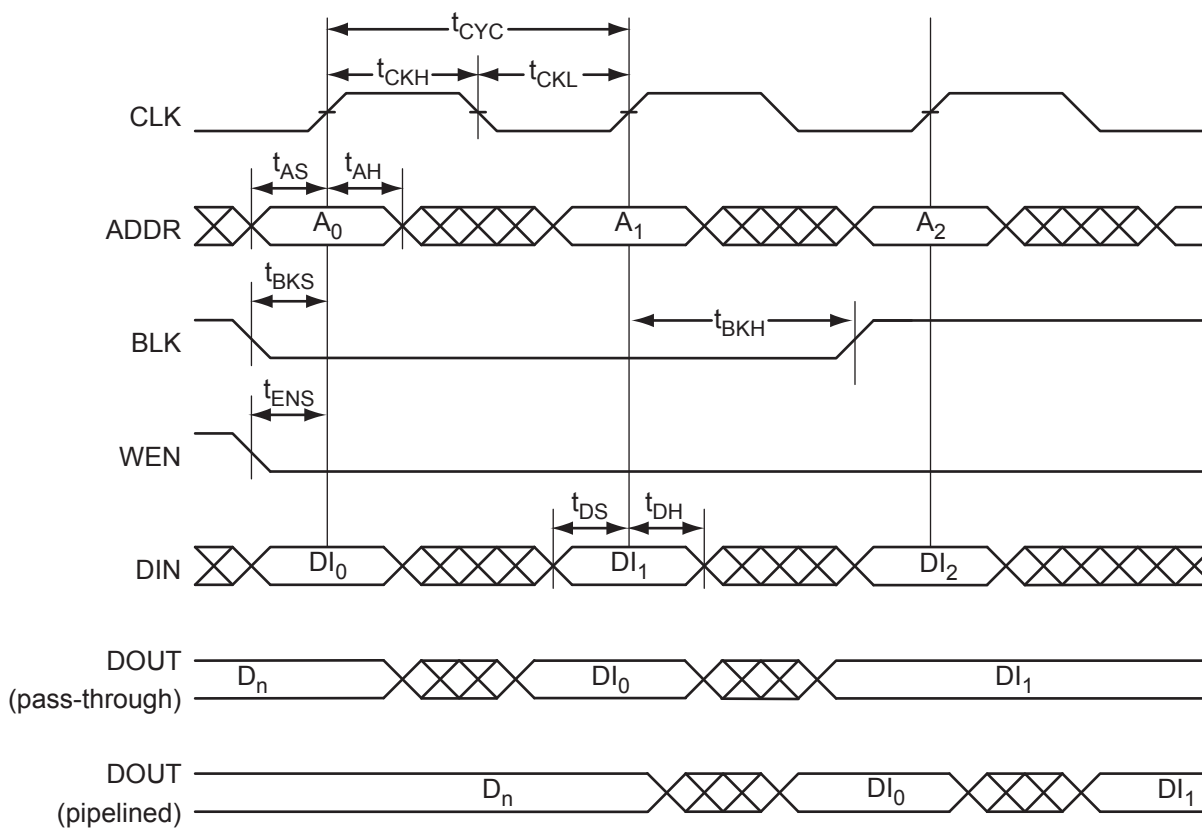


Figure 2-27 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.

1.2 V DC Core Voltage

Table 2-94 • RAM4K9

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.25	ns
t_{ENH}	REN, WEN hold time	0.25	ns
t_{BKS}	BLK setup time	2.54	ns
t_{BKH}	BLK hold time	0.25	ns
t_{DS}	Input data (DIN) setup time	1.10	ns
t_{DH}	Input data (DIN) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	5.51	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	2.82	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address – applicable to closing edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address – applicable to opening edge	0.32	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address – applicable to opening edge	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.21	ns
	RESET Low to data out Low on DOUT (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Waveforms

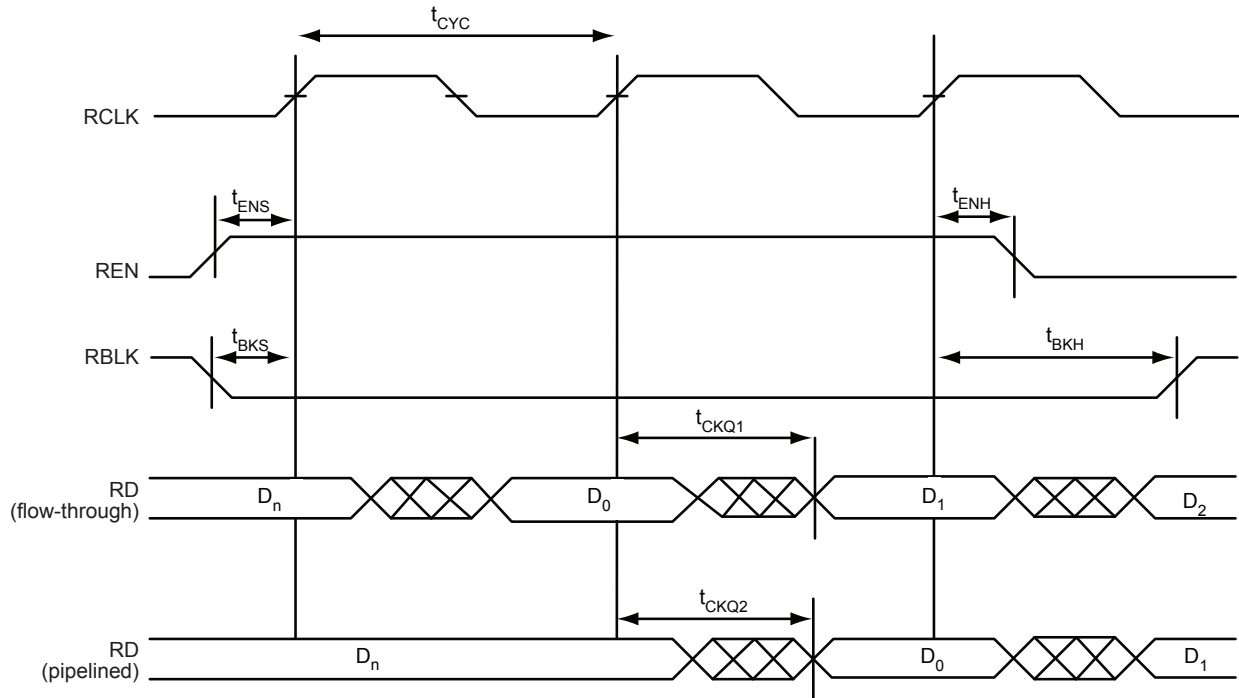


Figure 2-30 • FIFO Read

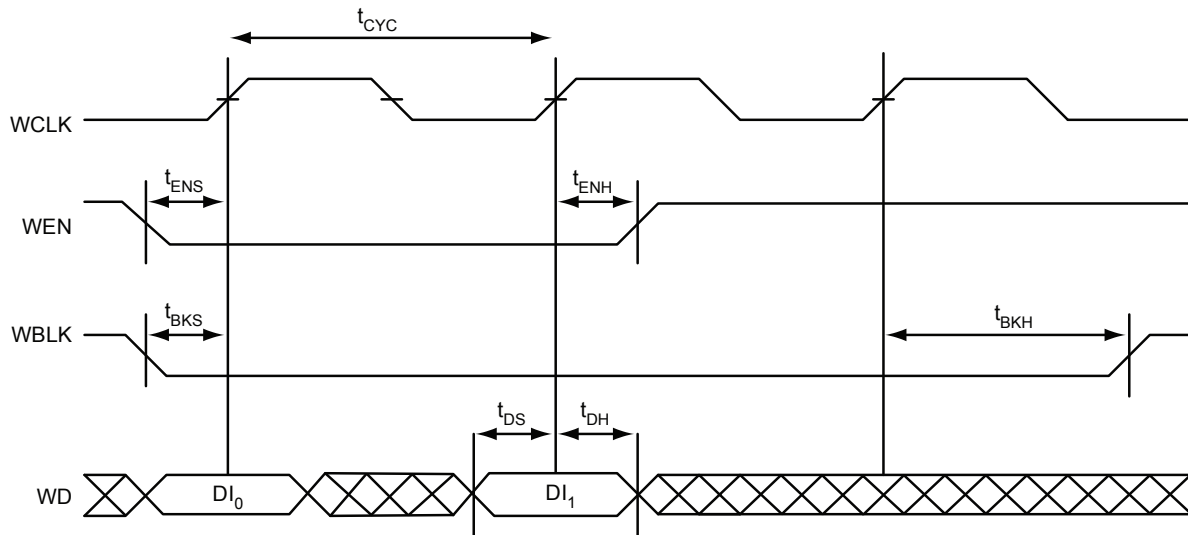


Figure 2-31 • FIFO Write

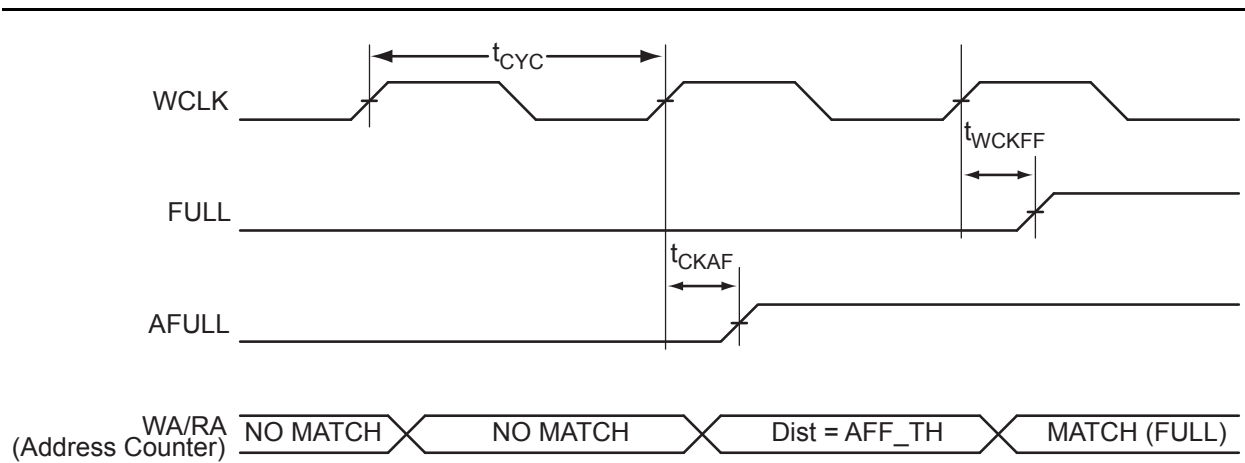


Figure 2-34 • FIFO FULL Flag and AFULL Flag Assertion

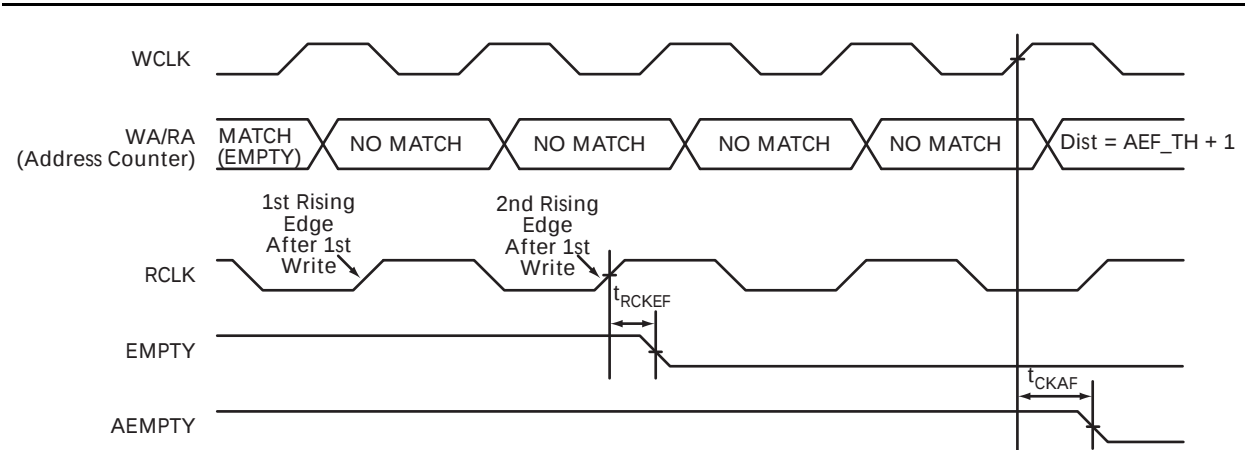


Figure 2-35 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

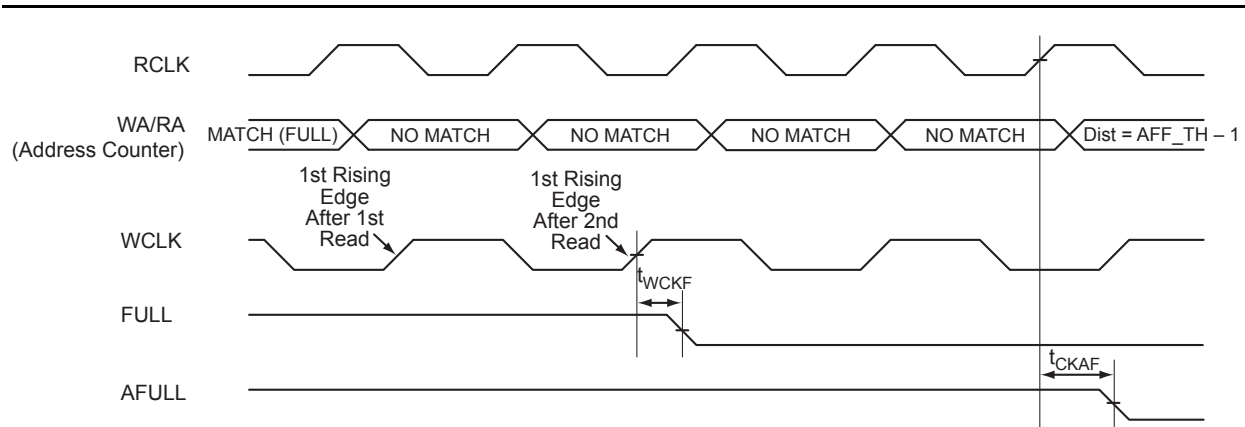


Figure 2-36 • FIFO FULL Flag and AFULL Flag Deassertion

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO PLUS devices.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOO PLUS devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

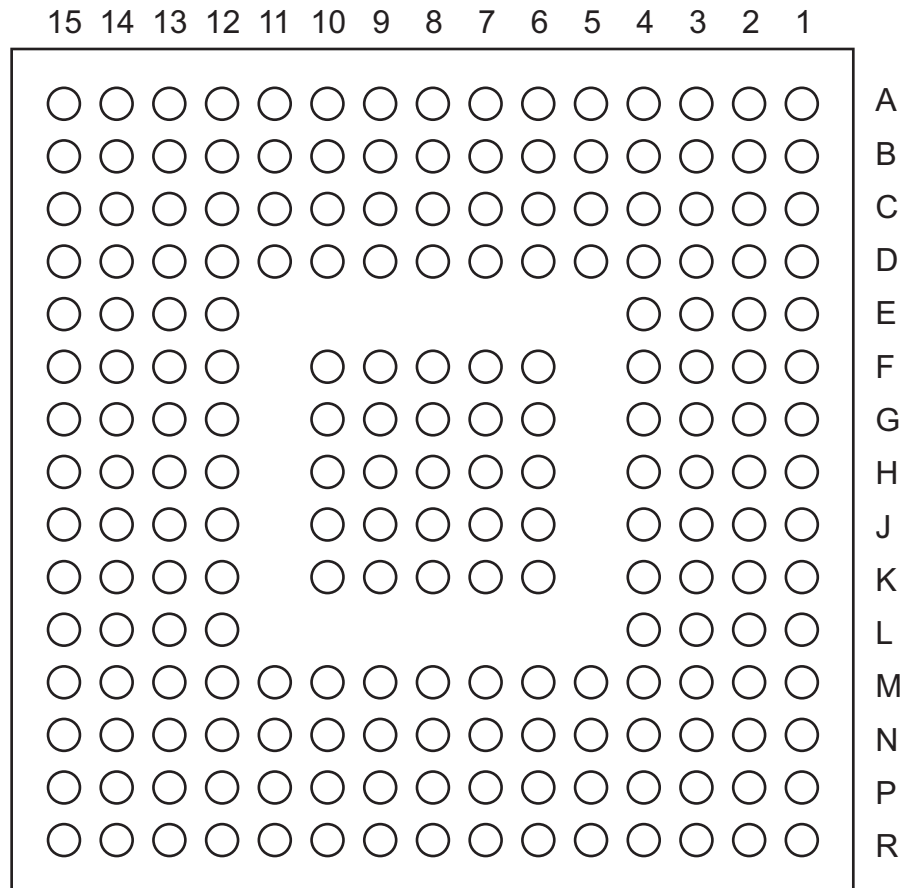
GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO PLUS FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure chapter of the *IGLOO PLUS FPGA Fabric User's Guide* for an explanation of the naming of global pins.

CS201



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.microsemi.com/soc/products/solutions/package/docs.aspx>.

CS281	
Pin Number	AGLP125 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO23RSB0
A9	IO25RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO41RSB0
A13	IO43RSB0
A14	IO46RSB0
A15	IO55RSB0
A16	IO56RSB0
A17	GBC1/IO58RSB0
A18	GBA0/IO61RSB0
A19	GND
B1	GAA2/IO211RSB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO11RSB0
B6	GND
B7	IO21RSB0
B8	IO22RSB0
B9	IO28RSB0
B10	IO32RSB0
B11	IO36RSB0
B12	IO39RSB0
B13	IO42RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO57RSB0
B17	GBA1/IO62RSB0

CS281	
Pin Number	AGLP125 Function
B18	VCCIB1
B19	IO64RSB1
C1	GAB2/IO209RSB3
C2	IO210RSB3
C6	IO12RSB0
C14	IO47RSB0
C18	IO54RSB0
C19	GBB2/IO65RSB1
D1	IO206RSB3
D2	IO208RSB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO10RSB0
D7	IO17RSB0
D8	IO24RSB0
D9	IO27RSB0
D10	GND
D11	IO31RSB0
D12	IO40RSB0
D13	IO49RSB0
D14	IO45RSB0
D15	GBB0/IO59RSB0
D16	GBA2/IO63RSB1
D18	GBC2/IO67RSB1
D19	IO66RSB1
E1	IO203RSB3
E2	IO205RSB3
E4	IO07RSB0
E5	IO06RSB0
E6	IO14RSB0
E7	IO20RSB0
E8	IO29RSB0
E9	IO34RSB0
E10	IO30RSB0
E11	IO37RSB0
E12	IO38RSB0

CS281	
Pin Number	AGLP125 Function
E13	IO48RSB0
E14	GBB1/IO60RSB0
E15	IO53RSB0
E16	IO69RSB1
E18	IO68RSB1
E19	IO71RSB1
F1	IO198RSB3
F2	GND
F3	IO201RSB3
F4	IO204RSB3
F5	IO16RSB0
F15	IO50RSB0
F16	IO74RSB1
F17	IO72RSB1
F18	GND
F19	IO73RSB1
G1	IO195RSB3
G2	IO200RSB3
G4	IO202RSB3
G5	IO08RSB0
G7	GAC2/IO207RSB3
G8	VCCIB0
G9	IO26RSB0
G10	IO35RSB0
G11	IO44RSB0
G12	VCCIB0
G13	IO51RSB0
G15	IO70RSB1
G16	IO75RSB1
G18	GCC0/IO80RSB1
G19	GCB1/IO81RSB1
H1	GFB0/IO191RSB3
H2	IO196RSB3
H4	GFC1/IO194RSB3
H5	GFB1/IO192RSB3
H7	VCCIB3

Revision	Changes	Page
Revision 11 (continued)	The tables in the "Single-Ended I/O Characteristics" section were updated. Notes clarifying IIL and IIH were added. Tables for 3.3 V LVCMOS and 1.2 V LVCMOS wide range were added (SAR 79370, SAR 79353, and SAR 79366). Notes in the wide range tables state that the minimum drive strength for any LVCMOS 3.3 V (or LVCMOS 1.2 V) software configuration when run in wide range is $\pm 100 \mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-27
	The following sentence was deleted from the "2.5 V LVCMOS" section: It uses a 5 V–tolerant input buffer and push-pull output buffer (SAR 24916).	2-32
	The tables in the "Input Register" section, "Output Register" section, and "Output Enable Register" section were updated. The tables in the "VersaTile Characteristics" section were updated.	2-45 through 2-56
	The following tables were updated in the "Global Tree Timing Characteristics" section: Table 2-85 • AGLP060 Global Resource (1.5 V) Table 2-86 • AGLP125 Global Resource (1.5 V) Table 2-88 • AGLP060 Global Resource (1.2 V)	2-58
	Table 2-90 • IGLOO PLUS CCC/PLL Specification and Table 2-91 • IGLOO PLUS CCC/PLL Specification were revised (SAR 79388). VCO output jitter and maximum peak-to-peak jitter data were changed. Three notes were added to the table in connection with these changes.	2-61
	Figure 2-28 • Write Access after Write onto Same Address and Figure 2-29 • Write Access after Read onto Same Address were deleted.	N/A
	The tables in the "SRAM" , "FIFO" and "Embedded FlashROM Characteristics" sections were updated.	2-68, 2-78



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