Microchip Technology - AGLP030V5-VQG128 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	792
Total RAM Bits	-
Number of I/O	101
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	128-TQFP
Supplier Device Package	128-VTQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/aglp030v5-vqg128

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

I/Os Per Package [1]

IGLOO PLUS Devices	AGLP030	AGLP060	AGLP125
Package	**Single-Ended I/Os**		
CS201	120	157	–
CS281	–	–	212
CS289	120	157	212
VQ128	101	–	–
VQ176	–	137	–

*Note: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*

Table 2 • IGLOO PLUS FPGAs Package Size Dimensions

Package	CS201	CS281	CS289	VQ128	VQ176
Length × Width (mm/mm)	8 × 8	10 × 10	14 × 14	14 × 14	20 × 20
Nominal Area (mm2)	64	100	196	196	400
Pitch (mm)	0.5	0.5	0.8	0.4	0.4
Height (mm)	0.89	1.05	1.20	1.0	1.0

IGLOO PLUS Device Status

IGLOO PLUS Device	Status
AGLP030	Production
AGLP060	Production
AGLP125	Production

IGLOO PLUS Ordering Information

AGLP125 V2 – CS G 289 Y I

Application (Temperature Range)
Blank = Commercial (0°C to +85°C junction temperature)
I = Industrial (–40°C to +100°C junction temperature)
PP = Pre-Production
ES = Engineering Sample (room temperature only)

Security Feature
Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G= RoHS-Compliant Packaging

Package Type
CS = Chip Scale Package (0.5 mm and 0.8 mm pitches)
VQ = Very Thin Quad Flat Pack (0.4 mm pitch)

Supply Voltage
2 = 1.2 V to 1.5 V
5 = 1.5 V only

Part Number
AGLP030 = 30,000 System Gates
AGLP060 = 60,000 System Gates
AGLP125 = 125,000 System Gates

1. *Marking information: IGLOO PLUS V2 devices do not have a V2 marking, but IGLOO PLUS V5 devices are marked accordingly.*
2. *"G" indicates RoHS-compliant packages.*

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-21 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD 3 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4,5]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	0.1	0.1

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range are applicable to 100 µA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to IGLOO PLUS V2 devices operating at $VCC_I \geq VCC$.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-24 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
VCCI	**Min.**	**Max.**	**Min.**	**Max.**
3.3 V	10 K	45 K	10 K	45 K
3.3 V (wide range I/Os)	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V (wide range I/Os)	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULLDOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULLDOWN\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
1.2 V LVCMOS	2 mA	26	20
1.2 V LVCMOS Wide Range	100 µA	26	20

Note: *T_J = 100°C

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-42 **• 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.97	5.85	0.18	1.18	1.64	0.66	5.86	5.05	2.57	2.57	ns
100 µA	6 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 µA	8 mA	STD	0.97	4.70	0.18	1.18	1.64	0.66	4.72	4.27	2.92	3.19	ns
100 µA	12 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns
100 µA	16 mA	STD	0.97	3.96	0.18	1.18	1.64	0.66	3.98	3.70	3.16	3.59	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-43 **• 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	4 mA	STD	0.97	3.39	0.18	1.18	1.64	0.66	3.41	2.69	2.57	2.73	ns
100 µA	6 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 µA	8 mA	STD	0.97	2.79	0.18	1.18	1.64	0.66	2.80	2.17	2.92	3.36	ns
100 µA	12 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns
100 µA	16 mA	STD	0.97	2.47	0.18	1.18	1.64	0.66	2.48	1.91	3.16	3.76	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

Timing Characteristics

Applies to 1.2 V DC Core Voltage

***Table 2-70* • 1.2 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	8.27	0.19	1.57	2.34	0.67	7.94	6.77	3.00	3.11	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-71* • 1.2 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.98	3.38	0.19	1.57	2.34	0.67	3.26	2.78	2.99	3.24	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
3. *Software default selection highlighted in gray.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO PLUS library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/ E Macro Library Guide*.

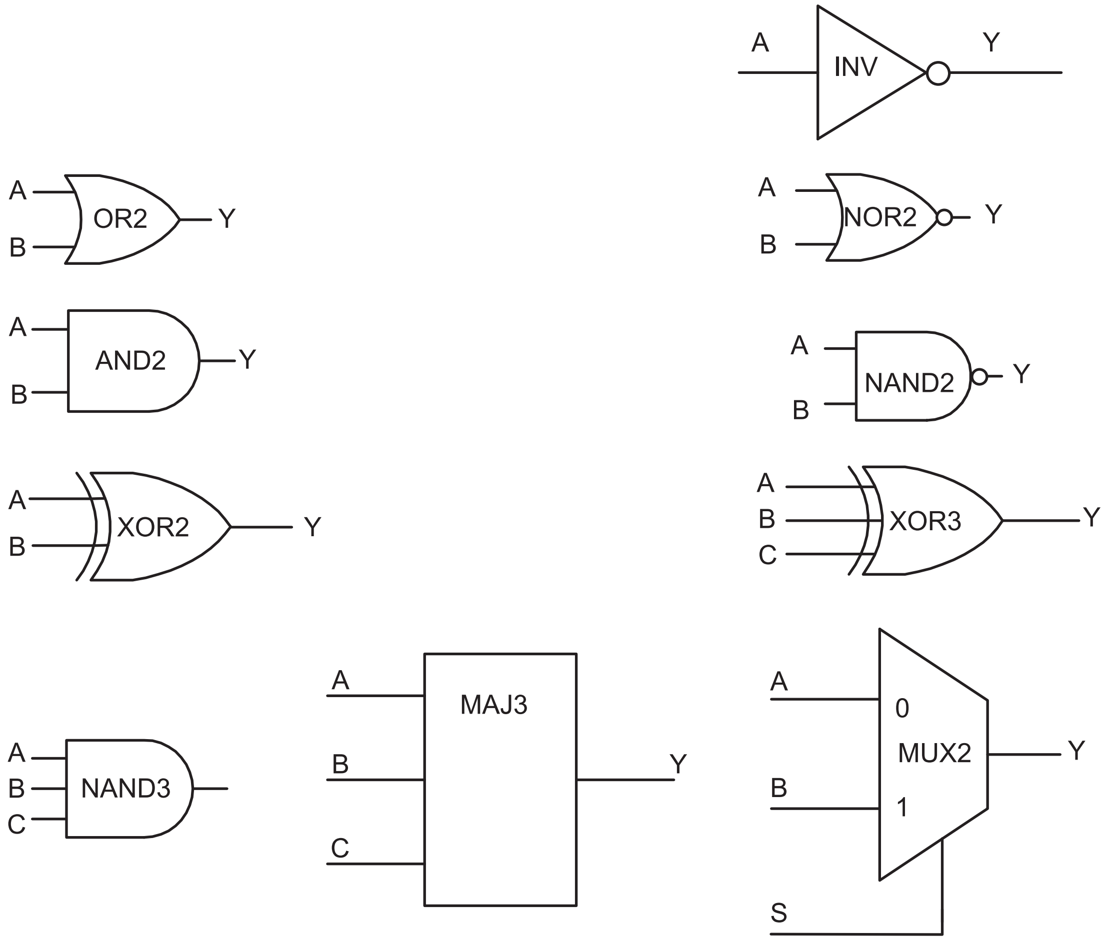

Figure 2-17 • Sample of Combinatorial Cells

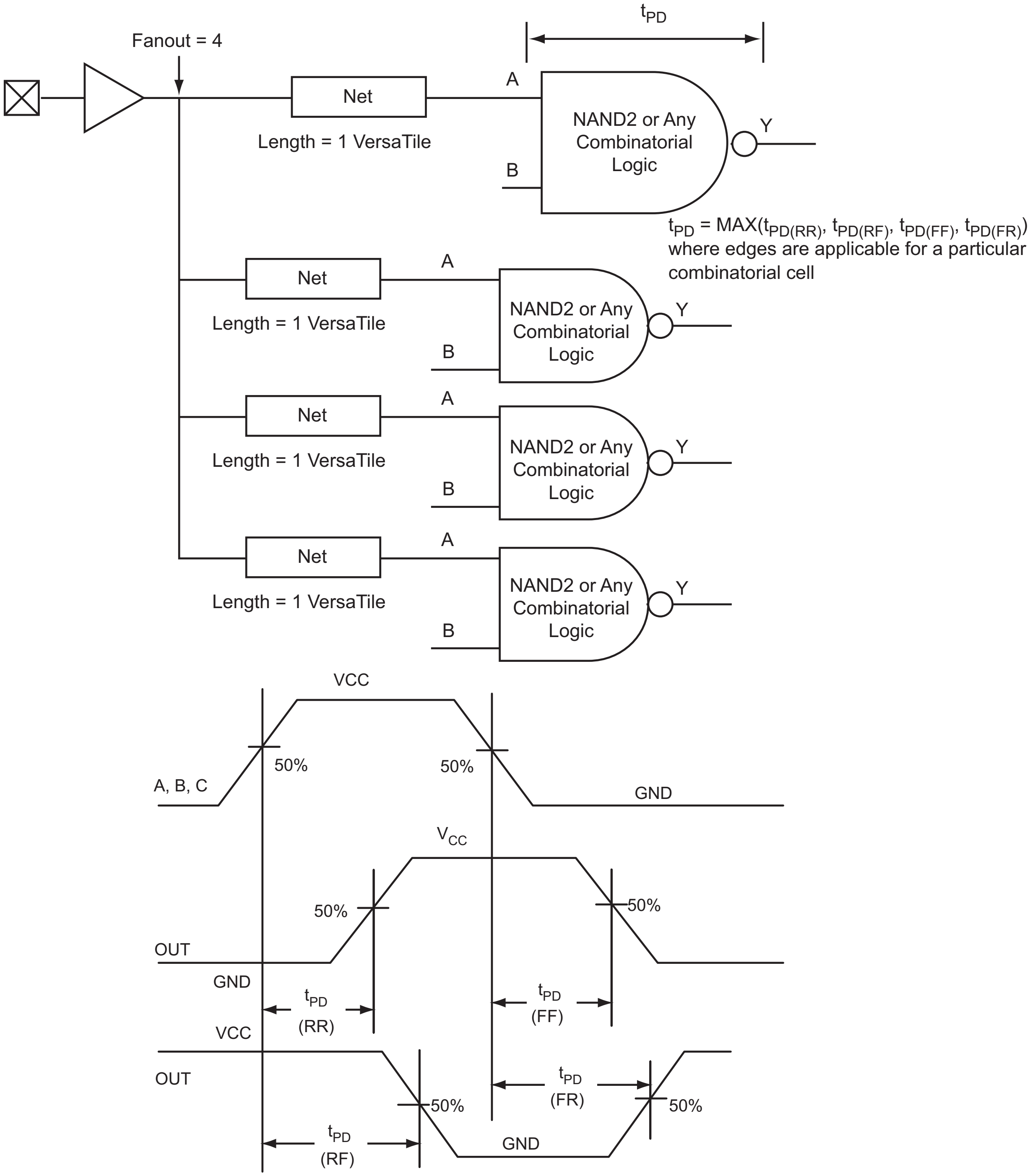

***Figure 2-18* • Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-80 **• Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.72	ns
AND2	Y = A · B	t_{PD}	0.86	ns
NAND2	Y = !(A · B)	t_{PD}	1.00	ns
OR2	Y = A + B	t_{PD}	1.26	ns
NOR2	Y = !(A + B)	t_{PD}	1.16	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.47	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	2.12	ns
MUX2	Y = A !S + B S	t_{PD}	1.24	ns
AND3	Y = A · B · C	t_{PD}	1.40	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-81 **• Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.26	ns
AND2	Y = A · B	t_{PD}	1.46	ns
NAND2	Y = !(A · B)	t_{PD}	1.78	ns
OR2	Y = A + B	t_{PD}	2.47	ns
NOR2	Y = !(A + B)	t_{PD}	2.17	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.62	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.66	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.77	ns
MUX2	Y = A !S + B S	t_{PD}	2.20	ns
AND3	Y = A · B · C	t_{PD}	2.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-86 • AGLP125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-87 • AGLP030 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

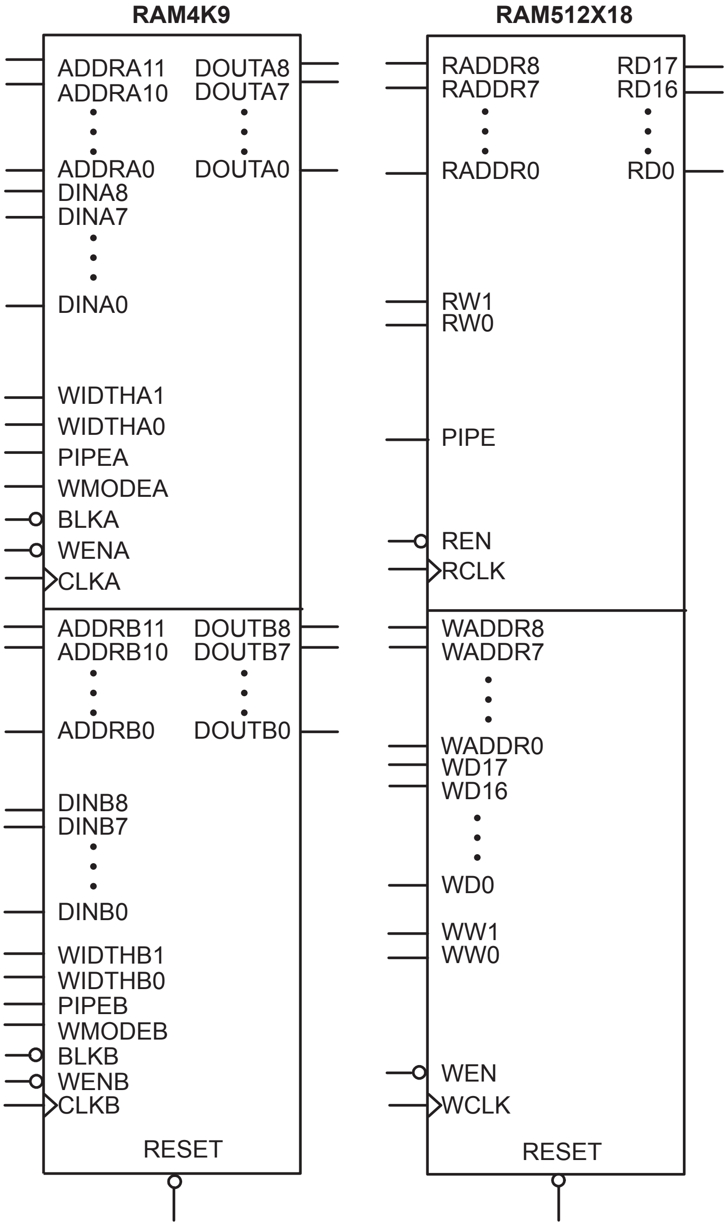

Figure 2-23 **• RAM Models**

Timing Waveforms

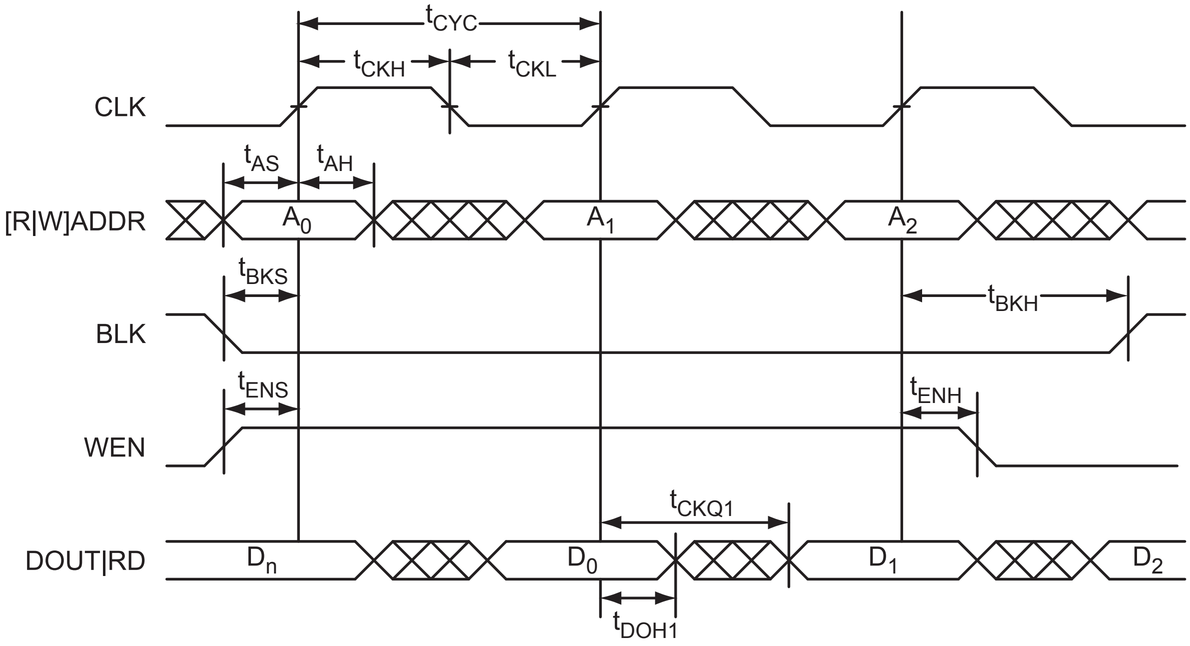

Figure 2-24 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

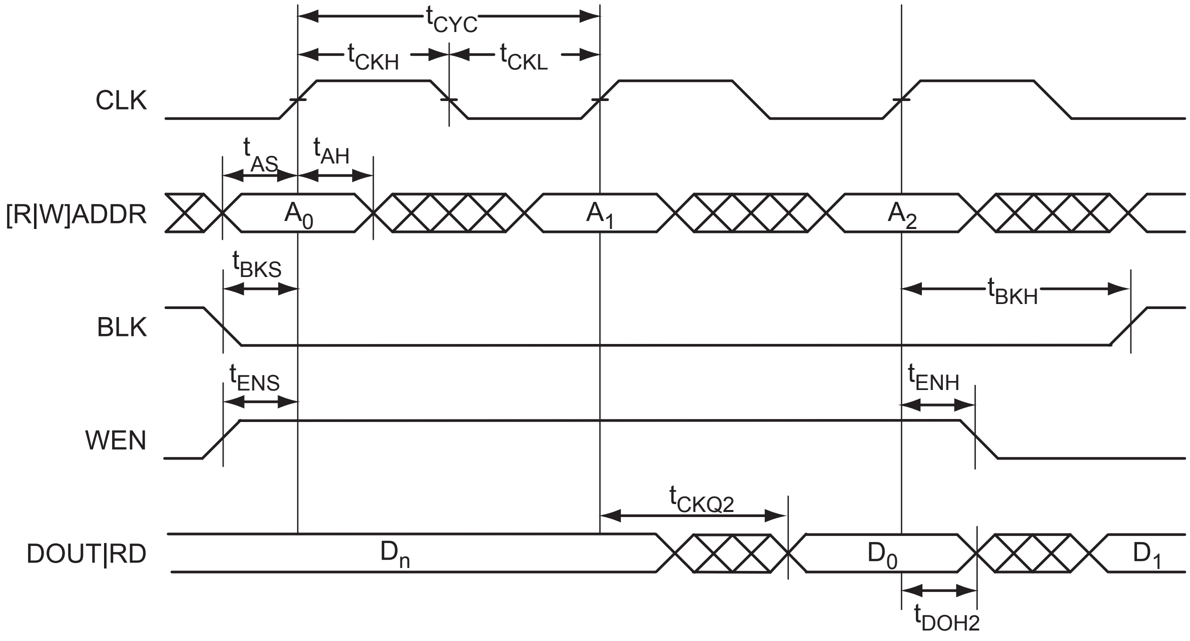

Figure 2-25 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 **• Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC	**No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC	**Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Microsemi consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microsemi IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microsemi offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

Related Documents

IGLOO PLUS Device Family User's Guide

http://www.microsemi.com/soc/documents/IGLOOPLUS_UG.pdf

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Microsemi. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are available at
http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

CS201	
Pin Number	AGLP030 Function
H14	IO45RSB1
H15	IO43RSB1
J1	GEA0/IO107RSB3
J2	IO105RSB3
J3	IO104RSB3
J4	IO102RSB3
J6	VCCIB3
J7	GND
J8	VCC
J9	GND
J10	VCCIB1
J12	NC
J13	NC
J14	IO52RSB1
J15	IO50RSB1
K1	IO103RSB3
K2	IO101RSB3
K3	IO99RSB3
K4	IO100RSB3
K6	GND
K7	VCCIB2
K8	VCCIB2
K9	VCCIB2
K10	VCCIB1
K12	NC
K13	IO57RSB1
K14	IO49RSB1
K15	IO53RSB1
L1	IO96RSB3
L2	IO98RSB3
L3	IO95RSB3
L4	IO94RSB3
L12	NC
L13	NC
L14	IO51RSB1

CS201	
Pin Number	AGLP030 Function
L15	IO58RSB1
M1	IO93RSB3
M2	IO92RSB3
M3	IO97RSB3
M4	GND
M5	NC
M6	IO79RSB2
M7	IO77RSB2
M8	IO72RSB2
M9	IO70RSB2
M10	IO61RSB2
M11	IO59RSB2
M12	GND
M13	NC
M14	IO55RSB1
M15	IO56RSB1
N1	NC
N2	NC
N3	GND
N4	NC
N5	IO88RSB2
N6	IO81RSB2
N7	IO75RSB2
N8	IO68RSB2
N9	IO66RSB2
N10	IO65RSB2
N11	IO71RSB2
N12	IO63RSB2
N13	GND
N14	TDO
N15	VJTAG
P1	NC
P2	NC
P3	NC
P4	NC

CS201	
Pin Number	AGLP030 Function
P5	IO87RSB2
P6	IO86RSB2
P7	IO84RSB2
P8	IO80RSB2
P9	IO74RSB2
P10	IO73RSB2
P11	IO76RSB2
P12	IO67RSB2
P13	IO64RSB2
P14	VPUMP
P15	TRST
R1	NC
R2	NC
R3	IO91RSB2
R4	FF/IO90RSB2
R5	IO89RSB2
R6	IO83RSB2
R7	IO82RSB2
R8	IO85RSB2
R9	IO78RSB2
R10	IO69RSB2
R11	IO62RSB2
R12	IO60RSB2
R13	TMS
R14	TDI
R15	TCK

CS281	
Pin Number	**AGLP125 Function**
R15	IO109RSB2
R16	GDA1/IO103RSB1
R18	GDB0/IO102RSB1
R19	GDC0/IO100RSB1
T1	IO171RSB3
T2	GEC0/IO169RSB3
T4	GEB0/IO167RSB3
T5	IO157RSB2
T6	IO158RSB2
T7	IO148RSB2
T8	IO145RSB2
T9	IO143RSB2
T10	GND
T11	IO129RSB2
T12	IO126RSB2
T13	IO125RSB2
T14	IO116RSB2
T15	GDC2/IO107RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO101RSB1
U1	IO160RSB2
U2	GEA1/IO166RSB3
U6	IO151RSB2
U14	IO121RSB2
U18	TRST
U19	GDA0/IO104RSB1
V1	IO159RSB2
V2	VCCIB3
V3	GEC2/IO162RSB2
V4	IO156RSB2
V5	IO153RSB2
V6	GND
V7	IO144RSB2
V8	IO141RSB2
V9	IO140RSB2
V10	IO133RSB2
V11	IO127RSB2
V12	IO123RSB2
V13	IO120RSB2
V14	GND
V15	IO113RSB2
V16	GDA2/IO105RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO163RSB2
W3	IO155RSB2
W4	IO152RSB2
W5	IO150RSB2
W6	IO147RSB2
W7	IO142RSB2
W8	IO139RSB2
W9	IO136RSB2
W10	VCCIB2
W11	IO128RSB2
W12	IO124RSB2
W13	IO119RSB2
W14	IO115RSB2
W15	IO114RSB2
W16	IO110RSB2
W17	GDB2/IO106RSB2
W18	TCK
W19	GND

CS289	
Pin Number	**AGLP030 Function**
A1	IO03RSB0
A2	NC
A3	NC
A4	GND
A5	IO10RSB0
A6	IO14RSB0
A7	IO16RSB0
A8	IO18RSB0
A9	GND
A10	IO23RSB0
A11	IO27RSB0
A12	NC
A13	NC
A14	GND
A15	NC
A16	NC
A17	IO30RSB0
B1	IO01RSB0
B2	GND
B3	NC
B4	NC
B5	IO07RSB0
B6	NC
B7	VCCIB0
B8	IO17RSB0
B9	IO19RSB0
B10	IO24RSB0
B11	IO28RSB0
B12	VCCIB0
B13	NC
B14	NC
B15	NC
B16	IO31RSB0
B17	GND
C1	NC
C2	IO00RSB0
C3	IO04RSB0
C4	NC
C5	VCCIB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO21RSB0
C10	GND
C11	IO29RSB0
C12	NC
C13	NC
C14	NC
C15	GND
C16	IO34RSB0
C17	NC
D1	NC
D2	IO119RSB3
D3	GND
D4	IO02RSB0
D5	NC
D6	NC
D7	NC
D8	GND
D9	IO20RSB0
D10	IO25RSB0
D11	NC
D12	NC
D13	GND
D14	IO32RSB0
D15	IO35RSB0
D16	NC
D17	NC
E1	VCCIB3
E2	IO114RSB3
E3	IO115RSB3
E4	IO118RSB3
E5	IO05RSB0
E6	NC
E7	IO06RSB0
E8	IO11RSB0
E9	IO22RSB0
E10	IO26RSB0
E11	VCCIB0
E12	NC
E13	IO33RSB0
E14	IO36RSB1
E15	IO38RSB1
E16	VCCIB1
E17	NC
F1	IO111RSB3
F2	NC
F3	IO116RSB3
F4	VCCIB3
F5	IO117RSB3
F6	NC
F7	NC
F8	IO08RSB0
F9	IO12RSB0
F10	NC
F11	NC
F12	NC
F13	NC
F14	GND
F15	NC
F16	IO37RSB1
F17	IO41RSB1
G1	IO110RSB3
G2	GND
G3	IO113RSB3
G4	NC
G5	NC
G6	NC
G7	GND
G8	GND
G9	VCC

CS289	
Pin Number	AGLP030 Function
G10	GND
G11	GND
G12	IO40RSB1
G13	NC
G14	IO39RSB1
G15	IO44RSB1
G16	NC
G17	GND
H1	NC
H2	GEC0/IO108RSB3
H3	NC
H4	IO112RSB3
H5	NC
H6	IO109RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	NC
H13	NC
H14	IO45RSB1
H15	VCCIB1
H16	GDB0/IO48RSB1
H17	IO42RSB1
J1	NC
J2	GEA0/IO107RSB3
J3	VCCIB3
J4	IO105RSB3
J5	NC
J6	NC
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	IO50RSB1

CS289	
Pin Number	AGLP030 Function
J13	IO43RSB1
J14	IO51RSB1
J15	IO52RSB1
J16	GDC0/IO46RSB1
J17	GDA0/IO47RSB1
K1	GND
K2	GEB0/IO106RSB3
K3	IO102RSB3
K4	IO104RSB3
K5	IO99RSB3
K6	NC
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	NC
K13	NC
K14	NC
K15	IO53RSB1
K16	GND
K17	IO49RSB1
L1	IO103RSB3
L2	IO101RSB3
L3	NC
L4	GND
L5	NC
L6	NC
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	IO58RSB1
L13	IO54RSB1
L14	VCCIB1
L15	NC

CS289	
Pin Number	AGLP030 Function
L16	NC
L17	NC
M1	NC
M2	VCCIB3
M3	IO100RSB3
M4	IO98RSB3
M5	IO93RSB3
M6	IO97RSB3
M7	NC
M8	NC
M9	IO71RSB2
M10	NC
M11	IO63RSB2
M12	NC
M13	IO57RSB1
M14	NC
M15	NC
M16	NC
M17	VCCIB1
N1	NC
N2	NC
N3	IO95RSB3
N4	IO96RSB3
N5	GND
N6	NC
N7	IO85RSB2
N8	IO79RSB2
N9	IO77RSB2
N10	VCCIB2
N11	NC
N12	NC
N13	IO59RSB2
N14	NC
N15	GND
N16	IO56RSB1
N17	IO55RSB1
P1	IO94RSB3

CS289	
Pin Number	AGLP060 Function
G13	IO41RSB1
G14	IO47RSB1
G15	IO49RSB1
G16	IO50RSB1
G17	GND
H1	VCOMPLF
H2	GFB0/IO137RSB3
H3	NC
H4	IO141RSB3
H5	IO143RSB3
H6	GFB1/IO138RSB3
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GCC1/IO52RSB1
H13	IO51RSB1
H14	GCA0/IO57RSB1
H15	VCCIB1
H16	GCA2/IO58RSB1
H17	GCC0/IO53RSB1
J1	VCCPLF
J2	GFA1/IO136RSB3
J3	VCCIB3
J4	IO131RSB3
J5	IO130RSB3
J6	IO129RSB3
J7	VCC
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO59RSB1
J13	GCB1/IO54RSB1
J14	IO62RSB1
J15	IO63RSB1
J16	GCB0/IO55RSB1
J17	GCA1/IO56RSB1
K1	GND
K2	GFA0/IO135RSB3
K3	GFB2/IO133RSB3
K4	IO128RSB3
K5	IO123RSB3
K6	IO125RSB3
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	IO64RSB1
K13	IO61RSB1
K14	IO66RSB1
K15	IO65RSB1
K16	GND
K17	GCC2/IO60RSB1
L1	GFA2/IO134RSB3
L2	GFC2/IO132RSB3
L3	IO127RSB3
L4	GND
L5	IO121RSB3
L6	GEC1/IO116RSB3
L7	GND
L8	GND
L9	VCC
L10	GND
L11	GND
L12	GDC1/IO72RSB1
L13	GDB1/IO74RSB1
L14	VCCIB1
L15	IO70RSB1
L16	IO68RSB1
L17	IO67RSB1
M1	IO126RSB3
M2	VCCIB3
M3	IO124RSB3
M4	IO122RSB3
M5	GEB0/IO113RSB3
M6	GEB1/IO114RSB3
M7	NC
M8	NC
M9	IO90RSB2
M10	NC
M11	IO83RSB2
M12	NC
M13	GDA1/IO76RSB1
M14	GDA0/IO77RSB1
M15	IO71RSB1
M16	IO69RSB1
M17	VCCIB1
N1	IO119RSB3
N2	IO120RSB3
N3	GEC0/IO115RSB3
N4	GEA0/IO111RSB3
N5	GND
N6	NC
N7	IO104RSB2
N8	IO98RSB2
N9	IO96RSB2
N10	VCCIB2
N11	NC
N12	NC
N13	GDB2/IO79RSB2
N14	NC
N15	GND
N16	GDB0/IO75RSB1
N17	GDC0/IO73RSB1
P1	IO118RSB3
P2	IO117RSB3
P3	GND
P4	NC
P5	NC
P6	IO106RSB2
P7	IO99RSB2